Code No: R1621042 **R16** SET - 1

II B. Tech I Semester Regular Examinations, October/November - 2017
SWITCHING THEORY AND LOGIC DESIGN
(Com to ECE, EIE and ECC)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A

1. a) Convert the binary number 11011101 to gray code. (2M)
   b) Find the dual of the function: $A'B(C+D)+B'C'D+AB'C$. (2M)
   c) What is a de-multiplexer? Write its applications. (3M)
   d) Write the merits and demerits of PROM. (2M)
   e) What are the differences between Johnson and ripple counter. (2M)
   f) What is a state diagram? Describe with an example. (3M)

PART –B

2. a) Express the following numbers in decimal: (7M)
   (i) $(26.24)_8$
   (ii) $(16.5)_{16}$
   b) Generate the Hamming code word for the message 1110010111. (7M)

3. a) Implement the following Boolean function with only two input NOR gates: (7M)
   $F=(AB'+CD')E+BC(A+B)$
   b) Simplify the following Boolean function with the don't conditions *d* using K-map method: (7M)
   $F(A, B, C, D)=\Sigma(4, 5, 7, 12, 13, 14); d(A, B, C, D)=\Sigma(1, 9, 11, 15)$

4. a) Design a 4-bit binary comparator with basic gates. (7M)
   b) Implement the following Boolean functions with a decoder. (7M)
   (i) $F1=\Sigma(3, 6, 7, 10, 13, 15)$
   (ii) $F2=\Sigma(1, 9, 12, 15)$
   (iii) $F3=\Sigma(2, 6, 8, 10, 14, 15)$

5. a) Implement the following Boolean functions using PLA. (7M)
   (i) $F1= \Sigma(0, 1, 2, 4)$
   (ii) $F2= \Sigma(0, 5, 6, 7)$
   b) Design a full adder circuit with a PAL. (7M)

6. a) Draw the circuit of a JK master slave flip-flop with active high clear and active low preset and explain its operation. (7M)
   b) Design a Mod-10 counter using RS flip-flops (7M)
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7. a) What are the capabilities and limitations of finite state machines? Explain. (7M)

b) Reduce the number of states in the following state table and tabulate the reduced state table. (7M)

PS	NS, O/P	
	X=0	X=1
a	f, 0	b, 0
b	d, 0	c, 0
c	f, 0	e, 0
d	g, 1	a, 0
e	d, 0	c, 0
f	f, 1	b, 1
g	g, 0	h, 1
h	g, 1	a, 0

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2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A

1. a) Find the 10's complement of 2476. (2M)
   b) Define the essential prime implicants in a K-map method. (3M)
   c) What is a multiplexer? Write its applications. (2M)
   d) Compare PROM, PLA and PAL. (3M)
   e) Write the differences between the synchronous and asynchronous sequential circuits. (2M)
   f) Write the features of Moore machine. (2M)

PART –B

2. a) Convert the following number to Hexadecimal: (7M)
      (i) $(735.5)_8$
      (ii) $(1011011)_2$
   b) Perform the following subtraction in binary using 1's and 2's complement method: $(677)_{10} – (899)_{10}$ (7M)

3. a) Find the complement and dual of the given function: (7M)
      xy+x(wz+wz′)
   b) Simplify the following Boolean function using tabular method: (7M)
      F(A, B, C, D)=Σ(2, 4, 6, 10, 12); d(A, B, C, D)=Σ(0, 8, 9, 13)

4. a) Realize 4:16 decoder using 2:4 decoders. (7M)
   b) Implement the following Boolean function with 4X1 multiplexer and external gates. Connect inputs B and C to the selection lines. (7M)
      F(A, B, C, D)=Σ(1, 2, 4, 7, 8, 9, 10, 11, 13, 15)

5. a) Draw the internal structure of 8X1 PROM and explain its operation. (7M)
   b) Give the realization of the following Boolean functions using PLA with 5 inputs, 4 outputs and 8 and gates. (7M)
      F1= Σ(0, 1, 2, 3, 11, 11, 13, 14, 15, 16, 17, 18, 19, 27, 28, 29, 30, 31)
      F2= Σ (4, 5, 6, 7, 8, 9, 10, 11, 20, 21, 22, 23, 30)

6. a) Convert the JK flip into T flip-flop. (5M)
   b) Design a Mod-12 counter using D flip-flops. (9M)
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7. a) Design a synchronous sequential circuit which goes through the following states: 1, 3, 5, 3, 6, 1, 3, 5. (7M)
   b) Convert the following Mealy machine into a corresponding Moore machine. (7M)

PS	NS, Z	
	X=0	X=1
A	C, 0	B, 0
B	A, 1	D, 0
C	B, 1	A, 1
D	D, 1	C, 0

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Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A

1. a) What are the universal gates? Why they are called as universal gates? (3M)
   b) Find the complement of the function: $A'B(C+D)+B'C'D+AB'C$. (3M)
   c) Write the truth table of a full subtractor. (2M)
   d) Write the merits and demerits of PLA. (2M)
   e) Write the differences between the Combinational and sequential circuits. (2M)
   f) What is a state table? Describe with an example. (2M)

PART –B

2. a) Convert the following numbers to Binary: (7M)
   (i) $(27.315)_{10}$
   (ii) $(68BE)_{16}$
   b) Reduce the following Boolean function to four literals and draw the logic diagram: $(A'+C)(A'+C')(A+B+C'D)$ (7M)

3. a) Implement the following Boolean function with only two input NAND gates: $F=(AB'+D')E+C(A'+B')$ (7M)
   b) Simplify the following Boolean function with the don't conditions *d* using K-map method: (7M)
   F(A, B, C, D)=Σ(1,3,8,10,15); d(A, B, C, D)=Σ(0, 2, 9)

4. a) Design an excess-3 adder circuit and explain its operation. (7M)
   b) Implement the following Boolean function with 8X1 multiplexer and external gates: (7M)
   F(A, B, C, D)=Σ(1, 3, 4, 11, 12, 13, 14, 15)

5. a) Design a 3-bit binary to Excess-3 code converter using a PROM. (7M)
   b) Implement the following Boolean functions using PLA. (7M)
   (i)F1= Σ(0, 1, 2, 4)
   (ii)F2= Σ(0, 5, 6, 7)

6. a) What is the drawback of JK flip-flop? How is it eliminated in Master Slave flip-flop? Explain. (7M)
   b) Design a decade counter using T flip-flops. (7M)
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7. a) Obtain the state table and state diagram for a sequence detector to recognize the occurrence of sequence bits 110 & 001. (7M)

   b) Find the equivalence partition and reduced table for the given state machine. (7M)

PS	**NS, O/P**	
	X= 0	**X=1**
A	B, 0	E, 0
B	E, 0	D, 0
C	D, 1	A, 0
D	B, 1	E, 0
E	C, 0	D, 0

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Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A

1. a) Find the 2'c complement of the decimal number 97. (2M)
   b) What are the prime implicants in a K-map method? (2M)
   c) What is a decoder? Write its applications. (2M)
   d) Write the merits and demerits of PAL. (2M)
   e) What are registers? Write their applications. (3M)
   f) Write the features of Mealy machine. (3M)

PART –B

2. a) Convert the following numbers to Octal: (7M)
      (i) $(1010.1010)_2$
      (ii) $(FAFA)_{16}$
   b) Reduce the following Boolean function to three literals and draw the logic diagram: $(x'y'+z)'+z+xy+wz$ (7M)

3. a) Find the dual and complement of the following function: (7M)
      $A'BD'+B'(C'+D')+A'C'$
   b) Simplify the following Boolean function using tabular method: (7M)
      F(A, B, C, D)=Σ(0, 6, 8, 13, 14); d(A, B, C, D)=Σ(2, 4,10)

4. a) Design a BCD adder circuit and explain its operation. (7M)
   b) Implement the following Boolean function with 4X1 multiplexer and external gates: (7M)
      F(A, B, C, D)=Σ(1, 3, 4, 11, 12, 13, 14, 15)

5. a) Realize the following Boolean functions using a PROM (7M)
      (i) F1= Σ(0, 4, 7)
      (ii) F2= Σ(1, 3, 6)
      (iii) F3= Σ(1, 3, 4, 6)
   b) Design a BCD to Excess-3 code converter using a PAL. (7M)

6. a) Convert JK flip-flop into D flip-flop. (7M)
   b) Design a modulo-10 ripple counter using RS flip-flops. (7M)
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7. a) Design a sequence detector that detects the overlapping sequence of 011010 using T flip-flops. (5M)
   b) Draw the diagram of Mealy type state machine for serial adder and explain its operation. (9M)