Code No: **RT42044B** **R13** **Set No. 1**

IV B.Tech II Semester Supplementary Examinations, July/August- 2017

SYSTEM ON CHIP

(Common to Electronics & Communication Engineering and Electronics & Instumentation Engineering)

Time: 3 hours **Max. Marks: 70**

Question paper consists of Part-A and Part-B
Answer ALL sub questions from Part-A
Answer any THREE questions from Part-B
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PART–A *(22 Marks)*

1. a) List and explain the components of the system? [4]
   b) List different types of processor by mentioning its architecture/implementation approach? [4]
   c) Explain process level addressing? [4]
   d) What is the purpose of address and data lines related to bus terminology? [4]
   e) What is meant by reconfiguration? [3]
   f) Define Interconnection? [3]

PART–B *(3x16 = 48 Marks)*

2. a) Describe the technology comparison between programmability and performance for general purpose processors? [8]
   b) Draw and explain the system-on-chip design flow diagram? [8]

3. a) Explain about the array processor model? [8]
   b) Explain about the pipelined processor model? [8]

4. a) With a neat diagram explain set associate cache and fully associative cache? [8]
   b) Explain the following SoC External Memory: (i) Flash (ii) placement. [8]

5. a) Differentiate between non-pipelined and pipelined bus data transfer modes with neat waveforms? [8]
   b) Explain the basic bus physical structure? [8]

6. a) How Effectiveness of a customization is to be estimated? [8]
   b) Discuss how custom Instructions are automatically identified? [8]

7. With respect to application Study explain the 3-D Graphics Processors? [16]