

Code No: R32045

R10

Set No. 1

III B.Tech II Semester Regular/Supplementary Examinations, April – 2017

VLSI DESIGN

(Common to Electronics and Communications Engineering, Electronics and Instrumentation Engineering & Electronics and Computer Engineering)

Time: 3 hours**Max. Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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|---|---|------|
| 1 | a) With neat sketches explain CMOS fabrication using p-well process? | [8M] |
| | b) List out the differences between CMOS and bipolar technologies. | [7M] |
| 2 | a) Explain latch up in CMOS circuits with neat sketches? | [7M] |
| | b) What are the alternate forms of pull up? Explain each. | [8M] |
| 3 | a) Explain with suitable examples how to design the layout of gate to maximize performance and minimize area. | [8M] |
| | b) Draw the stick and layout diagrams of CMOS inverter. | [7M] |
| 4 | a) Explain about the concepts of Sheet Resistance. | [7M] |
| | b) Describe three sources of wiring capacitances. Explain the effect of wiring capacitances on the performance of a VLSI circuit. | [8M] |
| 5 | a) Why scaling is required? Write the scaling factors for different types of device parameters? | [7M] |
| | b) Discuss the limits due to current density and logic levels. | [8M] |
| 6 | a) With a neat sketch explain the architecture of PLA? | [8M] |
| | b) Explain AND/NOR representation of PLA? | [7M] |
| 7 | a) Describe briefly the history of VHDL and state the requirements of VHDL? | [8M] |
| | b) What are sequential statements? Explain with example. | [7M] |
| 8 | a) With suitable diagram explain the simulation process. | [7M] |
| | b) Write a short note on constraints and technology libraries. | [8M] |
