Code No: **R32045** **R10** **Set No. 1**

III B.Tech II Semester Supplementary Examinations, November - 2017

VLSI DESIGN

(Common to Electronics and Communications Engineering, Electronics and Instrumentation Engineering, Electronics and Computer Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks
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1	a)	Explain in detail the n-well process for CMOS fabrication indicating the masks used.	[8M]
	b)	What is Moore's law? Explain its relevance with respect to evolution of technology.	[7M]
2	a)	With neat sketch explain the operation of BiCMOS inverter. Clearly specify its characteristics.	[10M]
	b)	Explain the functioning of MOS pass transistor.	[5M]
3	a)	Draw a stick diagram and layout for two input CMOS NAND gate indicating all the regions and layers.	[8M]
	b)	With neat sketches explain MOS layers.	[7M]
4	a)	Calculate the gate capacitance value of 5mm technology minimum size transistor with gate to channel value is $4x10^{-4}$ pF/mm^2.	[7M]
	b)	Explain about the constraints in choice of layers.	[8M]
5	a)	With EX-OR gate as an example explain about static, dynamic and domino logics.	[8M]
	b)	List out and explain the scaling factors for the different device parameters in terms of different scaling models?	[7M]
6	a)	With the help of a block diagram explain the principle and operation of standard cells.	[7M]
	b)	What is CPLD? Draw its basic structure and give its applications.	[8M]
7	a)	Briefly discuss about the different elements of VHDL?	[8M]
	b)	Explain different libraries in VHDL.	[7M]
8	a)	With suitable diagram explain about Synthesis Process in VHDL modeling.	[7M]
	b)	Explain the various static timing formats for design representation in VHDL.	[8M]

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