Code No: **RT41041** **R13** **Set No. 1**

IV B.Tech I Semester Supplementary Examinations, March - 2017

VLSI DESIGN

(Common to Electronics & Communication Engineering, and Electronics & Instumentation Engineering)

Time: 3 hours **Max. Marks: 70**

Question paper consists of Part-A and Part-B

Answer ALL sub questions from Part-A

Answer any THREE questions from Part-B

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PART–A ***(22 Marks)***

1. a) Write down the equations for I_{ds} of an n-channel enhancement MOSFET operating in Non-saturated region and saturated region? [4]
   b) Define stick diagram and layout diagram? [4]
   c) Explain about the constraints in choice of layers. [4]
   d) Draw the basic structure of a dynamic CMOS gate? [4]
   e) List out the back-end steps in ASIC design flow? [3]
   f) List out the front-end steps in FPGA design flow? [3]

PART–B ***(3x16 = 48 Marks)***

2. a) Explain the nMOS enhancement mode fabrication process for different conditions of V_{ds}? [8]
   b) Derive an equation for transconductance of an n-channel enhancement MOSFET operating in active region. [8]

3. a) Design a stick diagram and layout for two input CMOS NAND gate indicating all the regions and layers. [8]
   b) Explain 2µm Double Metal, Double Poly. CMOS / BiCMOS Rules. [8]

4. a) What are the issues involved in driving large capacitor loads in VLSI circuit regions? Explain. [8]
   b) Calculate the gate capacitance value of 5mm technology minimum size transistor with gate to channel value is $4x10^{-4}$ pF/mm^2. [8]

5. a) How switch logic can be implemented using Pass Transistors? Explain. [8]
   b) Draw the transistor circuit diagram of shift register capable of holding and shifting 4-bit word. Explain the circuit operation. [8]

6. a) What are FPGAs? Explain the principle and operation. [8]
   b) Explain how the pass transistors are used to connect wire segments for the purpose of FPGA programming. [8]

7. a) Clearly explain each step of high level design flow of an ASIC. [8]
   b) Write a short note on mixed signal design? [8]