

Code No: RT41041

R13**Set No. 1****IV B.Tech I Semester Regular/Supplementary Examinations, October/November - 2017****VLSI DESIGN****(Common to Electronics and Communication Engineering and Electronics and Instrumentation Engineering)****Time: 3 hours****Max. Marks: 70***Question paper consists of Part-A and Part-B**Answer ALL sub questions from Part-A**Answer any THREE questions from Part-B************PART-A (22 Marks)**

1. a) Clearly explain about ION-IMPLANTATION step in IC fabrication. [4]
- b) Why is VLSI design process presented in NMOS only? Justify with an example? [4]
- c) Explain the formal estimation of CMOS Inverter delay. [4]
- d) Write a short note on clocked sequential circuits. [3]
- e) Write a short note on clock mechanisms in VLSI design. [4]
- f) List out the applications of FPGAs. [3]

PART-B (3x16 = 48 Marks)

2. a) Compare CMOS and Bipolar technologies. [8]
- b) Explain the NMOS fabrication procedure. [8]
3. a) Illustrate the lambda-based design rules with neat sketches. [8]
- b) Design an area efficient layout diagram for the CMOS logic shown below
 $Y = (A + B + C)$. [8]
4. a) What is meant by sheet resistance R_s ? Explain the concept of R_s applied to MOS transistors. [8]
- b) Calculate on resistance of an inverter from VDD to GND. If n- channel sheet resistance $R_{sn}=10^4\Omega$ per square and P-channel sheet resistance $R_{sp} = 3.5 \times 10^4\Omega$ per square. ($Z_{pu}=4:4$ and $Z_{pd}=2:2$). [8]
5. a) Give the subsystem design considerations of a four-bit adder. [8]
- b) Explain step-by-step subsystem design approach. Consider an example. [8]
6. a) Explain the terms (i) Static power dissipation (ii) Dynamic power dissipation. [8]
- b) Discuss the VLSI design issues and design trends. [8]
7. a) Write about FPGA Programming Technologies in detail. [8]
- b) Explain the step by step approach of FPGA design process on Xilinx environment. [8]

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R13**Set No. 2****IV B.Tech I Semester Regular/Supplementary Examinations, October/November - 2017****VLSI DESIGN****(Common to Electronics and Communication Engineering and Electronics and Instrumentation Engineering)****Time: 3 hours****Max. Marks: 70***Question paper consists of Part-A and Part-B**Answer ALL sub questions from Part-A**Answer any THREE questions from Part-B************PART-A (22 Marks)**

1. a) Define threshold voltage of a MOS device and explain its significance. [4]
- b) Discuss different forms of pull up, mentioning merits and demerits of each form. [4]
- c) What is meant by standard unit of capacitance? Give some area capacitance calculations. [4]
- d) Draw and explain fan-in and fan-out characteristics of different CMOS design Technologies. [4]
- e) Give two reasons about the importance of package selection in VLSI design. [3]
- f) Write a short notes on FPGA configuration and configuration modes. [3]

PART-B (3x16 = 48 Marks)

2. a) Derive an equation for I_{DS} of an n-channel Enhancement MOSFET operating in Saturation region. [8]
- b) An nMOS transistor is operating in saturation region with the following parameters. $V_{GS} = 5V$; $V_{tn} = 1.2V$; $W/L = 110$; $\mu_n C_{ox} = 110 \mu A/V^2$. Find Transconductance of the device. [8]
3. a) Write a short note on “2 μm Double Metal, Double Poly, CMOS/BiCMOS rules”. [8]
- b) Draw the circuit diagrams and the corresponding stick diagrams for nMOS and CMOS inverters. [8]
4. a) What are the alternate gate circuits are available? Explain any one of item with suitable sketch. [8]
- b) Implement the realization of gates using NMOS and PMOS. [8]
5. a) Describe the nature of a parity generator and explain its structured design approach. [8]
- b) Draw and give the design approach for a carry look ahead adder with its structure. [8]
6. a) Write and explain about the sources of power dissipation in VLSI Design. [8]
- b) Explain in detail about ASIC design flow with neat sketch. [8]
7. a) Draw and explain the routing architecture of field programmable gate arrays. [8]
- b) Write about the shift register design and implementation onto FPGA. [8]

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R13**Set No. 3****IV B.Tech I Semester Regular/Supplementary Examinations, October/November - 2017****VLSI DESIGN****(Common to Electronics and Communication Engineering and Electronics and Instrumentation Engineering)****Time: 3 hours****Max. Marks: 70***Question paper consists of Part-A and Part-B**Answer ALL sub questions from Part-A**Answer any THREE questions from Part-B************PART-A (22 Marks)**

1. a) With neat sketch, explain drain characteristics of an n-channel enhancement MOSFET. [4]
- b) Compare and contrast the Lambda based and Micron based Rules for layout design. [4]
- c) Draw and explain the schematic of Pseudo-nMOS Inverter. [3]
- d) Explain the concept of driving large capacitive loads with, relevant examples. [4]
- e) List out the back-end steps in ASIC design flow. [3]
- f) Write about Programmable I/O blocks in FPGAs. [4]

PART-B (3x16 = 48 Marks)

2. a) With neat sketch explain BICMOS fabrication in an n-well process. [8]
- b) Explain the term "aspects of MOSFET" in VLSI Design. [8]
3. a) Tabulate the encoding scheme for a simple single metal CMOS/Bi-CMOS process with respect to various MOS layers. [8]
- b) Draw the symbolic layout for the CMOS inverter and write the general CMOS logic gate layout guidelines. [8]
4. a) Discuss the inverter delay and propagation delay. [8]
- b) Write about the scaling limitations due to sub Supply voltages in MOSFETS. [8]
5. a) Explain the architectural issues of subsystem design. [8]
- b) Explain the structural design approach with an example. [8]
6. a) What is the need of testability? Explain design for testability. [8]
- b) Explain about SoC design. [8]
7. a) Describe the shift register implementation using VHDL. [8]
- b) Explain about different programmable elements in FPGA architectures. [8]

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R13**Set No. 4****IV B.Tech I Semester Regular/Supplementary Examinations, October/November - 2017**
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1. a) Explain various regions of CMOS inverter transfer characteristics. [3]
- b) Write a short note MOS layers and symbolic diagram translation to MASK form. [4]
- c) Define and give the expressions for any four scaling factors of MOS device parameters. [4]
- d) Write about general considerations in subsystem design processes. [4]
- e) Write about technology options in VLSI design. [3]
- f) Explain the need for FPGA and its applications. [4]

PART-B (3x16 = 48 Marks)

2. a) Explain different forms of pull-ups used as load in CMOS enhancement. [8]
- b) Determine pull-up to pull-down ratio of an NMOS inverter when driven through one or more pass transistors. [8]
3. a) Tabulate the encoding scheme for a simple single metal nMOS process with respect to various MOS layers. [8]
- b) What is stick diagram and explain about different symbols used for components in Stick diagram. Draw the stick and layout for a two input CMOS NAND gate. [8]
4. a) Describe three sources of wiring capacitances. Explain the effect of wiring capacitance on the performance of a VLSI circuit. [8]
- b) Write about the scaling limitations due to sub threshold currents in MOSFETS. [8]
5. Realize the 2-i/p NAND gate using NMOS, PMOS and CMOS technologies. [16]
6. a) Discuss the design flow of system on chip design with neat sketch. [8]
- b) Explain the steps of specification and logic design in ASIC design flow. [8]
7. a) Write the steps involved to prototype the HDL code onto FPGA device. [10]
- b) List out the salient features of Xilinx 3000 CLB. [6]