Code No: R22054 **R10** SET - 1

**II B. Tech II Semester Supplementary Examinations January – 2014**
**COMPUTER ORGANIZATION**
(Com. to CSE, ECC)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
~~~~~~~~~~~~~~~~~~~~~~~~~

1. a) Describe the interconnection structure of a computer?
   b) Explain format of assembly language?

2. Explain about CPU organization?

3. Write short notes on the following:
   a) Register transfer language
   b) Instruction formats
   c) Addressing modes
   d) Reduced Instruction Set Computer

4. Explain the Hardwired control and Micro programmed control. Also explain their advantages and disadvantages?

5. a) Explain Booth's algorithm from its theoretical basis?
   b) Multiply $11101_2$ with $10101_2$ using Booth's algorithm.

6. a) Discuss about address translation in paging.
   b) How does page size effects storage utilization and effective memory data transfer rate?

7. Explain the following:
   a) Asynchronous Serial Transfer
   b) Asynchronous Communication Interface.

8. a) What is meant by instruction pipeline? Explain.
   b) Explain the following with related to the instruction pipeline
      i) Pre-fetch target instruction
      ii) Branch target buffer
~~~~~~~~~~~~~~~~~~~~~~~~~

Code No: R22054 **R10** SET - 2

**II B. Tech II Semester Supplementary Examinations January – 2014**
**COMPUTER ORGANIZATION**
(Com. to CSE, ECC)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
~~~~~~~~~~~~~~~~~~~~~~~~

1. a) Explain about instruction set architecture design?
   b) Explain about instruction format?

2. Explain about memory sub-system organization?

3. a) Explain about hardware description language?
   b) Explain about Micro operations?

4. a) Explain why hardwired control unit is faster than micro programmed control unit.
   b) What is microinstruction? How do we reduce number of microinstructions?

5. a) Find the output binary number after performing the arithmetic operation using 1's complement representation.
      i) $111.01_2 + 10.111_2$
      ii) $110.11_2 - 111.01_2$
   b) Explain steps involved in the addition of numbers using 2's complement notation?

6. a) Explain how the Bit Cells are organized in a Memory Chip.
   b) Explain the organization of a 1K x 1 Memory with a neat sketch.

7. a) Explain programmed I/O in detail.
   b) Explain interrupt initiated I/O in detail.

8. a) List and explain different interconnection structures used in multiprocessors?
   b) Explain system bus structure for multiprocessors with a neat sketch.
~~~~~~~~~~~~~~~~~~~~~~~~

Code No: R22054 **R10** SET - 3

**II B. Tech II Semester Supplementary Examinations January – 2014**
**COMPUTER ORGANIZATION**
(Com. to CSE, ECC)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
~~~~~~~~~~~~~~~~~~~~~~~~

1. a) Explain 8085 microprocessor instruction set architecture?
   b) Explain about addressing modes?

2. Explain about I/O sub-system organization and interfacing?

3. a) What are micro operations? Explain
   b) Explain the instructions used in Register Transfer Language?

4. a) Compare the hardwired control with micro programmed control in terms of complexity of the instruction set, ease of modification and clock speed.
   b) Explain about micro sequence control unit design?

5. a) Find the output binary number after performing the following arithmetic operations
      i) $111.01_2 + 10.111_2$
      ii) $11.01_2 + 110.11_2$
      iii) $110.11_2 - 111.01_2$
   b) Explain about specialized arithmetic hardware?

6. a) Differentiate between single versus two-level caches.
   b) Elaborate on Pentium Cache Organization.

7. a) What is Direct Memory Access? Explain the working of DMA.
   b) Discuss about I/O channel architecture.

8. a) Explain communication in multi processor systems?
   b) What is cache coherence? Explain its importance.
~~~~~~~~~~~~~~~~~~~~~~~~

Code No: R22054 **R10** SET - 4

**II B. Tech II Semester Supplementary Examinations January – 2014**
**COMPUTER ORGANIZATION**
(Com. to CSE, ECC)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
~~~~~~~~~~~~~~~~~~~~~~~~

1. a) What are the levels of programming language? Explain.
   b) What is instruction set? Explain with an example?

2. a) Explain about memory interfacing?
   b) Explain about I/O interfacing?

3. a) Explain about Register Transfer Language?
   b) Explain about programming through VHDL with a sample program?

4. a) Give the typical horizontal and vertical microinstruction formats.
   b) Describe how microinstructions are arranged in control memory and how they are interpreted.

5. a) How subtraction is done on the binary numbers represented in one's complement notation give an examples?
   b) What do you mean by r's complement?

6. a) Compare and contrast asynchronous DRAM and synchronous DRAM.
   b) Compare and contrast direct and associative mapping techniques.

7. a) How would CPU handles multiple devices. Explain with different techniques available?
   b) Discuss the characteristics of Intel 8259A interrupt controller.

8. a) Explain RISC pipeline?
   b) Explain different types of parallel processors?
~~~~~~~~~~~~~~~~~~~~~~~~