Code No: R22023 **R10** SET - 1

II B. Tech II Semester Supplementary Examinations, January - 2014
SWITCHING THEORY AND LOGIC DESIGN
(Com. to EEE, ECE, ECC, BME, EIE)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Using 9's complement, perform the following decimal arithmetic. Also justify answers with 10's Complement i) 3765 – 4249 ii) – 255 – 106
   b) What is meant by BCD? Obtain binary codes for decimal digits in BCD and 2421codes? (10M+5M)

2. a) Algebraically prove the following equations, identify the postulates or theorems of Boolean algebra used?
   i) $ab + a'b = b$ ii) $a' + ab + a' + b$ iii) $ab + a'c + bc = ab + a'c$ iv) $(ab)' = a' + b'$
   b) Discuss the importances of grey code? Explain how a four bit grey code is obtained? (8M+7M)

3. a) Use K – map to find the minimal SOP expression for the following functions.
   i) $f(w, x, y, z) = \prod m(3, 4, 5, 8, 10, 11, 12)$
   ii) $f(a, b, c, d) = \sum m(2, 3, 6, 9, 12, 13, 14) + d\ (0,11)$
   b) What do you understand by minimal *SOP* and canonical *SOP*? (10M+5M)

4. a) Explain the operation of half subtractor? Realize full subtractor using logic gates.
   b) Design a circuit that takes two 4- bit BCD numbers as inputs and produce its sum.(7M+8M)

5. a) What is meant by n – channel multiplexer? Draw the logic diagram of 16 × 1 MUX with the help of 3 to 8 line decoder and explain its operation?
   b) Realize the following logic function using 4 to 16 decoder and logic gates
   $f(w, x, y, z) = wx'y'z + wx'yz' + wy'$ (10M+5M)
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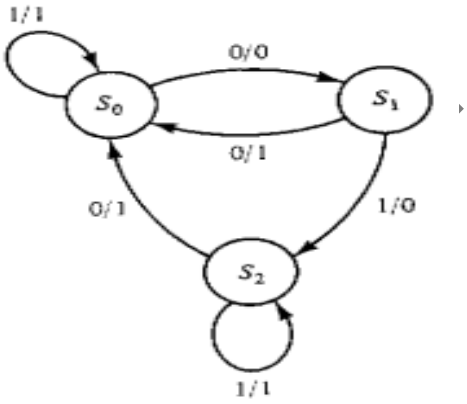
6. a) Discuss the functionality of PAL. How its programming table is prepared?
   b) Design a combinational logic circuit using ROM. The circuit accepts BCD number and generates an output binary number equal to the 2's complement of the input number.

(7M+8M)

7. a) Explain the operation of NAND latch. How the JK flip flop is derived from this latch?
   b) What is meant by ring counter? Design four bit ring counter and explain its operation.

(8M+7M)

8. Design a circuit using D flip flop that implements the machine whose state diagram is given below. (15M)



Code No: R22023 **R10** SET - 2

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1. a) Describe how signed number is represented in two's complement form.
   b) Encode the following numbers in BCD and excess – 3. (5M+10M)
   i) $(2A5)_{16}$ ii) $(325)_5$ iii) $(67)_8$

2. a) Write the dual of the following expressions and simplify them:
   i) $a'b + c'(d + e)$ ii) $(a + b)(a' + cd)$ iii) $(a' + b')(c + d')(b + c'd)$
   b) Briefly describe about error detecting and error correcting codes with suitable examples (8M+7M)

3. a) Use K – map to find the minimal SOP expression for the following functions.
   i) $f(w, x, y, z) = \prod m(0, 1, 3, 9, 10, 13) + d(7, 8, 11, 14)$
   ii) $f(a, b, c, d) = \sum m(0, 1, 3, 5, 7, 10, 12)$
   b) What do you understand by minimal *POS* and canonical *POS*? (10M+5M)

4. a) Obtain the truth tables for logic expressions of full adder and full subtractor?
   b) Discuss how four bit excess – 3 adder circuit is designed. Explain its operation. (7M+8M)

5. a) What is decoder? Draw the logic diagram of 3 to 8 line decoder and explain its operation.
   b) Implement the following function with 8 to 1 line multiplexer:
   $f(w, x, y, z) = wx'y'z + wx'yz' + wy'$ (8M+7M)

6. a) Discuss the functionality of PLA. How its programming table is prepared?
   b) Design a combinational logic circuit using ROM, the circuit accepts BCD number and generates an output binary number equal to the 1's complement of the input number. (7M+8M)

7. a) How do you convert each of the following flips flop into alternate flip flop?
   i) D to T ii) T to J-K
   b) How do you design universal shift register? Draw the logic diagram with flip flops. (7M+8M)

8. Construct Moore machine whose output is 1 if the last five inputs were 11010 using JK flip flops. (15M)
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Time: 3 hours Max. Marks: 75

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1. a) Perform the following:
   i) $(137.64)_{10} = (\ )_5 = (\ )_2$ ii) $(1111.1011)_2 = (\ )_8 = (\ )_{16}$
   b) What is meant by excess – 3 code? Obtain binary codes for decimal digits in excess – 3 and 2421 codes? (10M+5M)

2. a) Convert each of the following expressions to extended sum of products (SOP) form
   i) $(a+b')(a+b'+c)$ ii) $(b'c+d')\,a+a'\,b'(c'+d)$
   b) Implement the following functions with NAND and NOR gates
   i) $f(a,b,c,d)=a+b'(c+a'\,d)$ ii) $f(a,b,c,d)=ab'c'\,d+a'(bcd'+b'c')$ (7M+8M)

3. a) Explain how K – map is useful for simplifying Boolean functions. Use K – map to find the minimal SOP expression for the following function:
   $f(w,x,y,z)=w'\,y'+w'\,yz'+wxy+xyz'$
   b) Let us assume BCD code logic functions as $f(a,b,c,d)$ and an excess – 3 code logic functions as $f(w,x,y,z)$, knowing the $f(a,b,c,d)$ write $f(w,x,y,z)$. Also obtain simplified *SOP* expression for x? (7M+8M)

4. a) Explain the functionality of full adder. Design and explain operation of 4 bit binary adder.
   b) How full adder carries are calculated ahead? Discuss the design of carry look ahead adder. (8M+7M)

5. a) Discuss the operation of priority encoder with the help of logic diagram and truth table?
   b) Implement the full adder sum and carry functions with decoder and multiplexers. (7M+8M)

6. a) Discuss the structure of PROM with the help of schematic diagram? How it is programmed to store a logic function?
   b) Design a combinational logic circuit using PLA, the circuit accepts BCD number and generates an output binary number equal to the 1's complement of the input number. (7M+8M)

7. a) Draw the logic diagram of RS flip flop using NAND latch and explain its operation.
   b) Design 4 input Johnson counter, draw its logic diagram using flip flops and explain its operation. (7M+8M)

8. Construct Moore machine whose output is 1 if the last five inputs were 11010 using JK flip flops? (15M)
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1. a) Perform the following:

   $(i)\ (1523)_6 = (\ )_{12}$ $(ii)\ (1101.11)_2 = (\ )_{10}$

   b) Discuss how the binary codes are obtained in weighted form? Encode decimal digits in

   2 4 2 1, 7 3 2 -1 and 8 4 -2 -1 (5M+10M)

2. a) Simplify the following expressions in to minimal SOP form

   i) $(a' + b)(a + c)(a + c')$ ii) $a'd'e + b\,d'e + a\,b'c\,d + b'd'e + a\,b'c\,e'$

   iii) $(b' + c)(a + d)(b + c + d)$

   b) Use NAND gates and implement $f(a, b, c) = a\,b' + a'bc'$ (12M+3M)

3. a) Explain how K – map is useful for simplifying Boolean functions? Use K – map to find the minimal SOP expression for the following function?

   $f(w, x, y, z) = \sum m\,(0,4,6,7,12,13,14,15)$

   b) Let us assume BCD code logic functions as *f(a,b,c,d)* and grey code logic functions as *f(w,x,y,z)*, knowing the *f(a,b,c,d)* write *f(w,x,y,z)*? Also obtain simplified SOP expression for *w*? (7M+8M)

4. a) Construct full adder using half adders? Realize full adder using minimum number of NAND gates?

   b) Draw the functional diagram of adder–subtractor circuit and explain its operation? (7M+8M)
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5. a) Draw the logic diagram of Demultiplexer? Differentiate the functionalities of multiplexer and Demultiplexer?

   b) Realize the following logic functions with decoder (7M+8M)

   i) $F_1(w, x, y, z) = \sum m(0,2,3,4,5,6,11,12,13,14,15)$ ii) $F_2(w, x, y, z) = \sum m(1,2,3,5,7,9)$

6. a) What are the capabilities of programmable logic devices? How the sizes are defined for PROM, PLA and PAL?

   b) Design a combinational logic circuit using PAL, the circuit accepts BCD number and generates an output binary number equal to the 2's complement of the input number. (7M+8M)

7. a) Explain the operation of NOR RS latch? How RS flip flop is derived from this latch?

   b) Design bidirectional shift register, draw its logic diagram and explain its operation. (7M+8M)

8. Design a circuit using D flip flop that implements the machine whose state diagram is given below. (15M)