Code No: RT22023 **R13** SET - 1

II B. Tech II Semester Regular Examinations, April/May – 2016
PULSE AND DIGITAL CIRCUITS
(Com. to EEE, ECC)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1. a) What is meant by synchronization? (4M)
   b) Differentiate between sampling and logic gates. (4M)
   c) Draw the ringing circuit and derive its transfer function. (4M)
   d) What are various configurations of a clipping circuit. (4M)
   e) Why clamping circuit is called as DC restorer. (3M)
   f) What is hysteresis? (3M)

PART -B

2. a) Derive expression for rise time and percent tilt of a RC high pass circuit when square as input? (8M)
   b) A symmetrical square wave whose peak to peak amplitude is 1V and whose average value is zero is applied to an RC integrating circuit. The time constant is equal to time period of the square wave form. Find the peak to peak value of the output wave form. (8M)

3. a) With neat diagram and derivation explain the working of a clipping circuit at two independent levels. (8M)
   b) Design a diode clamper circuit to clamp the positive peaks of the input signal at zero level. The frequency of the input voltage is 1000 Hz. (8M)

4. a) What is a Bistable Multivibrator.? Explain the operation of any one of the Bistable Multivibrators. (8M)
   b) Design a Bistable Multivibrator if $V_{CC}=V_{BB}$ =11V. The DC current gain of each Transistor is30. (8M)

5. a) Explain the working of AND gate with diode. (8M)
   b) Explain the working of NOR gate using DTL Logic. (8M)

6. a) Design a bootstrap sweep generator given V_{CC}=15V, I_{Csat}=6mA and h_{femin}=30 (8M)
   b) Explain the working of a UJT based time base generator. (8M)

7. a) Draw and explain the operation of a four diode sampling gate. (8M)
   b) With the help of a circuit diagram and waveform explain frequency division by an astable blocking oscillator. (8M)
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Code No: RT22023 **R13** SET - 2

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2. Answer **ALL** the question in **Part-A**
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PART –A

1. a) What is an attenuator? (4M)
   b) Explain the operation of a diode clipper. (4M)
   c) What is the importance of commutating capacitors? (4M)
   d) Explain the working of miller sweep circuit. (4M)
   e) Explain what a pedestal gate circuit is. (3M)
   f) What is fan-in & fan-out? (3M)

PART -B

2. a) Find the expression for output voltage when a ramp signal is applied to a RC Low Pass filter circuit. (8M)
   b) A 10Hz Square wave is applied to an amplifier. Calculate and plot the output wave form under the following conditions. The Lower 3dB frequency is a) 0.5Hz b) 5Hz and c) 50Hz. (8M)

3. a) What is clamping circuit theorem? Derive an expression. (8M)
   b) Draw and explain the working of a diode comparator. (8M)

4. a) Draw the circuit of a self-biased binary and explain its operation (8M)
   b) Design a Flip-Flop with the following specifications, $V_{CC}=V_{BB}=12V$, $I_{C(sat)}$ =10mA, $h_{FE(min)}$=25. Maximum Trigger frequency = 20KHz. (8M)

5. a) Explain the operation of OR gate using diode logic. (8M)
   b) Explain the circuit of NAND gate using TTL logic. (8M)

6. a) Define and derive expressions for displacement error, slope error and transmission errors. (8M)
   b) With neat diagram and waveforms explain the working principle of a transistor current sweep circuit. (8M)

7. Write short notes on.
   a) Unidirectional diode gate (6M)
   b) Sweep circuit Frequency division (6M)
   c) Bidirectional sampling gate using transistor. (4M)
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Code No: RT22023 **R13** SET - 3

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2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1. a) Explain any one application of a CRO (4M)
   b) Explain about regenerative and non-regenerative comparators. (4M)
   c) Explain the difference between one-way and two-way clamping circuits. (4M)
   d) Explain a triggering mechanism of a monostable multivibartor (4M)
   e) What is positive logic? (3M)
   f) Explain how linearly varying current waveforms are generated? (3M)

PART -B

2. a) A Pulse of 6V amplitude and 0.8ms duration is applied to an RC High pass circuit with R=10K Ohm and C=0.47 Micro farad. Determine the Percent Tilt in the output. (8M)
   b) Explain the operation of a Compensate attenuator (8M)

3. a) With the help of a neat diagram explain the working of a emitter coupled clipper circuit. (8M)
   b) A 200V peak square wave with an average value of 0V and a period of 30ms is to be negatively clamped at 50V. Draw the circuit diagram necessary and also draw input and output waveforms. (8M)

4. a) Draw and explain the operation of collector coupled Astable multivibrator. (8M)
   b) Draw and explain the operation of a Schmitt trigger and find an expression for its UTP. (8M)

5. a) Design and Explain CMOS inverter circuit (8M)
   b) What is Emitter Coupled Logic? State its advantages compared to TTL and other logic families. (8M)

6. a) Derive the expressions for slope or sweep speed error of transistor miller time base generator (8M)
   b) Explain the operation of bootstrap sweep circuit with necessary derivations (8M)

7. Write short notes on
   a) Two diode sampling gate (8M)
   b) Frequency division with Astable. (8M)
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Code No: RT22023 **R13** SET - 4

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2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1. a) Explain diode reverse recovery time (4M)
   b) What is meant by biased clamping? (4M)
   c) What is the integrator condition? (4M)
   d) Explain triggering of binary using diode. (4M)
   e) What is synchronization on a one-to-one basis? (3M)
   f) Compare sine wave synchronization with pulse synchronization. (3M)

PART -B

2. a) Explain diode switching times and transistor switching times (8M)
   b) What is an attenuator? Explain about over compensation, perfect and under compensation circuits. (8M)

3. a) Design a diode clamper to restore a dc level of +6V to an input signal of peak value 16V. Assume the drop across the diode as 0.5V. (8M)
   b) Explain the necessity of practical Clamping circuits with necessary waveforms (8M)

4. a) Derive an expression for gate width of an emitter-coupled monostable multivibrator. (8M)
   b) Silicon npn Transistors with h_{femin}=40 are available. Design an Astable multivibrator to generate a square wave of 1KHz frequency with a duty cycle of 25%. (8M)

5. a) What are various performance factors of a digital logic family?. Define them. (8M)
   b) With an example explain about the realization of a function using AOI logic. (8M)

6. a) Draw the exponential sweep circuit and derive expression for e_t, e_d and e_s (8M)
   b) Draw and explain the operation of a Transistor boot strap sweep generator circuit and find the expressions for slope error, sweep amplitude. (8M)

7. Write short notes on
   a) Bidirectional gates using Transistors. (6M)
   b) Frequency division using sweep circuit (6M)
   c) Synchronization of sweep circuit (4M)
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