Code No: G6803/R13

M. Tech. I Semester Supplementary Examinations, December-2016

CMOS ANALOG IC DESIGN

(Common to VLSI & ES, ES & VLSI, VLSID & ES, ES & VLSID, VLSI, VLSID, VLSISD, VLSI&ME)

Time: 3 hours **Max. Marks: 60**

Answer any FIVE Questions
All Questions Carry Equal Marks

1. a Explain the Large-signal model for the MOS Transistor.
   b Discuss about the Passive Components of the MOS transistor.

2. Explain the given simplest forms of the current mirror
   a) Bipolar version of current mirror
   b) MOS version of the current mirror.

3. Explain about
   a) current amplifier
   b) cascode amplifier.

4. a Explain about the design of Two-stage op-amps.
   b Explain about the Cascode Op-amps.

5. Explain about
   a) Bipolar widlar current source
   b) Bipolar peaking current source.

6. a Explain the compensation of Op-amps.
   b Explain the Measurement technologies of Op-amp.

7. a Explain about computer simulation model.

   b Explain sub threshold MOS model.

8. a Explain the basic PLL Technology
   b Explain about charge-pump PLLs
      i. Problem of Lock Acquisition
      ii. Basic charge-pump PLL

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