Code No: I6810/R16

M. Tech. I Semester Regular Examinations, December-2016

SYSTEM ON CHIP DESIGN

Common to VLSI&ES (68), ES&VLSI (48), VLSID &ES (77), ES &VLSID (81)

Time: 3 Hours **Max. Marks: 60**

Answer any FIVE Questions
All Questions Carry Equal Marks

1. a Explain the processor architecture and its implementation with neat sketch.
   b Explain the simple sequential processor in architectural view.

2. a Explain SOC system level interconnection of bus based approach.
   b Discuss the requirements and specifications in a Design process.

3. a Discuss the interrupts and exceptions in processor architecture.
   b Explain the buffer designed for a fixed or maximum request rate.

4. a Explain vector functional units.
   b Discuss detecting instruction concurrency of superscalar processor.

5. a Discuss SOC (On-Die) memory systems.
   b Explain the Strecker- Ravi model.

6. a Explain Bus Bridge and Bus varieties Of bus architecture.
   b Discuss the AMBA SOC standard bus.

7. a Describe the Architecture of customizing instruction processor.
   b Explain reconfigurable Interconnects.

8. a Discuss the SOC design approach.
   b Discuss the application study of JPEG compression.

*****