Code No: G6802/R13

M. Tech. I Semester Supplementary Examinations, December-2016

VLSI TECHNOLOGY AND DESIGN

(Common to VLSI & ES, ES & VLSI, VLSID & ES, ES & VLSID, VLSI, VLSID, VLSISD, VLSI&ME, DS&CE, DE&CS, E&CE and DECE)

Time: 3 hours **Max. Marks: 60**

Answer any FIVE Questions
All Questions Carry Equal Marks

1. a Explain the terms SSI, LSI, VLSI and ULSI with the number of transistors per chip and applications? 6M
   b Clearly explain each step of high level design flow of an FPGA? 6M

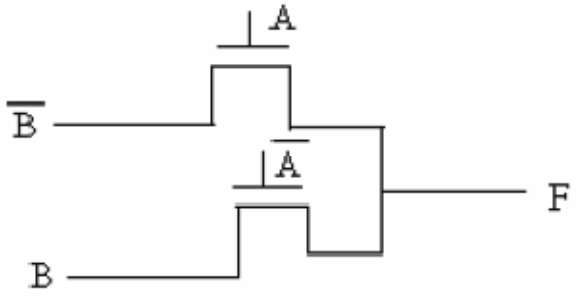
2. a Explain the process of fabrication for CMOS technology with neat diagrams. 6M
   b Compare BiCMOS technology with other Technologies. 6M

3. a Show that the pull up to pull down ratio of an nMOS inverter driven by another nMOS inverter is 4:1. 6M
   b Explain the problem of driving large capacitive loads? How such loads can be driven. 6M

4. a Discuss the limits of scaling. Why scaling is necessary for VLSI circuits? 6M
   b Explain the terms figure of merit of MOSFET and output conductance using necessary equations. 6M

5. a Explain clocked CMOS logic and domino logic with suitable example. 6M
   b Design a parity generator and explain the functioning of it with a transistor schematic and layout. 6M

6. a Consider the circuit shown in figure. 12M
   i. Determine the logic function F.
   ii. Design a circuit to implement the same logic function using NOR gates.
   iii. Draw a transistor level schematic and use CMOS technology.



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7.	a	How Architecture of chip can be tested? Give some example.	6M
	b	What is routing? Explain with some suitable example. How it is optimized?	6M
8.	a	What are the categories of Design for testability? Explain them briefly.	6M
	b	What are the λ -based design rules? Give them for each layer.	6M

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