

**Total No. of Pages : 02**

**B.Tech.(Electronics Engg.) (2012 Onwards)**

**B.Tech.(ECE/Electronics & Computer Engg./ETE) (2011 Onwards)**

**(Sem.-3)**

# DIGITAL CIRCUITS AND LOGIC DESIGN

**Subject Code : BTEC-302**

Paper ID : [A1131]

**Max. Marks : 60**

1. SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.
2. SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.
3. SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.

**Q1. Write briefly :**

- i. Perform the following subtraction using 10's complement method: 196-155.
- ii. Explain the difference between Gray code and the regular binary code.
- iii. Give one example each of an even and an odd parity generator, using suitable diagrams.
- iv. Distinguish between address and contents of a memory location.
- v. Determine the minimum conversion interval of an ADC using an 8-stage counter with a clock frequency of 2MHz.
- vi. Explain the working of a T flip-flop.
- vii. Differentiate between a fixed-point number and a floating-point number.
- viii. Describe a simple four-line multiplexer.
- ix. Draw the circuit diagram of a diode AND gate and explain its working.
- x. Convert  $(F80B)_{16}$  to binary.

**SECTION - B**

Q2. Obtain the minimal POS and SOP forms for the function given as :

$$F(A, B, C, D) = \pi(3, 4, 6, 7, 11, 12, 13, 14, 15)$$

Q3. Briefly explain the working of a 4-bit Bidirectional Universal shift register.

Q4. What is the significance of TTL? Describe the basic circuitry of a three-input TTL NAND gate.

Q5. Design a 2's complement BCD Adder/Subtractor.

Q6. Describe the Counter-ramp method of ADC.

**SECTION-C**

Q7. Design a Mod-5 Up counter, that counts in the sequence of 6-7-8-9-10-6-7-8-9-10 and so on using JK flip-flop.

Q8. i) Explain the operation of a Master-Slave JK flip-flop.

ii) Discuss Dual-slope Analog-to-Digital conversion operation.

Q9. i) Briefly describe RAM family.

ii) Explain and give a comparison of the various logic families in tabular form by defining all the parameters.