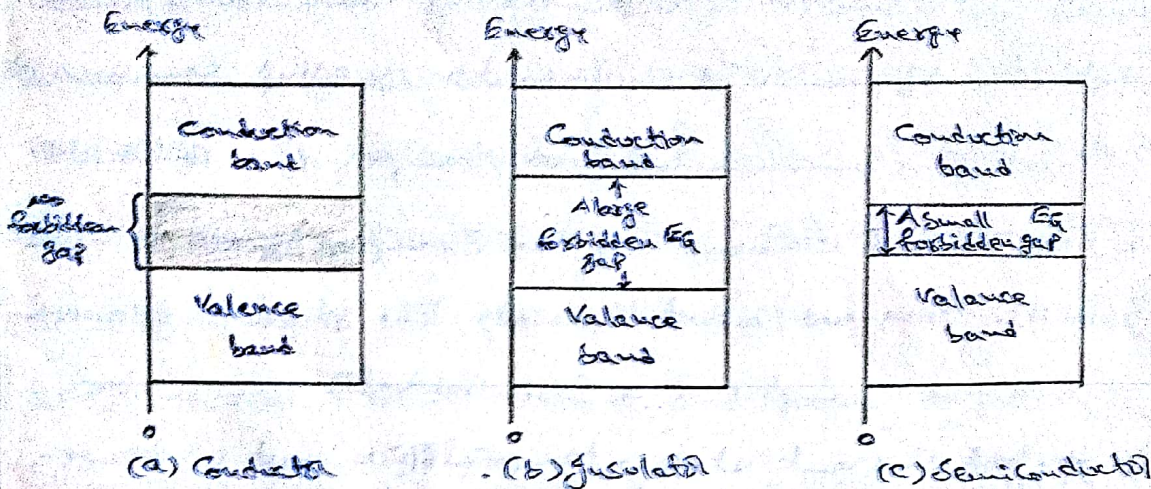


UNIT – 1

SEMI CONDUCTOR PHYSICS

Insulators, Semi-conductors & Metals classification

Using Energy Band Diagram



ENERGY BAND DIAGRAMS

Out of all the energy bands, three bands are most important to understand the behaviour of solids. These bands are,

1. Valance band
2. Conduction band
3. Forbidden band or gap

The energy band formed by due to merging of energy levels associated with the valance electrons i.e. electrons in the last shell, is called Valance band.

The energy band formed due to merging of energy levels associated with the free electrons is called Conduction band.

Under normal condition, the conduction band is empty and once energy is imparted, the valance electrons jump from valance band to conduction band and become free.

While jumping from valance band to conduction band, the electrons have to cross an energy gap.

The energy gap which is present separating the conduction band and the valance band is called forbidden band or forbidden gap.

Based on the ability of various materials to conduct current, the materials are classified as conductors, insulators and the semi-conductors.

is called conductor. A very poor conductor of electricity is termed as insulator. A metal having conductivity which is between conductor & an insulator is called semiconductor. The copper & Aluminium are good examples of a conductor. The glass, wood, diamond are the examples of an insulator which does not conduct current. The silicon & germanium are the examples of a semiconductor which does not conduct current at low temperatures but as temperature increases these materials behave as good conductors.

In the metals like copper, aluminium there is no forbidden gap between valance band & conduction band. The two bands overlap. Hence even at room temperature, a large number of electrons are available for conduction. So without any additional energy, such metals contain a large number of free electrons & hence called good conductors. An energy band diagram for a conductor is shown in the figure 1(a)

An insulator has an energy band diagram as shown in figure 1(b). In case of such insulating material, there exists a large forbidden gap in between the conduction band and the valance band. practically it is impossible for an electron to jump from the valance band to the conduction band. Hence such materials cannot conduct and are called insulators. The forbidden gap is very wide, approximately of about 7 eV is present in insulator. For a diamond, which is an insulator, the forbidden gap is about 6 eV.

The forbidden gap in such materials is very narrow as shown in figure (c). Such materials are called semiconductors. The forbidden gap is about 1 eV. In such materials, the energy provided by the heat at room temperature is sufficient to lift the electrons from the valance band to the conduction band. Therefore at room temperature, semiconductors are capable of conduction. But at 0°K or absolute zero (-273°), all the electrons of semiconductor materials find themselves locked in the valance band. Hence at 0°K , the semiconductor materials behave as perfect insulators. In case of semiconductors, forbidden gap energy depends on the temperature. For silicon & germanium, this energy is given by

$$E_g = 1.21 - 3.6 \times 10^{-4} \times T \quad \text{eV (for Silicon)}$$

$$E_g = 0.785 - 2.23 \times 10^{-4} \times T \quad \text{eV (for Germanium)}$$

where T = Absolute temperature in $^\circ\text{K}$

Assuming room temperature to be 27°C i.e. 300°K , the forbidden gap energy for Si & Ge can be calculated from the above equations. The forbidden gap for the germanium is 0.72 eV while for the silicon it is 1.12 eV at room temperature. The silicon & germanium are the two widely used semiconductor materials in electronic devices.

S.No	Parameter	Conductor	Insulator	Semiconductor
1.	Forbidden gap	not exist	Large of about 6ev	Small of about 1ev
2.	Conductivity	Very High	Very low	Moderate increases with temp
3.	Resistivity	Very low	Very High	Moderate
4.	Temperature Co-efficient of resistance	+ve	-ve	-ve
5.	Effect of Temperature on resistance	Resistance increases with temperature	Resistance decreases with temperature	Resistance decreases with temp.
6.	no. of free electrons	Very large	Very small	Moderate
7.	Examples	Copper, Iron, Silver, Tungsten, Aluminium	Carbon, Glass, Paper, Rubber	Germanium, Silicon
8.	Applications	wires, cables, lamp filaments, conductors etc.	For providing proper insulation in various applications, machines & in capacitors	In semiconductor devices such as diodes, Transistors etc.

Problem 1 Calculate the value of forbidden gap for Silicon & germanium at the temperature of 35°C.

Forbidden gap for Silicon is given by

$$E_G = 1.21 - 3.6 \times 10^{-4} \times T$$

$$\text{Now } T = 35 + 273 = 308^\circ \text{K}$$

$$\therefore E_G = 1.21 - 3.6 \times 10^{-4} \times 308 = 1.099 \text{ eV}$$

while forbidden gap for germanium is given by

$$E_G = 0.785 - 2.23 \times 10^{-4} \times T$$

$$= 0.785 - 2.23 \times 10^{-4} \times 308$$

$$= 0.7163 \text{ eV}$$

Problem The mobility of free electrons & holes in germanium are 3800 & 1800 $\text{cm}^2/\text{V-s}$ respectively. The corresponding values for pure silicon are 1300 & 500 $\text{cm}^2/\text{V-s}$ respectively. Determine the values of intrinsic conductivity for both germanium & silicon. Assume $n_i = 2.5 \times 10^{13}$ for germanium & $n_i = 1.5 \times 10^{10}$ for silicon at room temperature.

Sol

(i) The intrinsic conductivity of germanium

$$\begin{aligned}\sigma_i &= q n_i (\mu_n + \mu_p) \\ &= (1.6 \times 10^{-19}) (2.5 \times 10^{13}) (3800 + 1800) \\ &= 0.0224 \text{ S/cm}\end{aligned}$$

(ii) The intrinsic conductivity of silicon.

$$\begin{aligned}\sigma_i &= q n_i (\mu_n + \mu_p) \\ &= (1.6 \times 10^{-19}) (1.5 \times 10^{10}) (1300 + 500) \\ &= 4.32 \times 10^{-6} \text{ S/cm}\end{aligned}$$

In a pure semiconductor, the no. of holes is equal to no. of electrons. Thermal agitation continues to produce new electron-hole pairs & the electron-hole pair disappears because of recombination. With each electron-hole pair created, two charge-carrying parties are formed. One is -ve which is the free electron with mobility μ_n . The other is +ve, i.e. the hole mobility μ_p . The electrons & holes move in opposite directions in an electric field E , but since they are of opposite sign, the current due to each is in the same direction. Hence the total current density J within intrinsic semiconductor is given by

$$\begin{aligned} J &= J_n + J_p \\ &= q \cdot n \cdot \mu_n \cdot E + q \cdot p \cdot \mu_p \cdot E \\ &= (n \mu_n + p \mu_p) q E \\ &= \sigma E \end{aligned}$$

where J_n = electron drift current density

J_p = hole drift current density

n = no. of electrons per unit volume, i.e. magnitude of free-electron (-ve) concentration.

p = no. of holes per unit volume, i.e. magnitude of holes (+ve) concentration.

E = applied electric field strength, V/m

q = charge of electron or hole, Coulombs.

Hence, σ is the conductivity of a semiconductor which is equal to $(n \mu_n + p \mu_p) q$. The resistivity (ρ) of a semiconductor is the reciprocal of conductivity, i.e. $\rho = \frac{1}{\sigma}$.

It is evident from the above equation that current density within a semiconductor is directly proportional to the applied electric field.

For pure (intrinsic) semiconductor $n = p = n_i$
where n_i is the intrinsic carrier concentration.

$$\text{Therefore } J = n_i (e\mu_n + e\mu_p) qE$$

Conductivity of an intrinsic semiconductor is

$$\sigma_i = q \cdot n_i (\mu_n + \mu_p)$$

Hence it is clear that conductivity of an intrinsic semiconductor depends upon its intrinsic carrier concentration (n_i) & the mobility of electrons (μ_n) & holes (μ_p).

The intrinsic conductivity of germanium & Silicon increase by approximately 5 percent ° & 7 percent ° rise in temp respectively due to the influence of n_i .

Conductivity of N- and P-type semiconductors: The conductivity of an intrinsic semiconductor

$$\begin{aligned}\sigma_i &= q \cdot n_i (\mu_n + \mu_p) \\ &= q (n\mu_n + p\mu_p)\end{aligned}$$

For N-type semiconductor as $n \gg p$ then conductivity $\sigma = qn\mu_n$

For P-type semiconductor as $p \gg n$ then conductivity $\sigma = qp\mu_p$

Extrinsic Semiconductors.

Semiconductors are classified as

- (i) Intrinsic (Pure)
- (ii) Extrinsic (Impure)

The extrinsic semiconductors are of N-type & P-type

Intrinsic Semiconductor. A pure semiconductor is

called intrinsic semiconductor. At the room temp. some of the valence electrons may acquire sufficient energy to enter the conduction band to form free electrons. Under the influence of electric field, these electrons constitute electric current. A missing electron in the valence band leaves a vacant space there, which is known as a hole as shown in fig 1. Holes also contribute to electric current.

Under the influence of electric field, total current through the semiconductor is the sum of currents due to free electrons & holes.

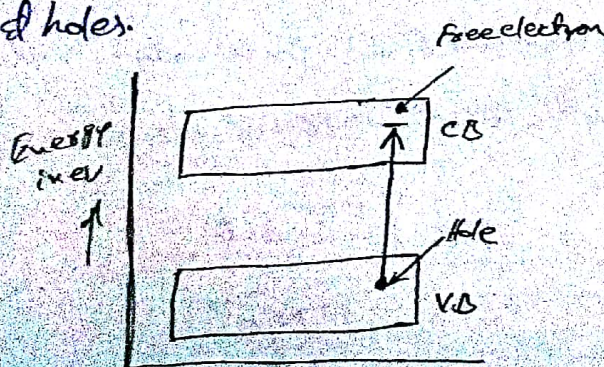


Fig 1 Creation of electron-hole pair in a semiconductor

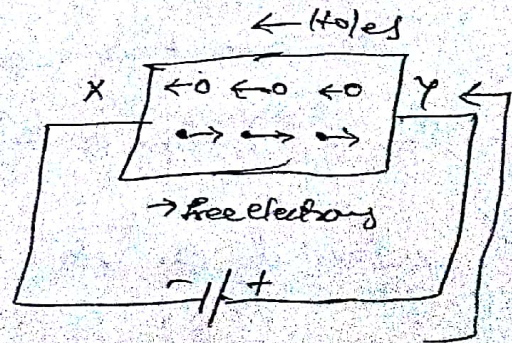


Fig 2 Current Conduction in Semiconductor.

Though the total current inside the semiconductor is due to free electrons & holes, the current in the external wire is due to electrons. In fig 2 holes being positively charged move towards the -ve terminal of the battery. As the holes reach the -ve terminal of the battery,

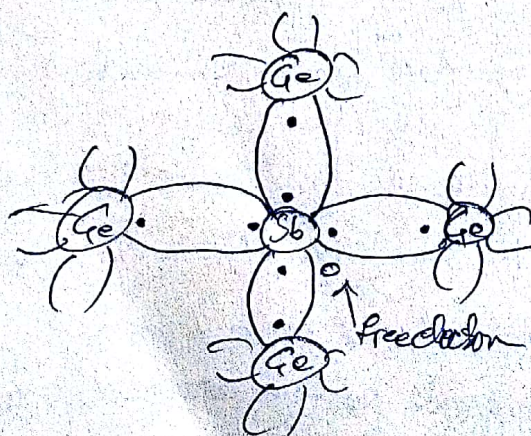
electrons enter the semiconductor near the terminal (x) and combine with the holes. At the same time, the loosely held electrons near the +ve terminal (y) are attracted away from their atoms into the +ve terminal. This creates new holes near the +ve terminal which again drift towards the -ve terminal.

Extrinsic Semiconductor. Due to the poor conduction at room temperature, the intrinsic semiconductor as such, is not useful in the electric devices. Hence, the current conduction capability of the intrinsic semiconductor should be increased.

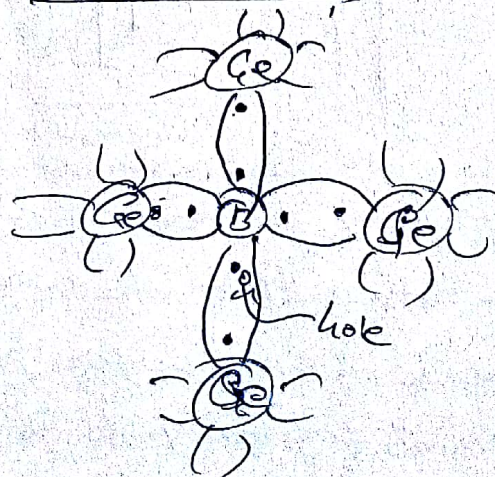
This can be achieved by adding a small amount of impurity to the intrinsic semiconductor, so that it becomes impure or extrinsic semiconductor. This process of adding impurity is known as 'doping'.

The amount of impurity added is externally small, say 1 or 2 atoms of impurity to 10^6 intrinsic atoms.

n-type semiconductor



p-type semiconductor



The flow of charge, i.e. current, through a semiconductor material are of two types, namely drift & diffusion.

Drift current

When a voltage is applied to a semiconductor, the free electrons try to move in a straight line towards the +ve terminal of the battery. The electrons, moving towards +ve terminal collide with the atoms of semiconductor & connecting wires, along its way. Each time the electron strikes an atom, it rebounds in a random direction. But still the applied voltage makes the electrons drift towards the +ve terminal. This drift causes current to flow in a semiconductor, under the influence of the applied voltage. This current produced due to drifting of free electrons is called "drift current" & the velocity with which electrons drift is called drift velocity.

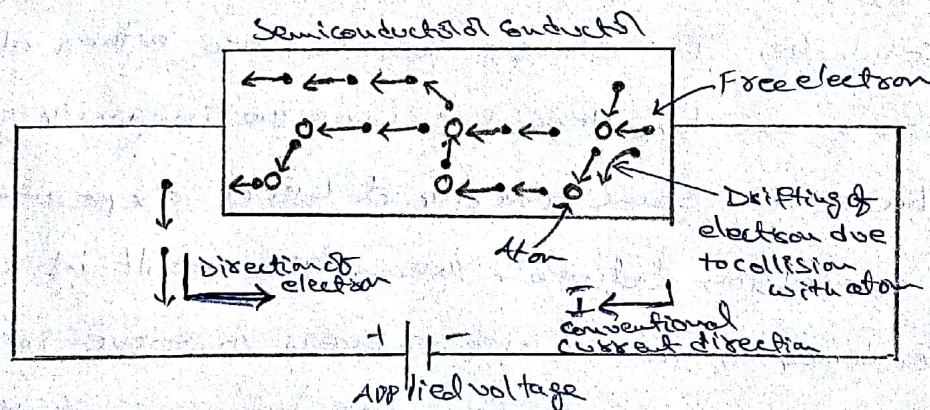


Fig: Drift mechanism causing drift current

The drift ~~is~~ current density due to the charge carriers such as free electrons & holes are the current passing through a square centimeter perpendicular to the direction of flow. The equation for the drift current density, J_n due to free electrons is given by

$$J_n = q n \mu_n E$$

and the drift current density, J_p , due to holes is given by

$$J_p = q p \mu_p E \text{ A/cm}^2$$

where n = no. of free electrons per cubic centimetre

p = no. of holes per cubic centimetre

μ_n = mobility of electrons in $\text{cm}^2/\text{V-s}$

μ_p = mobility of holes in $\text{cm}^2/\text{V-s}$

E = Applied electric field intensity in V/cm

q = Charge of an electron

$$= 1.6 \times 10^{-19} \text{ Coulomb}$$

Diffusion Current:

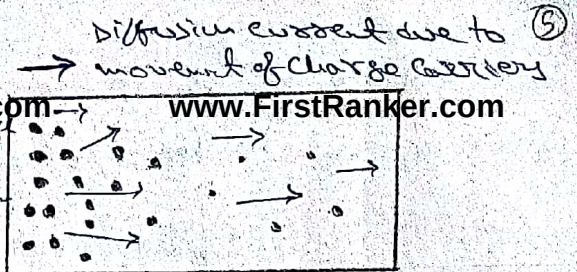
This is the current which is due to the transport of charges occurring because of non uniform concentration of charged particles in a semiconductor.

Consider a piece of semiconductor which is non-uniformly doped. Due to such nonuniform doping, one type of charge carriers occur at one end of a piece of semiconductor. The charge carriers are either electrons & holes, of one type depending upon the impurity used. They have the same polarity & hence experience a force of repulsion between them. The result is that there is a tendency of the charge carriers to move gradually i.e. to diffuse from the region of high carrier density to the low carrier density. This process is called diffusion. This movement of charge carriers under the process of diffusion constitutes a current called diffusion current.



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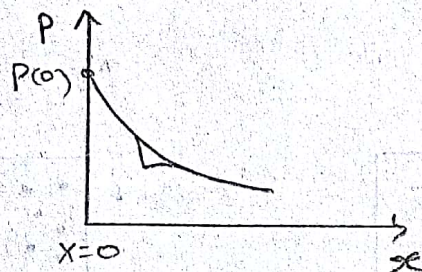


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Non-uniform concentration.

Process of diffusion

Fig: Diffusion current



The graph of concentration of holes against x

Slope of graph = concentration gradient

$$= \frac{dP}{dx}$$

The diffusion current density is proportional to the concentration gradient, which is responsible for the diffusion and hence the diffusion current

$$J_p \propto \frac{dP}{dx}$$

$$J_p = q D_p \frac{dP}{dx}$$

where D_p = Diffusion Constant for holes in m^2/sec

The current due to holes is in the direction of the conventional current and hence treated as +ve. But slope of the graph i.e. $\frac{dP}{dx}$ is -ve giving the -ve diffusion current density for holes. Hence diffusion current density for holes is mathematically expressed as

$$J_p = -q D_p \frac{dP}{dx}$$

In case of n-type bar, such diffusion current is due to the electrons. Current due to the electrons is in opposite direction to the conventional current and mathematically treated to be -ve. The concentration gradient $\frac{dn}{dx}$ is +ve

diffusion current density to electrons is expressed by,

$$J_n = +q D_n \frac{dn}{dx}$$

where D_n = Diffusion Coefficient for electrons in square meters per second (m^2/sec).

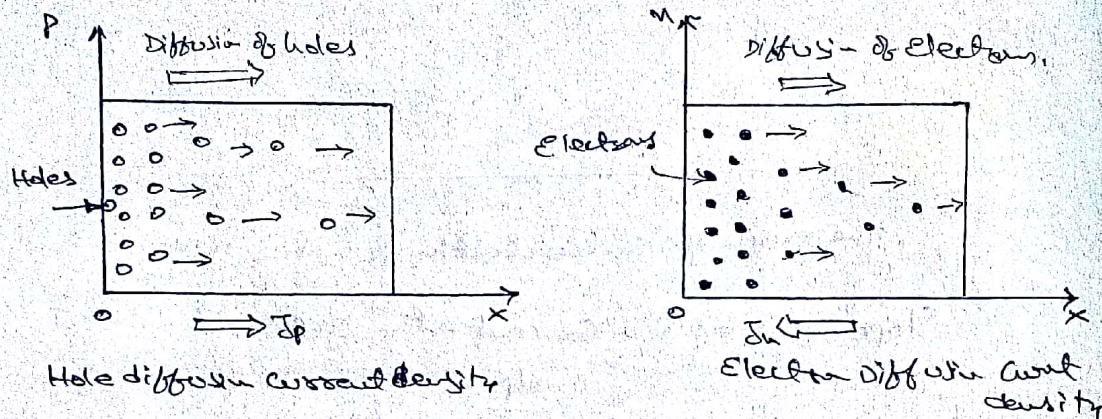


Fig. Diffusion Current densities

Total Current Density Due to Drift & Diffusion

Drift current density for electrons & holes can be expressed as

$$J_n = n q \mu_n E$$

$$J_p = p q \mu_p E$$

Diffusion current density for electrons & holes can be expressed as

$$J_n = q D_n \frac{dn}{dx}$$

$$J_p = -q D_p \frac{dp}{dx}$$

$\therefore$ Total current density due to the electron can be expressed as

$$J_n = n q \mu_n E + q D_n \frac{dn}{dx}$$

& total current density due to the holes can be expressed as

$$J_p = p q \mu_p E - q D_p \frac{dp}{dx}$$

And hence the total current density due to the electrons & holes (drift + diffusion) is

$$J = J_n + J_p$$

It is now known that drift current density is proportional to the mobility (μ) while diffusion current density is proportional to the diffusion constant (D). There exists a fixed relation between these two constants which is called Einstein's relation.

(57)

The equation which relates the mobility (μ) & the diffusion constant (D) is known as the Einstein's Relationship.

Mathematically it is expressed as

$$\frac{D_p}{\mu_p} = \frac{D_n}{\mu_n} = kT = \text{Constant at fixed temp.}$$

where T is the temperature in $^{\circ}\text{K}$.

And k is the Boltzmann's constant = ~~8.62~~ $8.62 \times 10^{-5} \text{ eV/K}$

Diffusion length L

Due to the recombination, the concentration of charge carriers decrease exponentially with the distance at the time of diffusion. The charge carriers have mean life time denoted by τ for which they exist before recombination.

$\therefore \tau_n = \text{Mean life time of the free electron}$

$\tau_p = \text{Mean life time of free hole.}$

After recombination, these charge carriers vanish & concentration decreases exponentially with distance.

The average distance covered by an excess charge carrier while diffusion during its life time is called diffusion length of that charge carrier, is denoted by L .

$\therefore L_n = \text{Diffusion length of free electrons}$ www.FirstRanker.com www.FirstRanker.com

$L_p = \text{Diffusion length of free hole}$

The diffusion length L is related to mean life time τ through the diffusion constant D of the charge carrier. Mathematically this relationship is given by

$$L = \sqrt{D\tau}$$

thus, $L_n = \sqrt{D_n \tau_n}$ $\tau_n = \frac{L_n^2}{D_n}$

$L_p = \sqrt{D_p \tau_p}$ $\tau_p = \frac{L_p^2}{D_p}$

Law of Junction

Mass Action Law

If n is the concentration of free electrons & p is the concentration of holes then the law of mass action states that the product of concentrations of electrons & holes is always constant, at a fixed temperature.

Mathematically it is expressed as,

$$np = n_i^2$$

where n_i is intrinsic concentration

Important observations

1. The law can be applied to both intrinsic & extrinsic semiconductors.
2. As n_i depends on temperature, the law is applicable at a fixed temperature.
3. In case of extrinsic semiconductors, n_i is intrinsic concentration of the basic semiconductor material used.

The law can be used to find the electron & hole densities in intrinsic semiconductors.

The law of mass-action has given the relationship between free electron concentration & hole concentration. These concentrations are further related by the law of Electrical Neutrality as explained below.

Let N_D = Concentration of donor atoms, in an n-type semiconductor.

N_A = Concentration of acceptor atoms, in an p-type semiconductor

P = Hole concentration.

n = Free electron concentration.

$\therefore$ Total no. of ^{charges} $+ve$ $/m^3$ (called total +ve charge density)

in a semiconductor = $N_D + P$

& Total no. of $-ve$ charges $/m^3$ (called total $-ve$ charge density)

in a semiconductor = $N_A + n$

Since the semiconductor, as a whole, is electrically neutral, therefore magnitude of total positive charge density is equal to total negative charge i.e.

$$N_D + P = N_A + n \rightarrow \textcircled{1}$$

Now consider an n-type semiconductor, we know that in n-type semiconductor, the concentration of acceptor atoms is zero (i.e. $N_A = 0$), and also the no. of free electrons is much larger than the no. of holes ($n \gg p$). Therefore for an n-type semiconductor, the eq. (1) may be written as

$$N_D = n$$

The above relation shows that in an N-type Semiconductor, the free electron concentration (n) is equal to the no. of donor atoms (N_D). The concentration of holes in an N-type Semiconductor may be obtained by using mass action law (i.e. $n \cdot p = n_i^2$) and its value is given by the relation

$$p = \frac{n_i^2}{n} = \frac{n_i^2}{N_D} \rightarrow (2)$$

Similarly in a P-type Semiconductor, the concentration of donor atoms is zero (i.e. $N_D = 0$) & the no. of holes is much larger than no. of free electrons ($p \gg n$). Therefore for a P-type Semiconductor, the eq. (1) may be written as:

$$p = N_A$$

The above relation shows that in a P-type Semiconductor, the hole concentration (p) is equal to the no. of acceptor atoms (N_A). The concentration of free electrons may be obtained by using mass action law ($n \cdot p = n_i^2$) & its value is given by the relation

$$n = \frac{n_i^2}{p} = \frac{n_i^2}{N_A} \rightarrow (3)$$

Extrinsic Conductivity:

The Conductivity of an N-type Semiconductor is given by

$$\sigma_N = q n \mu_n = q N_D \mu_n$$

$$\text{Since } n = N_D$$

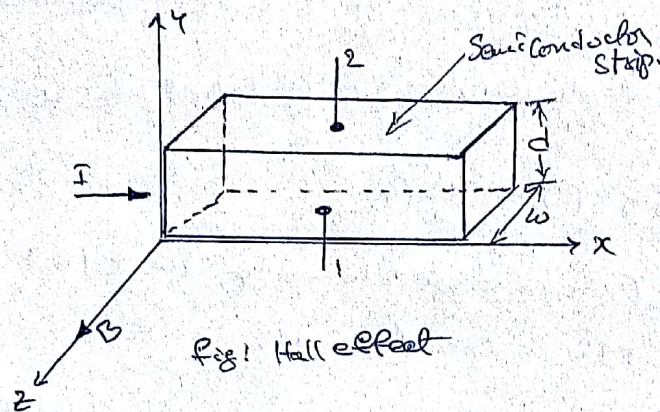
The Conductivity of a P-type Semiconductor is given by

$$\sigma_P = q p \mu_p = q N_A \mu_p$$

$$\text{Since } p = N_A$$

If a specimen of metal or semiconductor, carrying current I is placed in a transverse magnetic field with flux density B then an electric field E is induced in the direction perpendicular to both I & B . This phenomenon is called Hall effect.

This is very useful in semiconductors to determine the type of material, carrier concentration & mobility of the material.



Consider a semiconductor strip carrying current I as shown in the fig. The current I is flowing in the $+ve$ x direction. It is placed in the magnetic field with density B acting in the $+ve$ z direction.

In such conditions, the force is exerted on the current carriers in the $-ve$ y direction. This force is called Lorentz force. Thus if semiconductor used is n type, all the electrons, which are majority carriers will be forced towards side 1 of the strip. Hence side 1 will become negatively charged with respect to side 2.

In an equilibrium state, the induced electric field E due to Hall effect must exert a force on the carrier, which must balance the ~~magnetic~~ magnetic force. Thus,

$$F_{\text{electric}} = qE$$

$$F_{\text{magnetic}} = Bqv_d$$

$$qE = Bqv_d \rightarrow (1)$$

$$E = Bv_d \rightarrow (2)$$

where v_d is drift velocity. Also the electric field intensity due to Hall effect is

$$E = \frac{V_H}{d} \rightarrow (3)$$

where V_H is Hall voltage appearing between surfaces 1 & 2.
 d is the distance between surfaces 1 & 2.

The current density (J) is related to charge density (ρ) by

$$J = \rho v_d \rightarrow (4)$$

where ρ is charge density in C/m^3
 v_d = speed in m/s

Further, the current density (J) is related to current I by

$$J = \frac{I}{Area} = \frac{I}{wd} \rightarrow (5)$$

where w is width of the strip in the direction of B
 d is distance between surfaces 1 & 2.

combining (4) & (5)

$$\rho v_d = \frac{I}{wd} \rightarrow (6)$$

now by eq (3) $V_H = E d$

$$= Bv_d d \quad \because E = Bv_d$$

$$= \frac{BdJ}{\rho} \quad \because J = \rho v_d$$

$$= \frac{BdI}{\rho wd} = \frac{BI}{\rho w}$$

$$\therefore \boxed{V_H = \frac{BI}{\rho w}} \rightarrow (7)$$

Thus if V_H , B , I & w are measured, the charge density P can be determined.

The Hall co-efficient, R_H is defined by

$$R_H = \frac{1}{P} \rightarrow (8)$$

So that eq (7) becomes

$$V_H = \frac{R_H B I}{w} \rightarrow (9)$$

The Hall co-efficient for a p-type semiconductor is +ve, whereas it is -ve for an n-type semiconductor.

The advantage of hall effect transducers is that they are non-contact devices with high resolution & small size.

If the polarity of V_H is such that the surface 2 is +ve then the carriers are the electrons & we can write,

$$P = nq$$

while if the surface 1 is +ve then the carriers are holes & we can write,

$$P = pq$$

The Conductivity σ for Extrinsic Semiconductor is given by,

$$\sigma = \mu n q = \frac{\mu}{R_H}$$

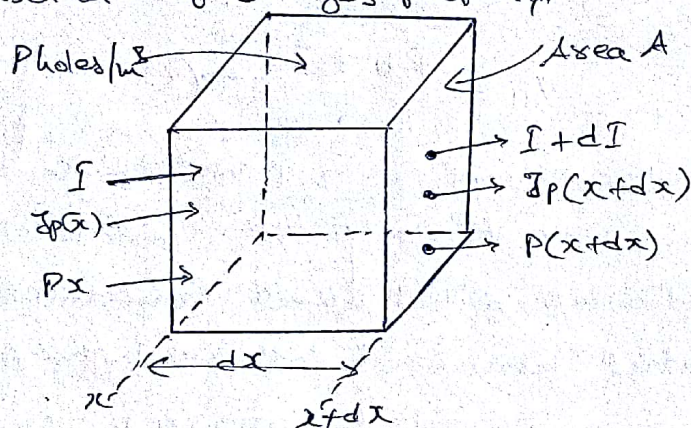
where μ = mobility of carriers in $m^2/V-s$

$$\mu = \sigma R_H = \frac{\sigma V_H w}{B I}$$

$$\sigma = \text{Conductivity} = \frac{1}{\text{sensitivity}}$$

$$\mu = \frac{1}{\text{sensitivity}} \times \frac{V_H w}{B I}$$

The continuity equation is a differential equation that governs the relationship of the carrier concentration both with time & distance. This equation is derived on the basis of conservation of charges property.



Consider the infinitesimal p type element of Volume of area A & length dx as shown in fig. The average hole concentration is p/m^3 . The current entering the volume at x is I & leaving at $x+dx$ is $I+dI$. This change in current is because of diffusion. Now due to diffusion the concentration of charge carriers decreases exponentially with the distance.

Hence,

$\therefore dI =$ no. of Coulombs per second decreased within the volume. $\rightarrow (1)$

now if τ_p is the mean life time of the holes then,

$\frac{P}{\tau_p} =$ Holes per second lost by recombination per unit volume

Due to recombination, no. of Coulombs per second decreased within the given volume is,

$$\begin{aligned}
 &= \left[\frac{\text{charge}}{\text{on hole}} \right] \times \left[\frac{\text{holes/sec}}{\text{per unit volume}} \right] \times [\text{Volume}] \\
 &= q \times \frac{P}{\tau_p} \times (A dx) = q A dx \frac{P}{\tau_p} \rightarrow (2)
 \end{aligned}$$

While g is the rate at which electron hole pairs are generated by thermal generation per unit volume. Due to this, no. of Coulombs per second increases with the volume

$$= \left[\text{Charges on hole} \right] \times \left[\text{Rate of generation} \right] \times \left[\text{Volume} \right]$$

$$= q g A dx \rightarrow (3)$$

Thus the total change in no. of Coulombs per second is because of three factors as indicated by the eq (1) (2) & (3)

Total change in holes per unit volume per second is $\frac{dp}{dt}$. Hence the total change in Coulombs per second within the given volume.

$$= q \frac{dp}{dt} \times (\text{Volume})$$

$$= q \frac{dp}{dt} A dx$$

$$= q A dx \frac{dp}{dt} \rightarrow (4)$$

According to law of conservation of charges.

$$q A dx \frac{dp}{dt} = -q A dx \frac{p}{\tau_p} + q g A dx - dI \rightarrow (5)$$

note: The -ve sign indicates decrease while +ve indicates increase in no. of Coulombs per second.

$$\therefore \frac{dp}{dt} = -\frac{p}{\tau_p} + g - \frac{dI}{q A dx} \rightarrow (6)$$

But $J = \frac{I}{A} = \text{current density}$

$$\therefore \frac{dp}{dt} = -\frac{p}{\tau_p} + g - \frac{1}{q} \cdot \frac{dJ}{dx} \rightarrow (7)$$

w.k.T The total current density J is due to drift & diffusion current

$$J = -q D_p \frac{dp}{dx} + p q \mu_p E \rightarrow (8)$$

Subjected to no external electric field then hole density will attain a constant value p_0 . Under this condition $I = 0$, i.e. $\frac{dp}{dt} = 0$ due to equilibrium. Using (7)

$$0 = -\frac{p_0}{\tau_p} + g - 0$$

$$\therefore g = \frac{p_0}{\tau_p} \rightarrow (8)$$

The eq (8) indicates the thermal equilibrium i.e. the rate at which holes are thermally generated just equal to the rate at which holes are lost due to recombination.

Using (8) & (9) in (7)

$$\frac{dp}{dt} = -\frac{p}{\tau_p} + \frac{p_0}{\tau_p} - \frac{1}{q} \frac{d}{dx} \left[-q D_p \frac{dp}{dx} + q p \mu_p E \right]$$

$$\frac{dp}{dt} = \frac{p_0 - p}{\tau_p} + \frac{1}{q} \frac{d}{dx} \left[q D_p \frac{dp}{dx} - q p \mu_p E \right]$$

$$\boxed{\frac{dp}{dt} = \frac{p_0 - p}{\tau_p} + D_p \frac{d^2 p}{dx^2} - \mu_p \frac{d(pE)}{dx}} \rightarrow (10)$$

This is called equation of conservation of charge or the continuity equation.

As holes in n-type material are considered

$$\frac{\partial p_n}{\partial t} = \frac{p_{n0} - p_n}{\tau_p} + D_p \frac{\partial^2 p_n}{\partial x^2} - \mu_p \frac{\partial p_n E}{\partial x}$$

Similarly the continuity equation for the electrons in p-type material can be written as

$$\frac{\partial n_p}{\partial t} = \frac{n_{p0} - n_p}{\tau_n} + D_n \frac{\partial^2 n_p}{\partial x^2} - \mu_n \frac{\partial (n_p E)}{\partial x}$$

Fermi Dirac function of Fermi levels in intrinsic & Extrinsic Semiconductors.

Fermi Dirac function:

~~In a pure or intrinsic semiconductor the~~

In Energy band diagram, the probability that the energy level is occupied by an electron is given by Fermi-Dirac probability function denoted as $f(E)$.

It is given by the Expression,

$$f(E) = \frac{1}{1 + e^{(E-E_F)/kT}}$$

(1)

$$f(E) = \frac{1}{1 + e^{(E-E_F)/kT}}$$

where $k = \text{Boltzmann's constant in } qV/qK$

$T = \text{Temp in } ^\circ K$

$E_F = \text{Fermi level or characteristic energy of the crystal in eV}$

$E = \text{Energy level occupied by an electron in eV}$

The Fermi level E_F indicates the probability of occupancy of an energy level by an electron.

Fermi levels in Intrinsic Semiconductor,

In intrinsic semiconductor, the probability of finding an electron in the conduction band is zero & the probability of finding a hole in the valence band is zero, at absolute zero i.e. $T = 0^\circ K$.

Now let E_c be the lowest energy level in the conduction band while E_v be the highest energy level in the valence band. As temperature increases, equal no. of electrons & holes get generated. Hence probability of finding electron in conduction band & probability of finding hole in valence band is same.

The Fermi level in such a case is given by,

$$E_F = \frac{E_c + E_v}{2}$$

Proof

In intrinsic material, the crystal must be electrically neutral.

$$n_i = p_i$$

$$N_c e^{-(E_c - E_F)/kT} = N_v e^{-(E_F - E_v)/kT}$$

N_c & N_v are the density of states in conduction & valence band respectively.

$$\frac{N_c}{N_v} = \frac{e^{-(E_F - E_v)/kT}}{e^{-(E_c - E_F)/kT}}$$

$$= e^{(E_F + E_v + E_c - E_F)/kT}$$

Taking logarithm of both sides

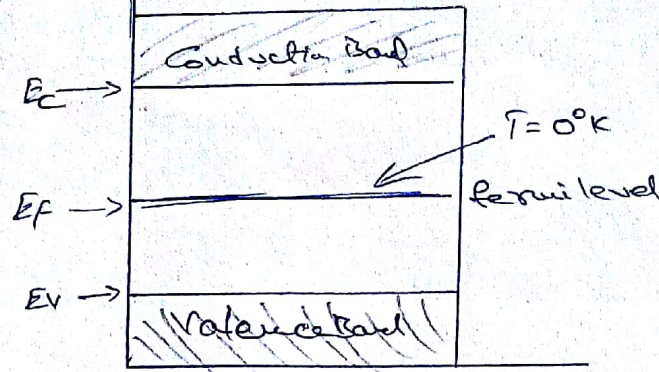
$$\ln \frac{N_c}{N_v} = (-E_F + E_v + E_c - E_F)/kT$$

$$= (E_c + E_v - 2E_F)/kT$$

$$kT \ln \frac{N_c}{N_v} = E_c + E_v - 2E_F$$

$$\therefore E_F = \frac{E_c + E_v}{2} - \frac{kT}{2} \ln \frac{N_c}{N_v}$$

$$E_F = \frac{E_c + E_v}{2} \quad \because N_c = N_v \text{ then } \ln \frac{N_c}{N_v} = 0$$



Fermi level in Extrinsic Semiconductor.

The Fermi level in an n-type material is given by

$$E_F = E_C - kT \ln \frac{N_C}{N_D}$$

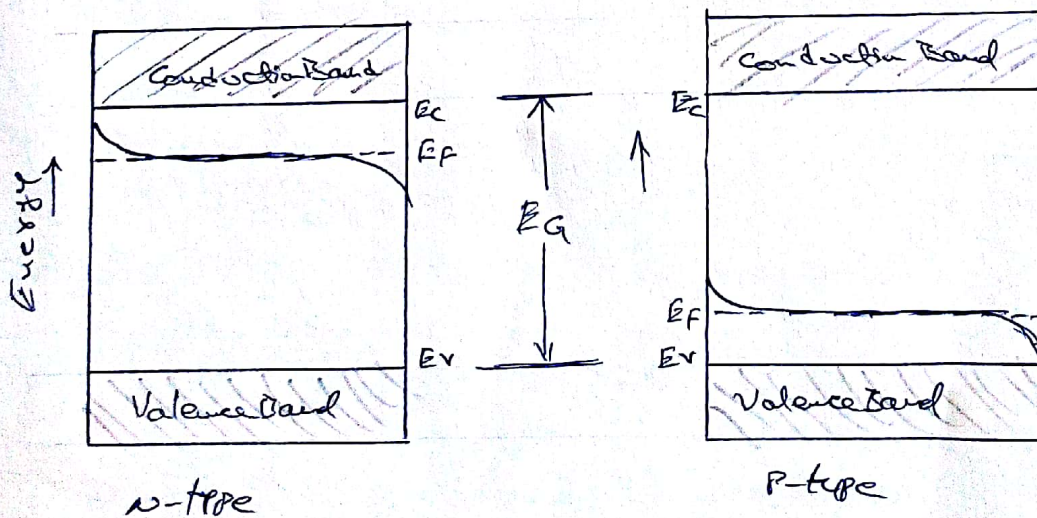
where $N_D = N_C e^{-(E_C - E_F)/kT}$ the concentration of donor atoms.

The Fermi level in a p-type material is given by

$$E_F = E_V + kT \ln \frac{N_V}{N_A}$$

where $N_A = N_V e^{-(E_F - E_V)/kT}$ the concentration of acceptor atoms.

The change in the position of Fermi level in n- & p-type Semiconductor is shown in below.



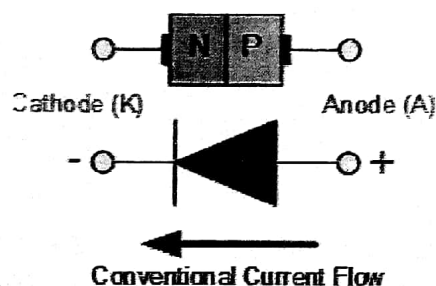
UNIT – 2

JUNCTION DIODE CHARACTERISTICS

SPECIAL SEMICONDUCTOR DEVICES

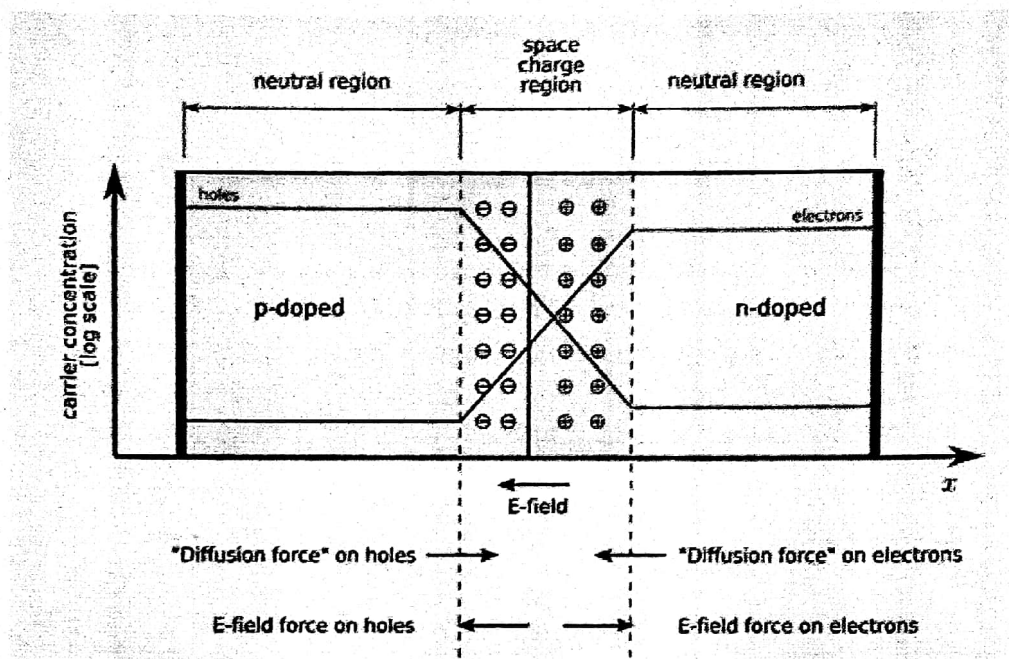
UNIT II**JUNCTION DIODE CHARACTERISTICS****1.1 QUANTITATIVE THEORY OF PN JUNCTION DIODE:****1.1.1 PN JUNCTION WITH NO APPLIED VOLTAGE OR OPEN CIRCUIT CONDITION:**

In a piece of sc, if one half is doped by p type impurity and the other half is doped by n type impurity, a PN junction is formed. The plane dividing the two halves or zones is called PN junction. As shown in the fig the n type material has high concentration of free electrons, while p type material has high concentration of holes. Therefore at the junction there is a tendency of free electrons to diffuse over to the P side and the holes to the N side. This process is called

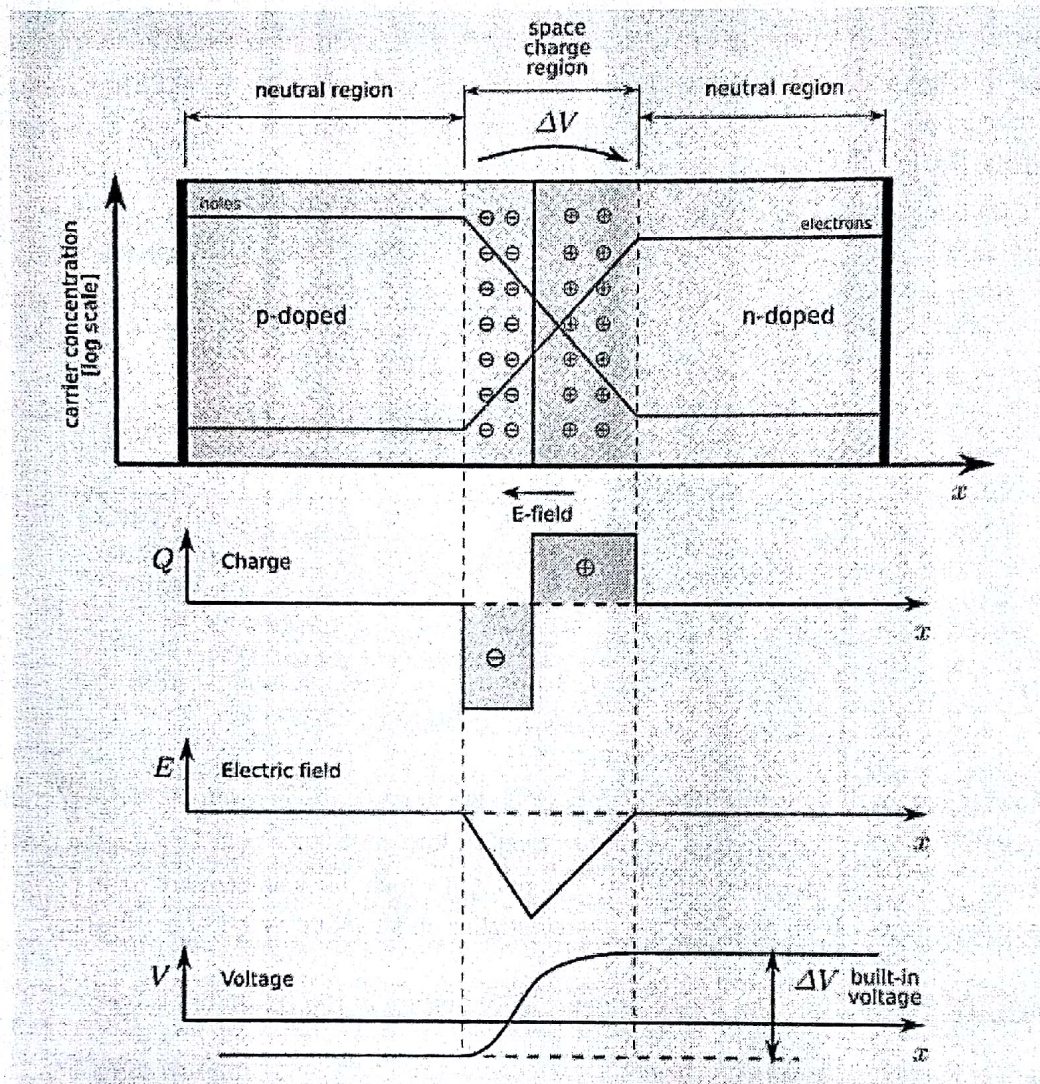


diffusion. As the free electrons move across the junction from N type to P type, the donor atoms become positively charged. Hence a positive charge is built on the N-side of the junction. The free electrons that cross the junction uncover the negative acceptor ions by filling the holes. Therefore a negative charge is developed on the p-side of the junction..This net negative charge on the p side prevents further diffusion of electrons into the p side. Similarly the net positive charge on the N side repels the hole crossing from p side to N side. Thus a barrier is set up near the junction which prevents the further movement of charge carriers i.e. electrons and holes. As a consequence of induced electric field across the depletion layer, an electrostatic potential difference is established between P and N regions, which are called the potential barrier, junction barrier, diffusion potential or contact potential, V_0 . The magnitude of the contact potential V_0 varies with doping levels and temperature. V_0 is 0.3V for Ge and 0.72 V for Si.

The electrostatic field across the junction caused by the positively charged N-Type region tends to drive the holes away from the junction and negatively charged p type regions tend to drive the electrons away from the junction. The majority holes diffusing out of the P region leave behind negatively charged acceptor atoms bound to the lattice, thus exposing a negative space charge in a previously neutral region. Similarly electrons diffusing from the N region expose positively ionized donor atoms and a double space charge builds up at the junction as shown in the fig. 1.7



It is noticed that the space charge layers are of opposite sign to the majority carriers diffusing into them, which tends to reduce the diffusion rate. Thus the double space of the layer causes an electric field to be set up across the junction directed from N to P regions, which is in such a direction to inhibit the diffusion of majority electrons and holes as illustrated in fig 1.7. The shape of the charge density, ρ , depends upon how diode is doped. Thus the junction region is depleted of mobile charge carriers. Hence it is called depletion layer, space region, and transition region. The depletion region is of the order of $0.5\mu\text{m}$ thick. There are no mobile carriers in this narrow depletion region. Hence no current flows across the junction and the system is in equilibrium. To the left of this depletion layer, the carrier concentration is $p = N_A$ and to its right it is $n = N_D$.

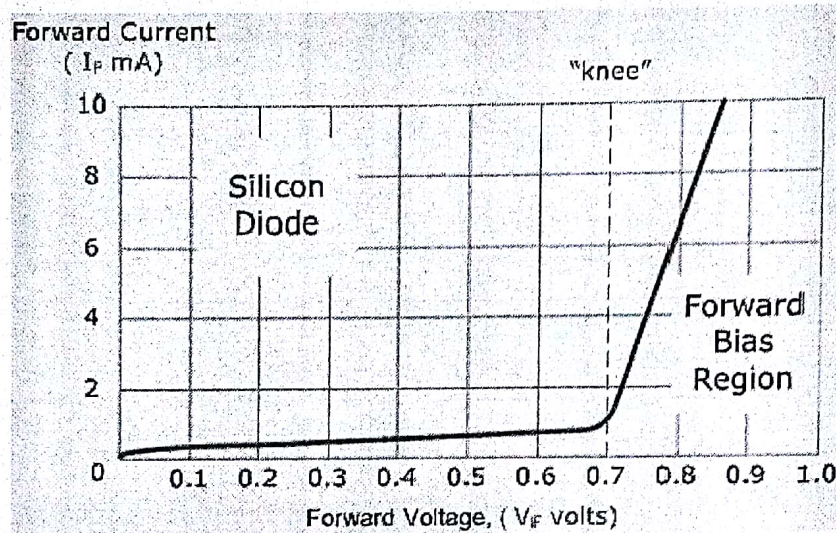


1.1.2 FORWARD BIASED JUNCTION DIODE

When a diode is connected in a **Forward Bias** condition, a negative voltage is applied to the N-type material and a positive voltage is applied to the P-type material. If this external voltage becomes greater than the value of the potential barrier, approx. 0.7 volts for silicon and 0.3 volts for germanium, the potential barriers opposition will be overcome and current will start to flow. This is because the negative voltage pushes or repels electrons towards the junction giving them the energy to cross over and combine with the holes being pushed in the opposite direction towards the junction by the positive voltage. This results in a characteristics curve of zero current

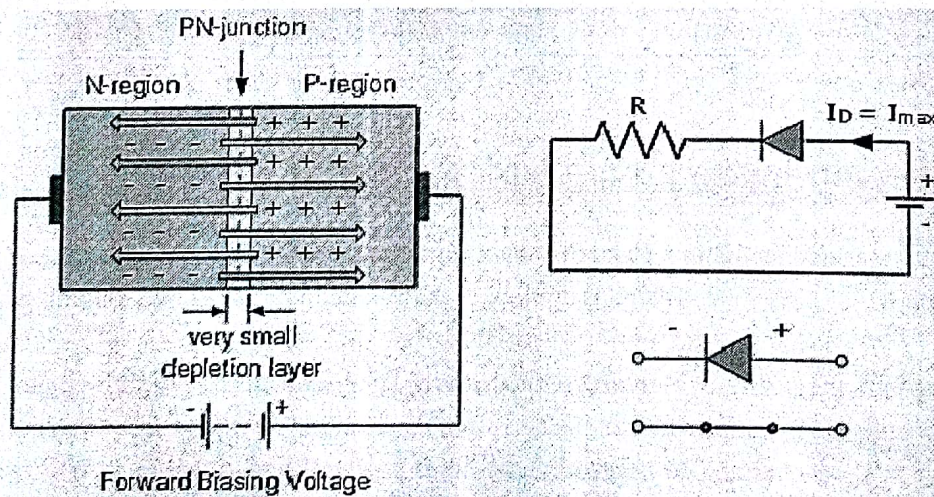
flowing up to this voltage point, called the "knee" on the static curves and then a high current flow through the diode with little increase in the external voltage as shown below.

Forward Characteristics Curve for a Junction Diode



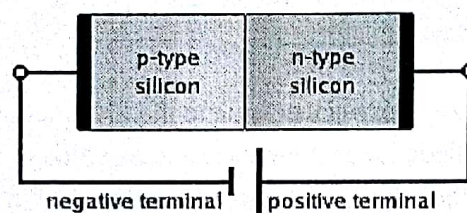
The application of a forward biasing voltage on the junction diode results in the depletion layer becoming very thin and narrow which represents a low impedance path through the junction thereby allowing high currents to flow. The point at which this sudden increase in current takes place is represented on the static I-V characteristics curve above as the "knee" point.

Forward Biased Junction Diode showing a Reduction in the Depletion Layer



This condition represents the low resistance path through the PN junction allowing very large currents to flow through the diode with only a small increase in bias voltage. The actual potential difference across the junction or diode is kept constant by the action of the depletion layer at approximately 0.3v for germanium and approximately 0.7v for silicon junction diodes. Since the diode can conduct "infinite" current above this knee point as it effectively becomes a short circuit, therefore resistors are used in series with the diode to limit its current flow. Exceeding its maximum forward current specification causes the device to dissipate more power in the form of heat than it was designed for resulting in a very quick failure of the device.

1.1.2 PN JUNCTION UNDER REVERSE BIAS CONDITION:

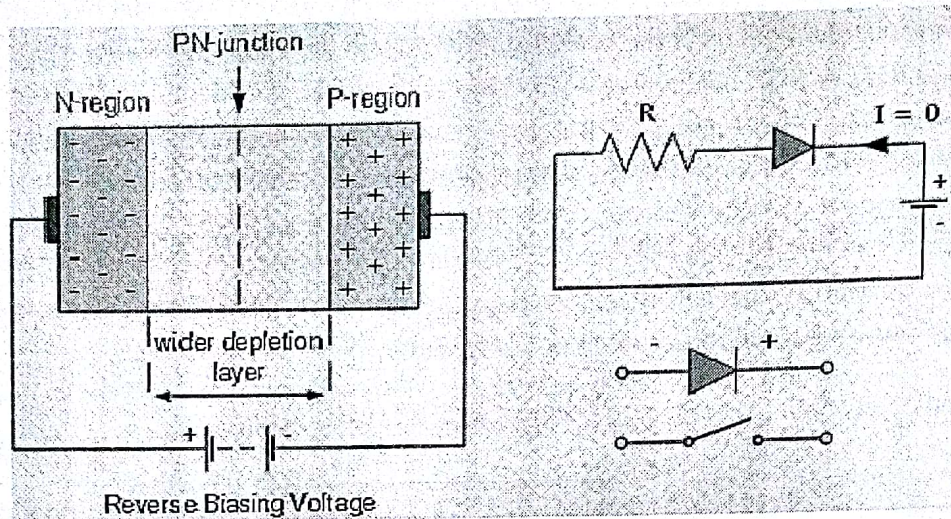


A silicon p-n junction in reverse bias.

Reverse Biased Junction Diode

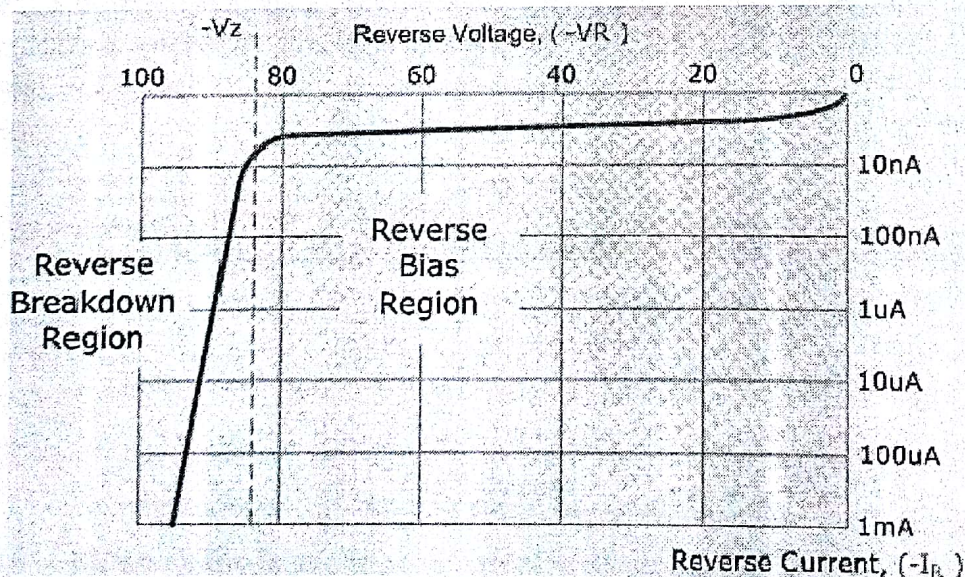
When a diode is connected in a **Reverse Bias** condition, a positive voltage is applied to the N-type material and a negative voltage is applied to the P-type material. The positive voltage applied to the N-type material attracts electrons towards the positive electrode and away from the junction, while the holes in the P-type end are also attracted away from the junction towards the negative electrode. The net result is that the depletion layer grows wider due to a lack of electrons and holes and presents a high impedance path, almost an insulator. The result is that a high potential barrier is created thus preventing current from flowing through the semiconductor material.

Reverse Biased Junction Diode showing an Increase in the Depletion Layer



This condition represents a high resistance value to the PN junction and practically zero current flows through the junction diode with an increase in bias voltage. However, a very small **leakage current** does flow through the junction which can be measured in microamperes, (μA). One final point, if the reverse bias voltage V_r applied to the diode is increased to a sufficiently high enough value, it will cause the PN junction to overheat and fail due to the avalanche effect around the junction. This may cause the diode to become shorted and will result in the flow of maximum circuit current, and this shown as a step downward slope in the reverse static characteristics curve below.

Reverse Characteristics Curve for a Junction Diode



Sometimes this avalanche effect has practical applications in voltage stabilising circuits where a series limiting resistor is used with the diode to limit this reverse breakdown current to a preset maximum value thereby producing a fixed voltage output across the diode. These types of diodes are commonly known as **Zener Diodes** and are discussed in a later tutorial.

1.2 VI CHARACTERISTICS AND THEIR TEMPERATURE DEPENDENCE: Diode terminal characteristics equation for diode junction current:

$$I_D = I_0 \left(e^{\frac{V}{\eta V_T}} - 1 \right)$$

Where $V_T = kT/q$;

V_D _ diode terminal voltage, Volts

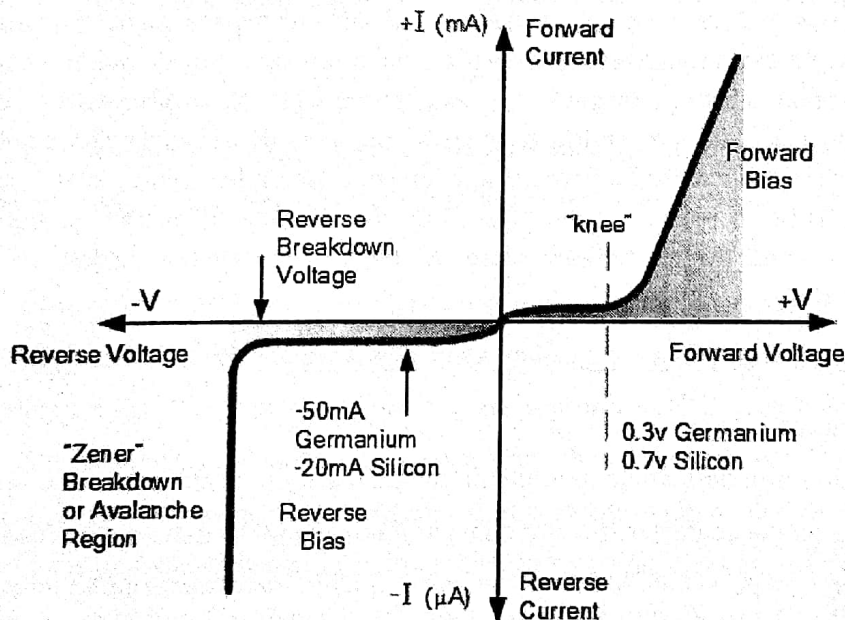
I_0 _ temperature-dependent saturation current, μA

T _ absolute temperature of p-n junction, K

k _ Boltzmann's constant $1.38 \times 10^{-23} J/K$

q _ electron charge $1.6 \times 10^{-19} C$

η = empirical constant, 1 for Ge and 2 for Si



Temperature Effects on Diode

Temperature can have a marked effect on the characteristics of a silicon semiconductor

diode as shown in Fig. 1.24. It has been found experimentally that the reverse saturation current I_o will just about double in magnitude for every 10°C increase in temperature.

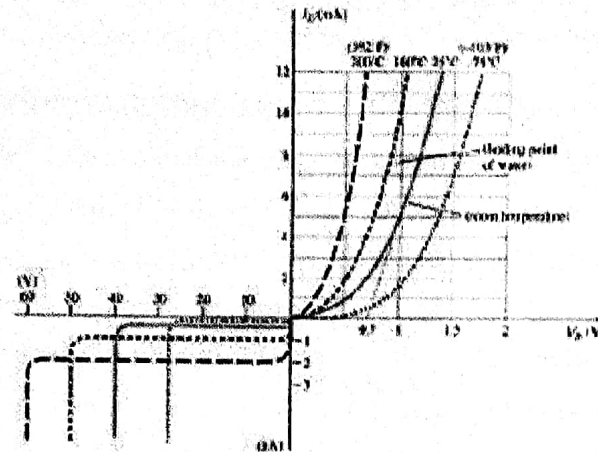


Figure 1.24 Variation in diode characteristics with temperature change.

It is not uncommon for a germanium diode with an I_o in the order of 1 or 2 A at 25°C to have a leakage current of 100 A _ 0.1 mA at a temperature of 100°C . Typical values of I_o for silicon are much lower than that of germanium for similar power and current levels. The result is that even at high temperatures the levels of I_o for silicon diodes do not reach the same high levels obtained for germanium—a very important reason that silicon devices enjoy a significantly higher level of development and utilization in design. Fundamentally, the open-circuit equivalent in the reverse bias region is better realized at any temperature with silicon than with germanium. The increasing levels of I_o with temperature account for the lower levels of threshold voltage, as shown in Fig. 1.24. Simply increase the level of I_o in and not rise in diode current. Of course, the level of V_K also will be increase, but the increasing level of I_o will overpower the smaller percent change in V_K . As the temperature increases the forward characteristics are actually becoming more “ideal,”

1.3 IDEAL VERSUS PRACTICAL RESISTANCE LEVELS

DC or Static Resistance

The application of a dc voltage to a circuit containing a semiconductor diode will result in an operating point on the characteristic curve that will not change with time. The resistance of the diode at the operating point can be found simply by finding the corresponding levels of V_D and I_D as shown in Fig. 1.25 and applying the following Equation:

$$R_D = \frac{V_D}{I_D}$$

The dc resistance levels at the knee and below will be greater than the resistance levels obtained for the vertical rise section of the characteristics. The resistance levels in the reverse-bias region will naturally be quite high. Since ohmmeters typically employ a relatively constant-current source, the resistance determined will be at a preset current level (typically, a few mill amperes).

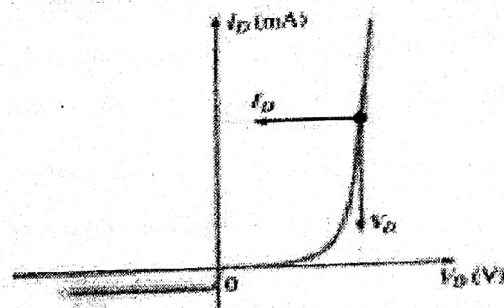


Figure 1.25 determining the dc resistance of a diode at a particular operating point.

AC or Dynamic Resistance

It is obvious from Eq. 1.5 that the dc resistance of a diode is independent of the shape of the characteristic in the region surrounding the point of interest. If a sinusoidal rather than dc input is applied, the situation will change completely. The varying input will move the instantaneous operating point up and down a region of the characteristics and thus defines a specific change in current and voltage as shown in Fig. 1.27. With no applied varying signal, the point of operation would be the Q-point appearing on Fig. 1.27 determined by the applied dc levels. The designation Q-point is derived from the word quiescent, which means "still or unvarying." A straight-line drawn tangent to the curve through the Q-point as shown in Fig. 1.28 will define a particular change in voltage and current that can be used to determine the ac or dynamic resistance for this region of the diode characteristics. In equation form,

$$r_d = \frac{\Delta V_D}{\Delta I_D}$$

where Δ signifies a finite change in the quantity.



Figure 1.28 determining the ac resistance at a Q-point.

1.4 DIODE EQUIVALENT CIRCUITS

An equivalent circuit is a combination of elements properly chosen to best represent the actual terminal characteristics of a device, system, or such in a particular operating region. In other words, once the equivalent circuit is defined, the device symbol can be removed from a schematic and the equivalent circuit inserted in its place without severely affecting the actual behaviour of the system. The result is often a network that can be solved using traditional circuit analysis techniques.

Piecewise-Linear Equivalent Circuit

One technique for obtaining an equivalent circuit for a diode is to approximate the characteristics of the device by straight-line segments, as shown in Fig. 1.31. The resulting equivalent circuit is naturally called the piecewise-linear equivalent circuit. It should be obvious from Fig. 1.31 that the straight-line segments do not result in an exact duplication of the actual characteristics, especially in the knee region. However, the resulting segments are sufficiently close to the actual curve to establish an equivalent circuit that will provide an excellent first approximation to the actual behaviour of the device. The ideal diode is included to establish that there is only one direction of conduction through the device, and a reverse-bias condition will result in the open-circuit state for the device. Since a silicon semiconductor diode does not reach the conduction state until V_D reaches 0.7 V with a forward bias (as shown in Fig. 1.31), a battery V_T opposing the conduction direction must appear in the equivalent circuit as shown in Fig. 1.32. The battery simply specifies that the voltage across the device must be greater than the threshold battery voltage before conduction through the device in the direction dictated by the ideal diode can be established. When conduction is established, the resistance of the diode will be the specified value of r_{av} .

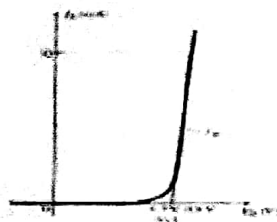


Figure 1.31 Defining the piecewise-linear equivalent circuit using straight-line segments to

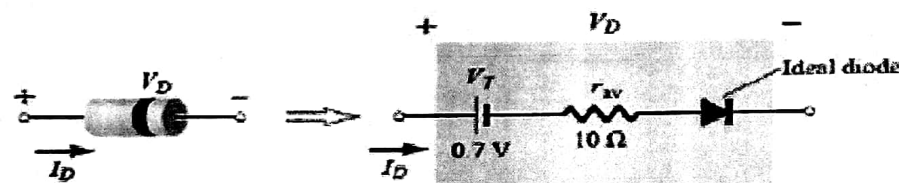


Figure 1.32 Components of the piecewise-linear equivalent circuit.

The approximate level of r_{zv} can usually be determined from a specified operating point on the specification sheet. For instance, for a silicon semiconductor diode, if $I_F \approx 10$ mA (a forward conduction current for the diode) at $V_D \approx 0.8$ V, we know for silicon that a shift of 0.7 V is required before the characteristics rise.

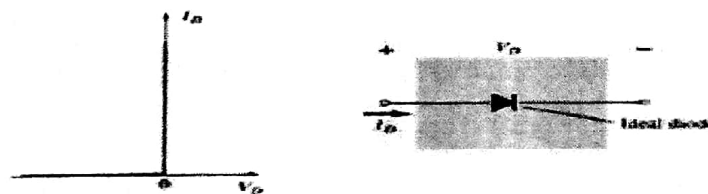
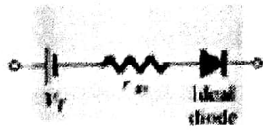
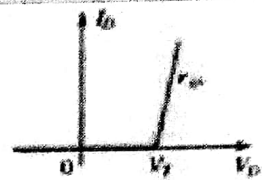
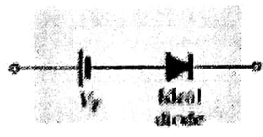
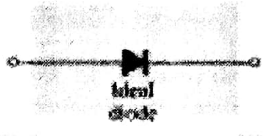
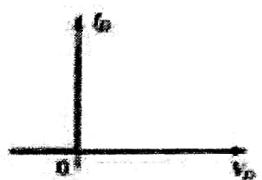


Figure 1.34 Ideal diode and its characteristics.

TABLE 1.3 Diode Equivalent Circuits (Models)			
Type	Conditions	Model	Characteristics
Piecewise-linear model			
Simplified model	$R_{\text{network}} \gg r_{\text{av}}$		
Ideal device	$R_{\text{network}} \approx r_{\text{av}}$ $E_{\text{network}} \gg V_T$		

1.5 TRANSITION AND DIFFUSION CAPACITANCE

Electronic devices are inherently sensitive to very high frequencies. Most shunt capacitive effects that can be ignored at lower frequencies because the reactance $X_C = 1/2\pi fC$ is very large (open-circuit equivalent). This, however, cannot be ignored at very high frequencies. X_C will become sufficiently small due to the high value of f to introduce a low-reactance “shorting” path. In the p-n semiconductor diode, there are two capacitive effects to be considered. In the reverse-bias region we have the transition- or depletion region capacitance (CT), while in the forward-bias region we have the diffusion (CD) or storage capacitance. Recall that the basic equation for the capacitance of a parallel-plate capacitor is defined by $C = \epsilon A/d$, where ϵ is the permittivity of the dielectric (insulator) between the plates of area A separated by a distance d . In the reverse-, bias region there is a depletion region (free of carriers) that behaves essentially like an insulator between the layers of opposite charge. Since the depletion width (d) will increase with increased reverse-bias potential, the resulting transition capacitance will decrease. The fact that the capacitance is dependent on the applied reverse-bias potential has

Fig 1.7d VI characteristics of ideal diode

application in a number of electronic systems. Although the effect described above will also be present in the forward-bias region, it is over shadowed by a capacitance effect directly dependent on the rate at which charge is injected into the regions just outside the depletion region. The capacitive effects described above are represented by a capacitor in parallel with the ideal diode, as shown in Fig. 1.38. For low- or mid-frequency applications (except in the power area), however, the capacitor is normally not included in the diode symbol.

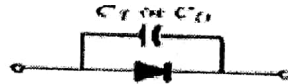


Figure 1.38 Including the effect of the transition or diffusion capacitance on the semiconductor diode.

Diode capacitances: The diode exhibits two types of capacitances transition capacitance and diffusion capacitance.

- **Transition capacitance:** The capacitance which appears between positive ion layer in n-region and negative ion layer in p-region.
- **Diffusion capacitance:** This capacitance originates due to diffusion of charge carriers in the opposite regions.

The transition capacitance is very small as compared to the diffusion capacitance.

In reverse bias transition, the capacitance is the dominant and is given by:

$$C_T = \epsilon A/W$$

where C_T - transition capacitance

A - diode cross sectional area

W - depletion region width

In forward bias, the diffusion capacitance is the dominant and is given by:

$$C_D = dQ/dV = \tau^* dI/dV = \tau^* g = \tau^* r \text{ (general)}$$

where C_D - diffusion capacitance

dQ - change in charge stored in depletion region

V - change in applied voltage

τ - time interval for change in voltage

g - diode conductance

r - diode resistance

The diffusion capacitance at low frequencies is given by the formula:

$$C_D = \tau^* g / 2 \text{ (low frequency)}$$

The diffusion capacitance at high frequencies is inversely proportional to the frequency and is given by the formula:

$$C_D = g(\tau / 2\omega)^{1/2}$$

Note: The variation of diffusion capacitance with applied voltage is used in the design of varactor.

1.6 BREAK DOWN MECHANISMS

When an ordinary P-N junction diode is reverse biased, normally only very small reverse saturation current flows. This current is due to movement of minority carriers. It is almost independent of the voltage applied. However, if the reverse bias is increased, a point is reached when the junction breaks down and the reverse current increases abruptly. This current could be large enough to destroy the junction. If the reverse current is limited by means of a suitable series resistor, the power dissipation at the junction will not be excessive, and the device may be operated continuously in its breakdown region to its normal (reverse saturation) level. It is found that for a suitably designed diode, the breakdown voltage is very stable over a wide range of reverse currents. This quality gives the *breakdown diode* many useful applications as a *voltage reference source*.

The critical value of the voltage, at which the breakdown of a P-N junction diode occurs is called the *breakdown voltage*. The breakdown voltage depends on the width of the depletion region, which, in turn, depends on the doping level. The junction offers almost zero resistance at the breakdown point.

There are two mechanisms by which breakdown can occur at a reverse biased P-N junction :

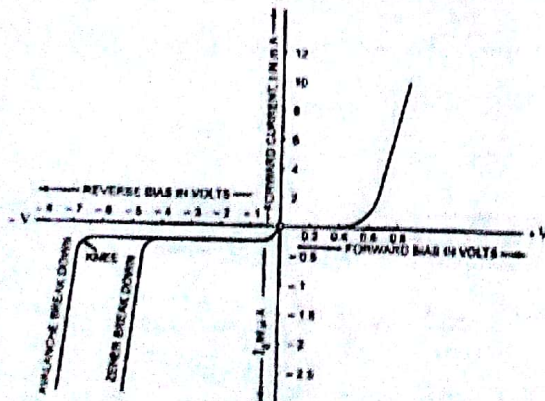
1. *avalanche breakdown* and
2. *Zener breakdown*.

Avalanche breakdown and

The minority carriers, under reverse biased conditions, flowing through the junction acquire a kinetic energy which increases with the increase in reverse voltage. At a sufficiently high reverse voltage (say 5 V or more), the kinetic energy of minority carriers becomes so large that they knock out electrons from the covalent bonds of the semiconductor material. As a result of collision, the liberated electrons in turn liberate more electrons and the current becomes very large leading to the breakdown of the crystal structure itself. This phenomenon is called the avalanche breakdown. *The breakdown region is the knee of the characteristic curve. Now the current is not controlled by the junction voltage but rather by the external circuit.*

Zener breakdown

Under a very high reverse voltage, the depletion region expands and the potential barrier increases leading to a very high electric field across the junction. The electric field will break some of the covalent bonds of the semiconductor atoms leading to a large number of free minority carriers, which suddenly increase the reverse current. This is called the Zener effect. The breakdown occurs at a particular and constant value of reverse voltage called the breakdown voltage, it is found that Zener breakdown occurs at electric field intensity of about 3×10^7 V/m.



Either of the two (Zener breakdown or avalanche breakdown) may occur independently, or both of these may occur simultaneously. Diode junctions that breakdown below 5 V are caused by Zener effect. Junctions that experience breakdown above 5 V are caused by avalanche effect. Junctions that breakdown around 5 V are usually caused by combination of two effects.

Expression for the Barrier Potential

It is known that the change in concentration ~~induced~~ induces the voltage & is given by,

$$V_{bi} = V_T \ln \left(\frac{p_1}{p_2} \right)$$

At junction, there is a abrupt change in the concentration of holes ~~disappears~~ from p_p to p_n .

$$\text{So } p_1 = p_p \propto N_A \text{ \& } p_2 = p_n$$

Substituting above we get,

$$V_{bi} = V_T \ln \left(\frac{N_A}{p_n} \right)$$

$$\text{w.k.T. } n_n \cdot p_n = n_i^2$$

$$p_n = \frac{n_i^2}{n_n}$$

$$\therefore V_{bi} = V_T \ln \left[\frac{N_A}{\left(\frac{n_i^2}{n_n} \right)} \right]$$

$$\text{But } n_n \approx N_D$$

$$\therefore V_{bi} = V_T \ln \left[\frac{N_A N_D}{n_i^2} \right]$$

This eq gives the values of Junction Potential. It can be seen from this eq that the Junction potential depends on voltage equivalent of temp i.e V_T & the amount of doping of N-side & P-side i.e N_D & N_A .

Diode Equation

$$I = I_0 \left[e^{V/\eta V_T} - 1 \right]$$

I_0 = Reverse Saturation Current

V = Applied Voltage

η = 1 for Ge
2 for Si

V_T = Voltage equivalent of Temp

$$V_T = kT$$

when unbiased

$V = 0$ hence we get

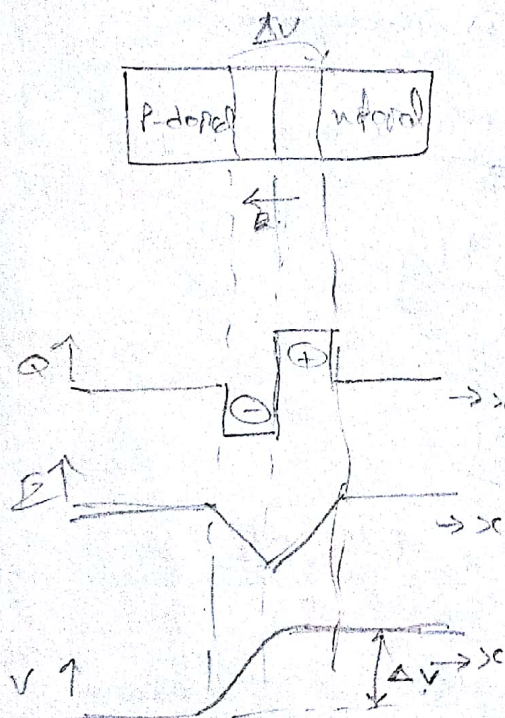
$$I = I_0 [e^0 - 1] = 0A$$

Thus there is no current through diode when unbiased
if both sides of diode are of δ divided by cross-section
area A of the junction

$$\frac{I}{A} = \frac{I_0}{A} [e^{V/\eta V_T} - 1]$$

$$J = J_0 [e^{V/\eta V_T} - 1] \text{ A/cm}^2$$

The space charge density in the depletion region is shown in Fig. The charge density to the left of the PN Junction is $-ve$, whereas the charge density to the right of the PN Junction is $+ve$. This creates an electric field configuration shown in Fig. The electric field in the depletion region establishes a potential barrier V which obstructs the flow of electrons & holes across the junction. Since the no. of holes in the p-side is equal to the no. of acceptor ions & the no. of electrons in n-side is equal to the no. of donor ions, we can write $p = N_A$ & $n = N_D$. If q is charge of holes & electrons the charge density in the depletion region may be described as



$$\rho = -qN_A, \quad 0 > x > x_1$$

$$\rho = +qN_D, \quad x_2 > x > 0$$

$$\rho = 0 \text{ else where.}$$

where ρ is space charge density.

Poisson's equation gives the relation between potential & charge density in a given region. Thus

$$\frac{d^2V}{dx^2} = -\frac{\rho}{\epsilon} \rightarrow \text{① } \epsilon \text{ is permittivity}$$

Applying the above equation to the p-side of the Junction, we get

$$\frac{d^2V}{dx^2} = \frac{qN_A}{\epsilon} \rightarrow \text{②}$$

Integrating twice, we get

$$V = \frac{qN_A x^2}{2\epsilon} + Cx + D \rightarrow \text{③}$$

where C & D are the constants of integration.

In eq (3) we get

$$V = \frac{qNAx^2}{2\epsilon_0} + Cx + D$$

$$0 = 0 + 0 + D$$

$$\therefore D = 0$$

For $x < x_1$ on the p-side, the potential is constant, so that

$$\frac{dV}{dx} = 0 \text{ at } x = x_1 \text{ Hence}$$

$$\frac{dV}{dx} = \frac{qNAx}{\epsilon} + C$$

$$0 = \frac{qNAx_1}{\epsilon} + C$$

$$\therefore C = -\frac{qNAx_1}{\epsilon}$$

Substitute D & C values in eq (3) therefore.

$$V = \frac{qNAx^2}{2\epsilon} - \frac{qNAx_1}{\epsilon} \cdot x + 0$$

$$V = \frac{qNA}{\epsilon} \left[\frac{x^2}{2} - x_1 x \right]$$

At $V = V_1$ & $x = x_1$ we have

$$V_1 = \frac{qNA}{\epsilon} \left[\frac{x_1^2}{2} - x_1^2 \right]$$

$$= \frac{qNA}{\epsilon} \left[\frac{x_1^2 - 2x_1^2}{2} \right] = \frac{qNA}{\epsilon} \cdot \frac{-x_1^2}{2}$$

$$\boxed{V_1 = -\frac{qNA}{2\epsilon} \cdot x_1^2} \rightarrow (4)$$

Similarly if we apply above procedure to the n-side we get

$$\boxed{V_2 = \frac{qND}{2\epsilon} \cdot x_2^2} \rightarrow (5)$$

Therefore, the total built-in potential of the contact potential is V_0 , where

$$V_0 = V_2 - V_1$$

$$= \frac{qND}{2\epsilon} x_2^2 + \frac{qNA}{2\epsilon} x_1^2$$

$$V_0 = \frac{q}{2\epsilon} \left[N_D x_2 + N_A x_1 \right] \rightarrow (6) \quad \text{www.FirstRanker.com}$$

we know the fact that the +ve charge on the n-side must be equal in magnitude to the -ve charge on the p-side for the neutral specimen. Hence,

$$N_A x_1 = + N_D x_2$$

$$\therefore x_1 = + \frac{N_D}{N_A} x_2 \rightarrow (8) \quad x_2 = + \frac{N_A}{N_D} x_1 \rightarrow (7)$$

For getting x_1 value, put eq (7) in eq (6)

$$\begin{aligned} \therefore V_0 &= \frac{q}{2\epsilon} \left[N_A x_1^2 + N_D \cdot \left(\frac{N_A}{N_D} x_1 \right)^2 \right] \\ &= \frac{q}{2\epsilon} \left[N_A x_1^2 + N_D \cdot \left[\frac{N_A^2 x_1^2}{N_D^2} \right] \right] \\ &= \frac{q}{2\epsilon} \left[N_A x_1^2 + \frac{N_A^2}{N_D} x_1^2 \right] \\ &= \frac{q}{2\epsilon} \left[x_1^2 \left(N_A + \frac{N_A^2}{N_D} \right) \right] \\ &= \frac{q}{2\epsilon} \left[x_1^2 N_A \left(1 + \frac{N_A}{N_D} \right) \right] \end{aligned}$$

$$x_1^2 = \left[\frac{2 \epsilon V_0}{q N_A \left(1 + \frac{N_A}{N_D} \right)} \right]$$

$$x_1 = \left[\frac{2 \epsilon V_0}{q N_A \left(1 + \frac{N_A}{N_D} \right)} \right]^{1/2} \rightarrow (9)$$

where '-' sign indicates -ve charge on p-side.

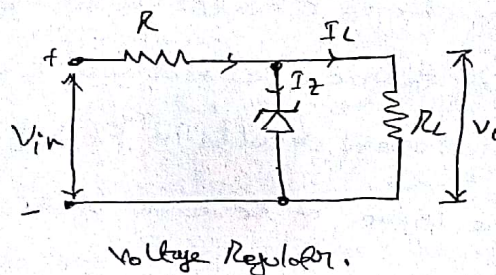
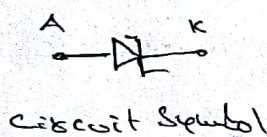
$$\text{Similarly } x_2 = \left[\frac{2 \epsilon V_0}{q N_D \left(1 + \frac{N_D}{N_A} \right)} \right]^{1/2} \rightarrow (10)$$

The total depletion width $w = x_2 - x_1$ & hence

$$w = \left[\frac{2 \epsilon V_0}{q} \cdot \left(\frac{N_A + N_D}{N_A N_D} \right) \right]^{1/2} \rightarrow (11)$$

In addition to PN Junction Diode, other types of diodes are also manufactured for specific applications. These special diodes are two terminal devices with their doping levels carefully selected to give the desired characteristics.

When the reverse voltage reaches breakdown voltage in normal PN junction diode, the current through the junction & the power dissipated at the junction will be high. Such an operation is destructive and the diode gets damaged. Whereas diodes can be designed with adequate power dissipation capabilities to operate in the breakdown region. One such a diode is known as Zener diode. Zener diode is heavily doped than the ordinary diode.



From the V-I characteristics of the Zener diode it is found that the operation of Zener diode is same as that of ordinary PN diode under forward-biased condition, whereas under reverse-biased condition, breakdown of the junction occurs. The breakdown voltage depends upon the amount of doping. If the diode is heavily doped, depletion layer will be thin and, consequently, breakdown occurs at lower reverse voltage & further, the breakdown voltage is sharp, whereas a lightly doped diode has a higher breakdown voltage. Thus breakdown voltage can be selected with the amount of doping.

The sharp increasing current under breakdown conditions are due to the following two mechanisms.

- (i) Avalanche breakdown
- (ii) Zener breakdown

As the applied reverse bias increases, the field across the junction increases correspondingly. Thermally generated carriers while traversing the junction acquire a large amount of kinetic energy from this field. As a result the velocity of these carriers increases. These electrons disrupt covalent bond by colliding with immobile ions and create new electron-hole pairs. These new carriers again acquire sufficient energy from the field & collide with other immobile ions thereby generating further electron-hole pairs. This process is cumulative in nature & results in generation of avalanche of charge carriers within a short time. This mechanism of carrier generation is known as Avalanche multiplication. This process results in flow of large amount of current at the same value of reverse bias.

Zener Break down

When the P & N regions are heavily doped, direct rupture of covalent bonds takes place because of the strong electric fields, at the junction of PN diode. The new electron-hole pairs so created increase the reverse current in a reverse biased PN diode. The increase in current takes place at a constant value of reverse bias typically below 6V for heavily doped diodes. As a result of heavy doping of P & N regions, the depletion region width becomes very small and for an applied voltage of 6V or less, the field across the depletion region becomes very high, of the order of 10^7 V/cm, making conditions suitable for Zener break down. For lightly doped diodes, Zener break down voltage becomes high & breakdown is then predominantly by avalanche multiplication.

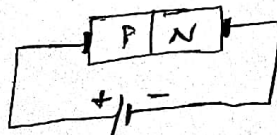
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voltage & Avalanche breakdown occurs for higher breakdown voltage. Such diodes are normally called Zener diodes.

Applications

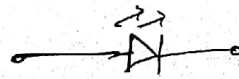
- Zener diodes can be used as a voltage regulator.

Light Emitting Diode (LED).

The Light Emitting Diode (LED) is a PN junction device which emits light when forward biased, by a phenomenon called electroluminescence. In all semiconductor PN Junctions, some of the energy will be radiated as heat and some in the form of photons. In Silicon & Germanium, greater percentage of energy is given out in the form of heat & the emitted light is insignificant. In other materials such as Gallium phosphide (GaP) & Gallium arsenide phosphide (GaAsP), the no. of photons of light energy emitted is sufficient to create a visible light source. Here the charge carrier recombination takes place when electrons from the N-side cross the junction & recombine with the holes on the P-side.



④ LED under forward bias



⑤ Circuit Symbol

LED under forward bias and its symbol are shown in fig ④ & ⑤ respectively. When an LED is forward biased, the electrons and holes move towards the junction & recombination takes place. As a result of recombination, the electrons lying in the conduction bands of N-region fall into the holes lying in the valence band of a P-region. The difference of energy between

of light energy. Each recombination causes radiation of light energy. Light is generated by recombination of electrons and holes whereby their excess energy is transferred to an emitted photon. The brightness of the emitted light is directly proportional to the forward bias current.

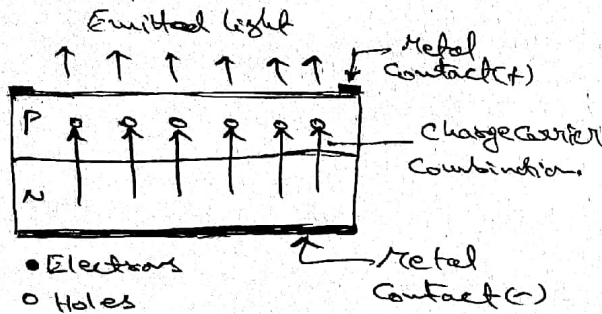


Fig. 1 Recombinations & Emission of Light

Fig. 1 shows the basic structure of an LED showing recombination of carriers & emission of light. Here, an n-type layer is grown on a substrate & a p-type is deposited on it by diffusion.

Since carrier recombination takes place in the p-layer, it is kept uppermost. The metal anode connectors are made at the outer edges of the p-layer so as to allow more central surface area for the light to escape.

LEDs are manufactured with domed lenses in order to reduce the reabsorption problem. A metal (gold) film is applied to the bottom of the substrate for reflecting as much light as possible to the surface of the device & also to provide cathode connection. LEDs are always encased to protect their delicate wires.

LEDs radiate different colours such as red, green, yellow, orange, blue & white. Some of the LEDs emit infrared (invisible) light also. The wave length of emitted light depends on the energy gap of the material. Hence, the colour of the emitted light depends on the type of material used is given as follows.

- Gallium arsenide (GaAs) - Infrared
- Gallium phosphide (GaP) - Red & green
- Gallium arsenide phosphide (GaAsP) - red & yellow

LCDs are used in similar applications where LEDs are used. The applications of LCDs are display of numeric & alphanumeric characters in segmental & dot matrix displays.

Liquid crystals have been called "the fourth state of matter" (after solids, liquids & gases) because they have certain crystal properties normally found in solids, yet flow like liquids. Unlike LEDs & other electroluminescent devices, LCDs do not generate light energy, but simply alter or control existing light to make selected areas appear bright or dark.

Advantages.

- a low power consumption than the LED, typically of the order of μW where as LED mW .
- Low power consumption requirement has made it compatible with VLSI integrated logic circuit.
- Low cost good contrast.

Disadvantages.

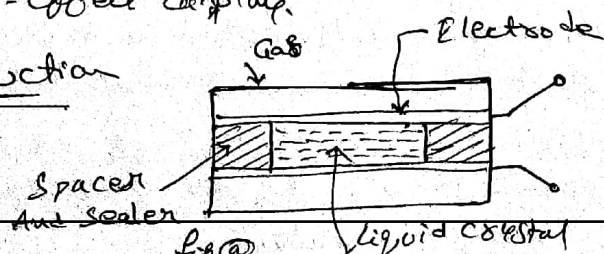
- Additional requirement of light source
- A limited temperature range of operation (0°C to 60°C)
- Low reliability
- Short operating life
- Poor visibility in low ambient lighting.
- Slow speed & the need for an ac drive.

There are two basic ways in which liquid crystals are used for controlling properties of light & thereby change its appearance. Accordingly, there are two types of LCD displays.

(i) Dynamic Scattering Display

(ii) Field-effect display.

Construction



The basic construction of a liquid crystal display is depicted in fig ①. A thin layer of liquid crystal, 10-20 μm thick, is sandwiched between two glass sheets. To enable application of an electric field across the crystal, a transparent conductive material is deposited on the inside surface of each glass sheet. The conductive material forms the electrodes to which an external voltage is connected when it is desired to change the molecular structure of the liquid crystal. The electrodes are etched in patterns or in individually accessible segments that can be selectively energized to develop a desired display, similar to a seven segment LED display. Materials used to form the electrodes include stannic oxide (SnO_2) & indium oxide (In_2O_3).

LED	LCD
1. Needs more power (10-250 mW per digit)	1. Essentially acts as a capacitor and needs very less power (10-20 mW)
2. Because of high power need, it needs external interface circuitry when driven from ICs	2. Can be driven directly from IC chips.
3. Operating voltage range is 1.5 to 5V d.c	3. Operating voltage range is 3-20V a.c.
4. Life time is about 100,000 hours	4. Life time is limited to 50,000 hours due to its chemical degradation.
5. Good brightness level.	5. Moderate brightness level.
6. Temp. range for operation is -45°C to 85°C	6. Temp range for operation is -20 to 60°C .
7. Emits light in red, orange, yellow, green, blue & white	7. Invisible in darkness - needs external or internal light source.
8. Viewing angle is 150°	8. Viewing angle is 100°
9. Font style: 7-16 segments, dot matrix	9. Font style: 7-16 segments, dot matrix.

Silicon photodiode is light sensitive device, also called photo detector, which converts light signals into electrical signals. The construction & symbol of a photo diode are shown in fig (a). The diode is made of a semiconductor p-n junction kept in a sealed plastic or glass casing. The cover is so designed that the light rays are allowed to fall on one surface across the junction. The remaining sides of the casing are painted to restrict the penetration of light rays. A lens permits light to fall on the junction. When light falls on the reverse biased p-n photodiode junction, hole-electron pairs are created. The movement of these hole-electron pairs in a properly connected circuit results in current flow. The magnitude of the photo current depends on the no. of charge carriers generated & hence, on the illumination of the diode element. This current is also affected by the frequency of the light falling on the junction of the photodiode. The magnitude of the current under large reverse bias is given by

$$I = I_s + I_0 (1 - e^{-V/\eta V_T})$$

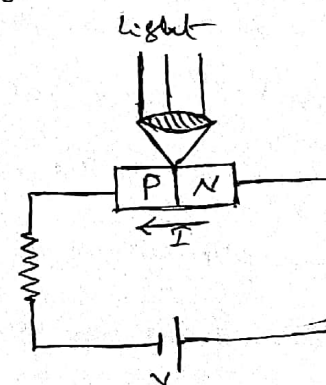
where I_0 = reverse saturation current

I_s = short-circuit current which is proportional to the light intensity

V = voltage across the diode

V_T = volt equivalent of temp.

η = parameter 1 for Ge & 2 for Si



fig(a) construction



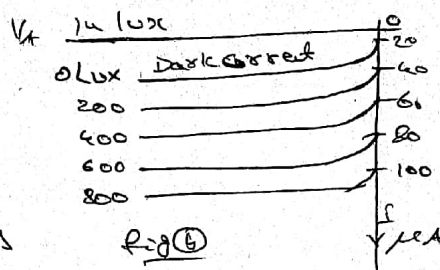
fig(b) circuit symbol

The characteristics of a photo diode are shown in fig (c). The reverse current increases in direct proportion to the level of illumination. Even when no light is applied,

dark current, flowing through the device. Germanium has a higher dark current than Silicon, but it also has a higher level of reverse current.

Applications:

- used as light detectors
- Demodulators & Encoders
- Used in optical communication system
- High Speed Counting & Switching circuits.
- Used in computer card punching & tapes
- light operated switches
- Sound track films & electric control circuits.

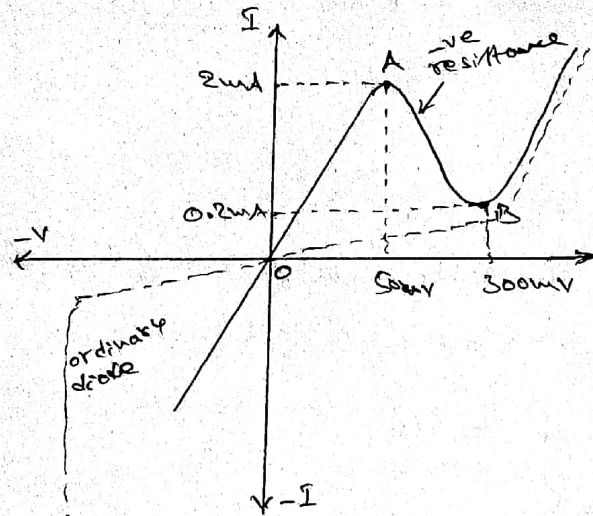


Tunnel diode

The tunnel or Esaki diode is thin-junction diode which exhibits negative resistance under low forward bias conditions.

An ordinary pn junction diode has an impurity concentration of about 1 part in 10^8 . With this amount of doping the width of the depletion layer is of the order of 5 microns. This potential barrier restrains the flow of carriers from the majority carrier side to the minority carrier side. If the concentration of impurity atoms is greatly increased to the level of 1 part in 10^3 , the device characteristics are completely changed. The width of the junction barrier varies inversely as the square root of the impurity concentration and therefore, is reduced from 5 microns to less than $100 \text{ \AA}$ (10^{-8} m). This thickness is only about $1/50$ th of the wavelength of visible light. For such thin potential energy barriers, the electrons will penetrate through

the junction rather than submounting them. This quantum mechanical behaviour is referred to as tunneling & hence these high-impurity-density PN junction devices are called tunnel diodes.



fig@ V-I characteristic of tunnel diode

The V-I characteristic for a typical germanium tunnel diode is shown in fig@. It is seen that at first forward current rises sharply as applied voltage is increased, where it would have risen slowly for an ordinary PN junction diode. Also, reverse current is much larger for comparable back bias

than in other diodes due to the thinness of the junction. The interesting portion of the characteristics starts at the point A on the curve, i.e. the peak voltage. As the forward bias is increased beyond this point, the forward current drops & continues to drop until point B is reached. This is the valley voltage. At B, the current starts to increase once again & does so very rapidly as bias is increased further. Beyond this point, characteristic resembles that of an ordinary diode. Apart from the peak voltage & valley voltage, the other two parameters normally used to specify the diode behaviour are the peak current & the peak-to-valley current ratio, which are 2mA & 10 respectively, as shown. The V-I characteristic of the tunnel diode illustrates that it exhibits dynamic resistance between A & B.

The equivalent circuit of the tunnel diode when biased in the -ve resistance region is as shown in fig@. In the circuit, R_s is the series resistance & L_s is the series inductance which may be ignored except at highest

is thus reduced to parallel combination of the function Capacitance C_j & -ve resistance $-R_n$. Typical values of Capacitance the circuit components are $R_s = 6\Omega$, $L_s = 0.1nH$, $C_j = 0.6pF$ & $R_n = 75\Omega$.

Applications.

1. Tunnel diode is used as an ultra-high speed switch with switching speed of the order of ns or ps.
2. As logic memory storage device
3. As microwave oscillator.
4. In relaxation oscillator circuit.
5. As an amplifier.

Advantages.

1. Low noise
2. Easy of operation
3. High speed
4. Low power.

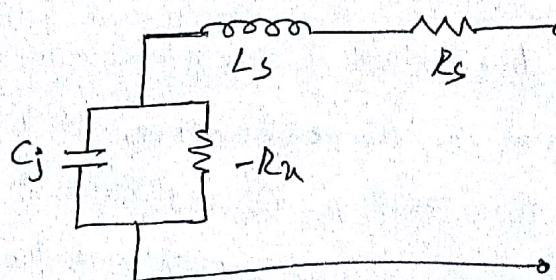


Fig (6): Equivalent circuit of tunnel diode

Disadvantages.

1. Voltage range over which it can be operated is 1V less.
2. Being a two terminal device, there is no isolation between the i/p & o/p circuit.

Varactor Diode

The varactor, also called a varicap, tuning or voltage variable capacitor diode, is a junction diode with a small impurity dose at its junction, which has the useful property that its junction or transition capacitance is easily varied electronically.

When any diode is reverse biased, a depletion region is formed, as seen in fig (a). The larger the reverse bias applied across the diode, the width of the depletion layer " w " becomes wider. Conversely, by decreasing the reverse bias voltage, the depletion region width " w " becomes narrower. This depletion region is devoid of majority carriers and acts like an insulator preventing conduction between the N & P regions of the diode, just like a dielectric, which separates the two plates of a capacitor. The varactor diode with its symbol is shown in fig (b).

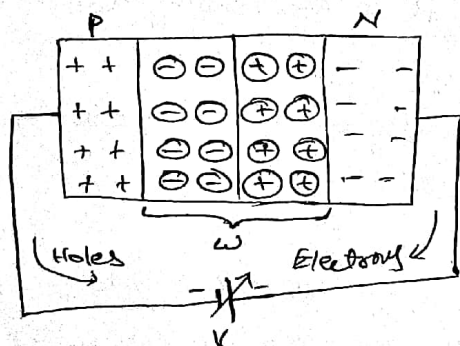


fig (a) Depletion region in a reverse biased PN Junction

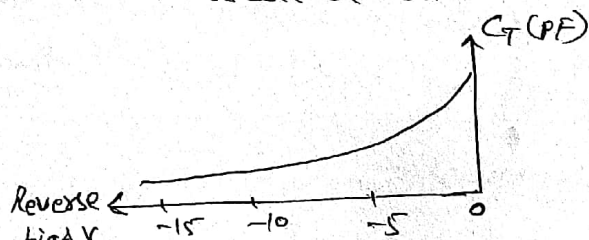
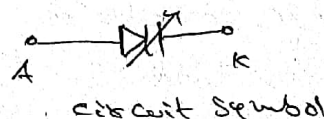


fig (b) ~~circuit~~ characteristics of varactor diode.

As the capacitance is inversely proportional to the distance between the plates ($C_T \propto 1/w$), the transition capacitance C_T varies inversely with the reverse voltage as shown in fig (b). Consequently, an increase in reverse bias voltage will result in an increase in the depletion region width and a subsequent decrease in transition capacitance C_T . At zero volt, the varactor depletion region " w " is small and capacitance is large at approximately 600 pF. when the reverse bias voltage across

The varactor diodes are used in

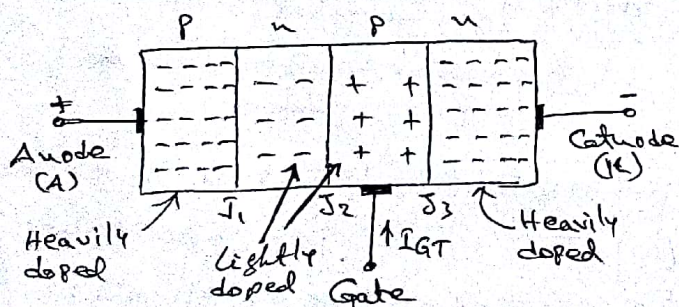
- FM radio & TV receivers
- AFC circuits
- Self adjusting bridge circuits
- adjustable band pass filters.
- Tuning of LC resonant circuit in re-wave frequency multipliers.
- In very low noise re-wave parametric amplifiers.

Silicon Control Rectifier (SCR)

The SCR is an unidirectional device and like diode, it allows to flow current in only one direction. But unlike diode, it has a built in feature to switch 'on' & 'off'. The switching of SCR is controlled by the additional input called 'gate' and biasing conditions. This switching property of SCR allows to control the 'ON' periods of the SCR thus controlling average power delivered to the load.

It can be used as a rectifier element like diode to convert a.c signals to d.c signals.

construction.



Fig@ Construction of SCR

The outer p-layer is called "anode" while outer n layer is called "cathode". Middle p-layer is called "gate". The three terminals are taken out respectively from these three layers as shown in the fig@. Anode must be +ve w.r.t Cathode to forward bias the SCR. But this is not sufficient criterion to turn SCR ON. To make it ON, a current is to be passed through

The SCR is a four layer p-n-p-n device where p & n layers are alternately arranged. The outer layers are heavily doped. There are three p-n junctions called J_1 , J_2 & J_3 .

The outer p-layer is called "anode" while outer n layer is

the gate terminal denoted as I_{GT} . Thus it is a constant operated device.

Three types of Constructions are used to manufacture SCR,

- (i) planar type
- (ii) Mesa type
- (iii) Press pack type

(i) Planar type

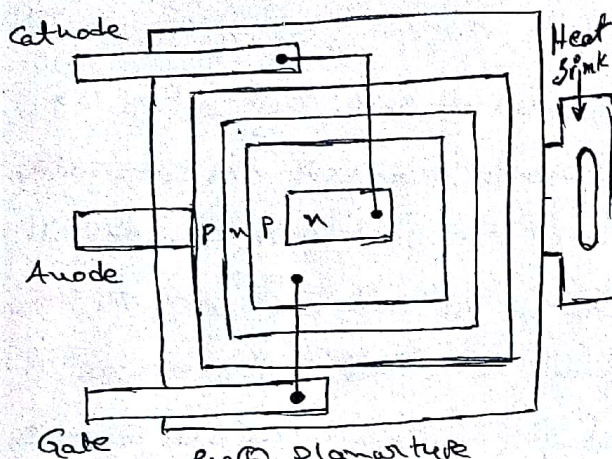


fig 6 Planar type

The construction is used for low current SCRs. In this type, all the p-n junctions come to the same surface on the cathode side. This is shown in the fig 6. All the junctions are diffused in this type of construction. The disadvantage of this type is more silicon per ampere current is required. The advantage of this type is that

the mass production is possible and large no of SCRs can be manufactured with uniform characteristics.

(ii) Mesa type:

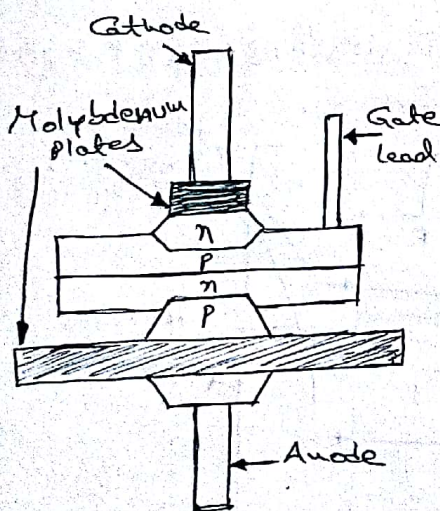


fig 7: Mesa type Construction.

In this construction, the junction J_2 is diffused while the outer layers are alloyed to it. This is shown in the fig 7. To handle the large currents, the molybdenum or tungsten plates are braced to p-n-p-n silicon pellet. This provides the additional mechanical strength. When SCR is on, the area around the gate starts the conduction first. But in this construction, area around the gate is small hence this construction is not suitable for high di/dt ratings.

(iii) Press type. This construction is used for the center gate SCRs, the entire circular area around the gate takes part in the initial condition hence di/dt capability of such SCRs is large. This is shown in the fig 8. The construction is used for high power SCRs. A silicon wafer is used to make such a high power SCR. This type of

Instruction provides double sided cooling arrangement
 www.FirstRanker.com www.FirstRanker.com
 which is necessary for high power SCRs.

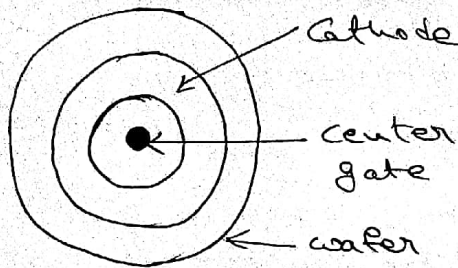


Fig (a) Power pack type
 Construction

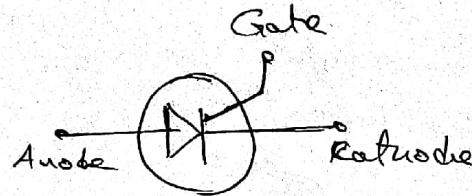


Fig (c) Symbol of SCR

The fig (c) shows the symbol of SCR. The I_{GT} is the gate trigger current required to make the SCR on. Basically it is a diode symbol, with a third terminal gate connected to it. Thus the basic material used for the SCR fabrication is Silicon whose reverse current is very small compared to the other important semiconductor material germanium. The SCR conducts only in one direction & not only that the point at which it starts conduction can be controlled. Due to this, the device is called "Silicon Controlled Rectifier" (SCR).

Operation of SCR : The operation of SCR is divided into 2 categories.

① when gate is open:

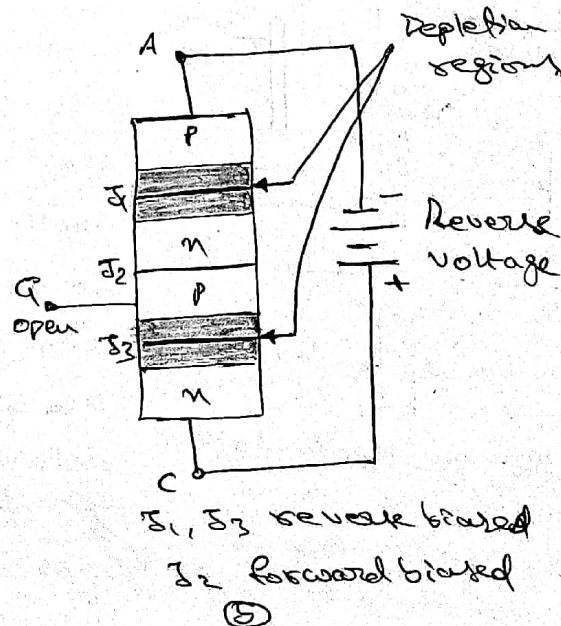
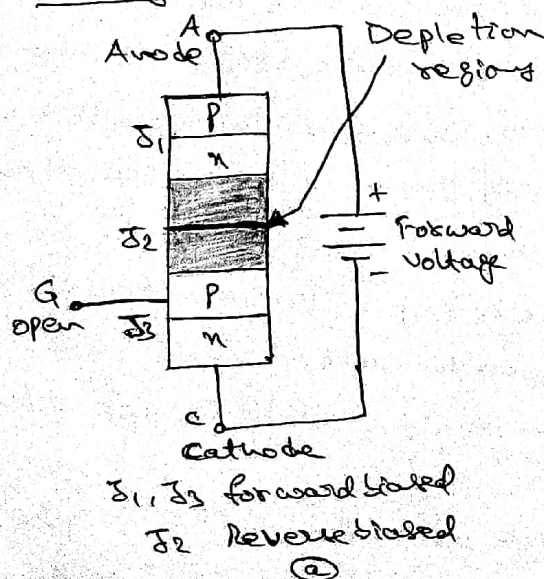


Fig (d) Operation of SCR when gate is open

Consider that the anode is +ve w.r.t. Cathode & gate is open. The Junctions J_1 & J_3 are forward biased and Junction J_2 is reverse biased. There is depletion region around J_2 & only leakage current flows which is negligible small. Practically the SCR is said to be "OFF". This is called "forward blocking state" of SCR & voltage applied to anode & Cathode with anode +ve is called "forward voltage". This is shown in the fig (10).

With gate open, if Cathode is made +ve w.r.t anode, the junctions J_1 , J_3 become reverse biased and J_2 forward biased. Still the current flowing is leakage current, which can be neglected as it is very small. The voltage applied to make Cathode +ve is called reverse voltage and SCR is said to be in "reverse blocking state". This is shown in fig (11).

In forward blocking state, if the forward voltage is increased, the current remains almost zero upto certain limit. At a particular value, the reverse biased junction J_2 breaks down & SCR conducts heavily. This voltage is called "forward breakover voltage V_{BO} " of SCR. In such condition SCR is said to be ON or triggered.

(ii) When gate is closed:

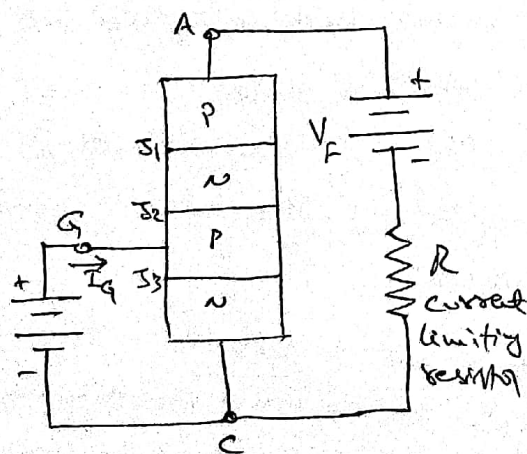


Fig (12): When gate is closed

Consider that the voltage is applied between gate and Cathode when the SCR is in forward blocking state. The gate is made +ve w.r.t to the Cathode. The electrons from n-type Cathode which are majority in number, cross the Junction J_3 to reach to +ve of battery.

While holes from p-type move towards the -ve of battery, this constitutes the gate current. This current increases the anode current as some of the electrons cross Junction J_2 . As anode current increases, more electrons cross the Junction J_2 & the anode current further increases.

Due to regenerative action, within short time, the junction J_2 breaks & SCR conducts heavily. The connections are shown in the fig 8. The resistance R is required to limit the current. Once the SCR conducts, the gate loses its control.

Characteristics of SCR

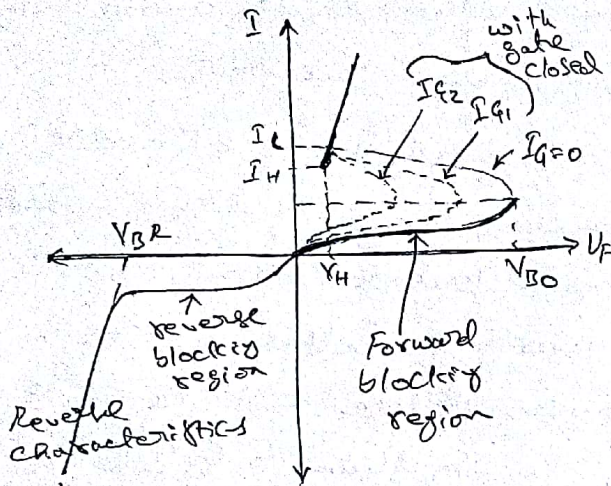


Fig 8: Characteristics of SCR

The characteristics are divided into two categories.

1. Forward characteristics.
2. Reverse characteristics.

1. Forward Characteristics:

It shows a forward blocking region, when $I_G = 0$. It also shows that when forward voltage increases upto V_{BO} , the SCR turns on & high current results. The drop across

SCR reduces suddenly which is now the ohmic drop in the four layers. The current must be limited only by the external resistance in series with the device.

It also shows that, if gate terminal is used then as gate current increases, less voltage is required to turn on the SCR.

If the forward current falls below the level of the "holding current" I_H , then depletion region begins to develop around J_2 & device goes into the forward blocking region.

When SCR is turned on from off state, the resulting forward current is called "latching current" I_L . The latching current is slightly higher than the holding current.

2. Reverse Characteristics. If the anode to Cathode voltage is reversed, then the device enters into the reverse blocking region. The current is negligibly small & practically neglected. If the reverse voltage is increased, similar to the diode, at a particular value avalanche breakdown occurs & a large current flows through the device. This is called "reverse breakdown" & the voltage at which this happens is called "reverse breakdown voltage" V_{BR} .

A unijunction transistor (UJT) is a device which does not belong to the ~~BJT~~ family but is used to turn on ^{SCRs} ~~off~~.

CONSTRUCTION:

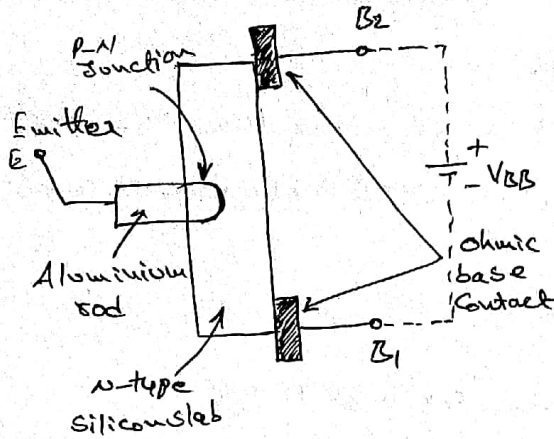


Fig ① Construction of UJT

It is a 3 terminal device, having

two bases. It consists of a slab of lightly doped n type silicon material. The two base contacts are attached to both the ends of this n-type surface. These are denoted as B_1 & B_2 respectively. A p-type material is used to form a p-n junction at the boundary of the aluminium rod & n-type silicon

slab. The third terminal called emitter (E) is taken out from this p-type material. The n-type is slightly doped while p type is heavily doped. The basic construction is shown in the fig ①.

As n type is lightly doped, it provides high sensitivity & p type as heavily doped, provides low sensitivity.

The symbolic representation of UJT is shown in the fig ②. The emitter is shown by an arrow which is at an angle to the vertical line representing n-type material. This arrow indicates the direction of flow of conventional current when the UJT is forward biased.

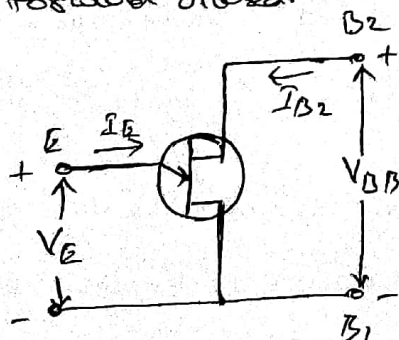


Fig ② Symbol of UJT

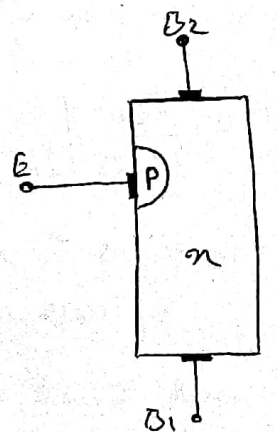


Fig ③ Structure

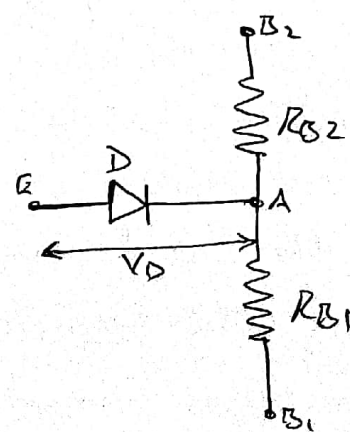


Fig ④ Equivalent circuit

Fig 1 shows the basic structure of BJT while the Fig 2 shows the equivalent circuit of BJT.

The internal resistances of the two bases are represented as R_{B1} & R_{B2} . In the actual construction, the terminal E is closer to B_2 as compared to B_1 . Hence resistance R_{B1} is more than the resistance R_{B2} . The p-n junction is represented by a normal diode with V_D as the ~~drop~~ ^{drop} across it.

When the emitter diode is not conducting then the resistance between the two bases B_1 & B_2 is called "interbase resistance" denoted as R_{BB} .

$$\therefore R_{BB} = R_{B1} + R_{B2}$$

Its value ranges between $4k\Omega$ to $12k\Omega$.

Intrinsic Standoff Ratio (η)

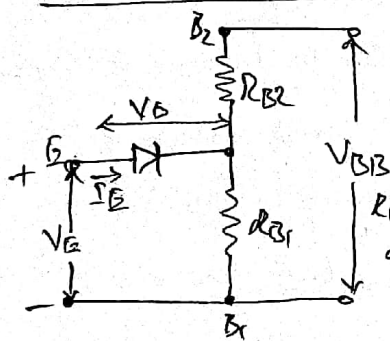


Fig 2

Consider BJT as shown in Fig 2 to which supply V_{BB} is connected. with $I_E = 0$ i.e. emitter diode is not conducting.

$$R_{BB} = R_{B1} + R_{B2}$$

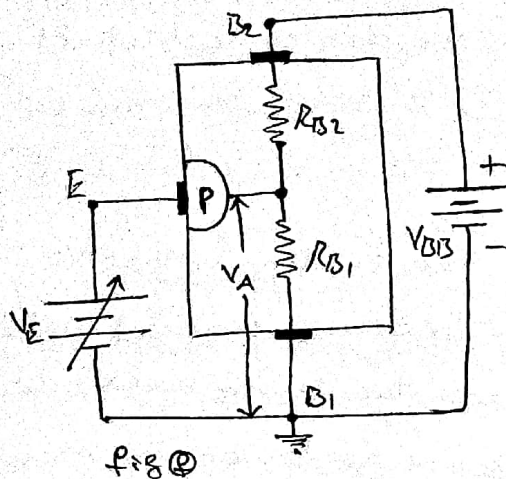
Then the voltage drop across R_{B1} can be obtained by using potential divider rule.

$$V_{RB1} = \frac{R_{B1} V_{BB}}{R_{B1} + R_{B2}} = \eta V_{BB} \dots \text{when } I_E = 0$$

$$\text{Then } \eta = \text{Intrinsic Standoff ratio} = \frac{R_{B1}}{R_{B1} + R_{B2}} \bigg|_{I_E = 0}$$

$$\eta = \frac{R_{B1}}{R_{BB}} \bigg|_{I_E = 0}$$

The typical range of η is from 0.5 to 0.8. The voltage V_{RB1} is called "Intrinsic Standoff Voltage" because it keeps the emitter diode reversed biased for all the emitter voltages less than V_{RB1} .



while operating as a UJT, the supply V_{BB} is applied between B_2 and B_1 , while the variable emitter voltage V_E is applied across the emitter terminals. This arrangement is shown in fig 8(a). Let us see the effect of change in V_E . The potential of A is decided by η and is equal to ηV_{BB} .

Case 1: $V_E < V_A$

As long as V_E is less than V_A , the P-N junction is reverse biased. Hence emitter current I_E will not flow. Thus UJT is said to be OFF.

Case 2: $V_E > V_P$

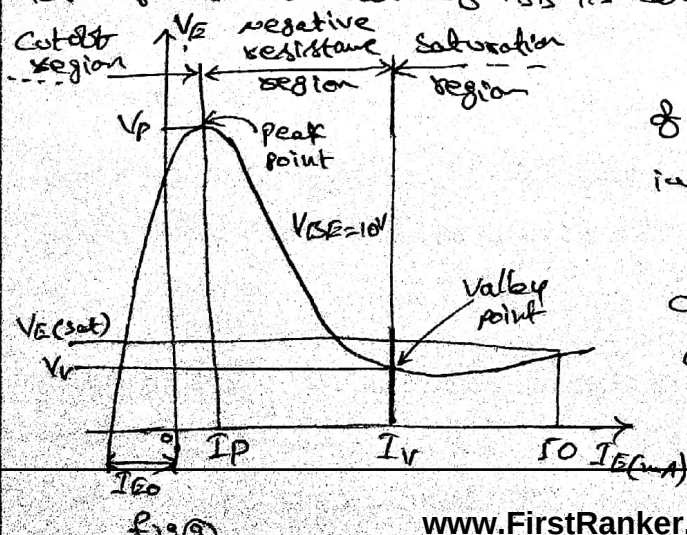
The diode drop V_D is generally between 0.3 to 0.7V. Hence we can write,

$$V_P = V_A + V_D = \eta V_{BB} + V_D$$

When V_E becomes equal to or greater than V_P the P-N junction becomes forward biased & current I_E flows. The UJT is said to be ON.

UJT CHARACTERISTICS

The graph of emitter current against voltage plotted for a particular value of V_{BB} is called the characteristics of UJT.



For a particular fixed value of V_{BB} such characteristics shown in fig 8(b).

The characteristics can be divided into three main regions, which are:

- (i) Cutoff-region
- (ii) negative resistance region
- (iii) Saturation region.

The emitter voltage V_E is less than V_p and the p-n junction is reverse biased. A small amount of reverse saturation current I_{EO} flows through the device, which is negligible small of the order of μA . This condition remain till the peak point.

2. Negative Resistance region: when the emitter voltage V_E becomes equal to V_p the p-n junction becomes forward biased and I_E starts flowing. The voltage across the device decreases in this region, though the current through the device increases. Hence the region is called negative resistance region. This decreases the resistance R_B . This region is stable and used in many applications. This region continues till valley point.

3. Saturation region: Increase in I_E further valley point current I_v drives the device in the saturation region. The voltage corresponding to valley point is called "valley point voltage" denoted as V_v . In this region further decrease in voltage does not take place. The characteristic is similar to that of a Semiconductor diode, in this region.

The active region i.e. negative resistance region, the holes, which are large in number of p-side, get injected into n-side. This causes increase in free electrons in the n-type slab. This increases the conductivity i.e. decreases the resistivity. Hence the resistance R_B decreases in this region.

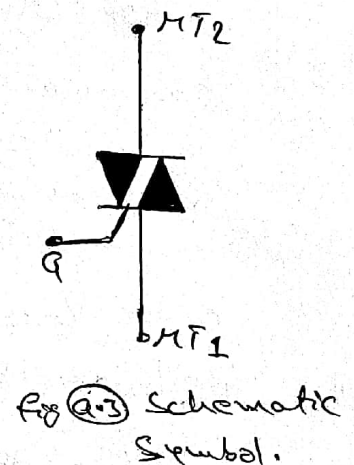
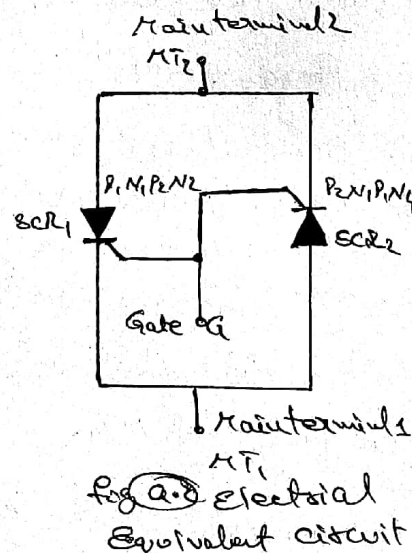
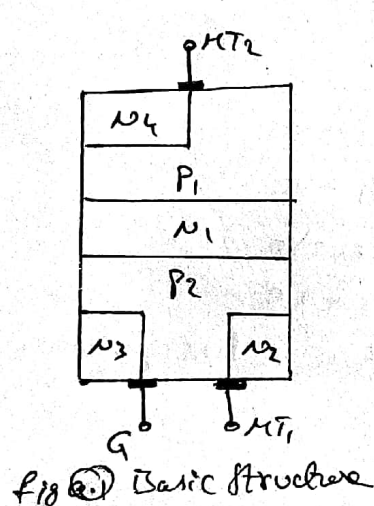
As the V_{BE} increases, the potential V_p corresponding to peak point will increase.

~

"Triac" is an abbreviation for three terminal ac switch. 'Tri' indicates that the device has three terminals and 'ac' indicates that the device controls alternating current or can conduct in either direction.

Unlike the SCR, the triac conducts in either direction when turned on. The triac also differs from the SCR in that either a +ve or -ve gate signal triggers it into conduction. Thus the triac is a three terminal, four layer, bidirectional, semiconductor device that controls ac power. Because of its bidirectional conduction property, the triac is widely used in the field of power electronics for control purposes. Triacs of 16kW rating are readily available in the market.

Construction



Triac incorporates two SCRs connected in inverse parallel with a common gate terminal in a single chip device. The arrangement of triac is shown in Fig (a.1). As seen, it has six doped regions. The gate terminal G makes ohmic contacts with both the N & P materials. This permits trigger pulse of either polarity to start conduction. Electrical equivalent circuit & schematic symbol are shown in Fig (a.2) & Fig (a.3) respectively. Since the triac is a bilateral device, the term "anode" & "cathode" has no meaning, & therefore, terminals are designated as main terminal 1 (MT1), main terminal 2 (MT2) & gate (G).

To avoid confusion, it has become common practice to specify all voltages & currents using MT_1 as the reference.

Characteristics

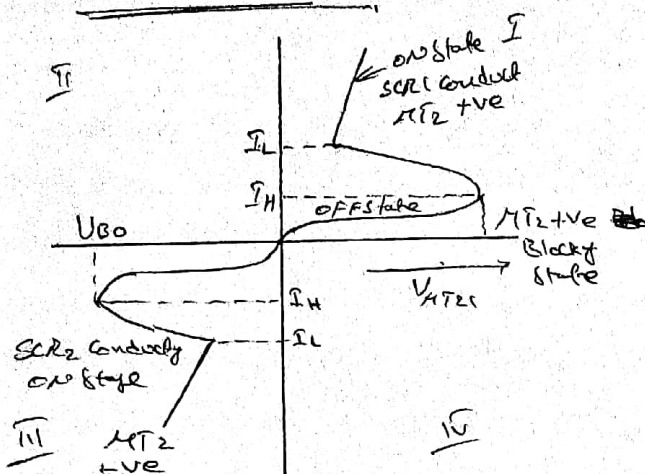


Fig 5: V-I characteristics of a Triac

Typical V-I characteristics of a triac are shown in Fig 5. The triac has ~~no~~ ON & OFF state characteristics similar to SCR but now the characteristic is applicable to both +ve & -ve voltages. This is expected because triac consists of two SCRs connected in parallel but opposite in directions.

MT_2 is +ve with MT_1 in the first quadrant & it is -ve in the III quadrant. The gate triggering may occur in any of the following four modes.

Quadrant I operation: V_{MT2} +ve; V_G +ve

Quadrant II operation: V_{MT2} +ve; V_G -ve

Quadrant III operation: V_{MT2} -ve; V_G -ve

Quadrant IV operation: V_{MT2} -ve; V_G +ve

where V_{MT2} & V_G are the voltages of terminal MT_2 & gate with respect to terminal MT_1 .

The device, when starts conducting permits a very heavy amount of current to flow through it. This large inrush of current must be restricted by employing external resistance, otherwise the device may get damaged.

The gate is the control terminal of the device. By applying proper signal to the gate, the firing angle of the device can be controlled. The circuits used in the gate for triggering the device are called the gate triggering circuits. These triggering circuits usually generate trigger pulses for firing the device. The triggering pulse should be of sufficient magnitude & duration so that firing of the device is assured. Usually, a duration of 35 μ s is sufficient for sustaining the firing of the device.

A diac is a two terminal bidirectional avalanche diode which can be switched from off-state to the on-state for either polarity of the applied voltage. This is just like a triac without gate terminal, as shown in fig (a). Its equivalent circuit is a pair of inverted four layer diodes. Two schematic symbols are shown in fig (b).

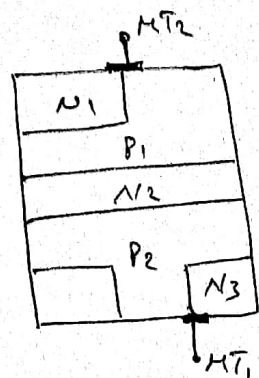


fig (a) Basic structure

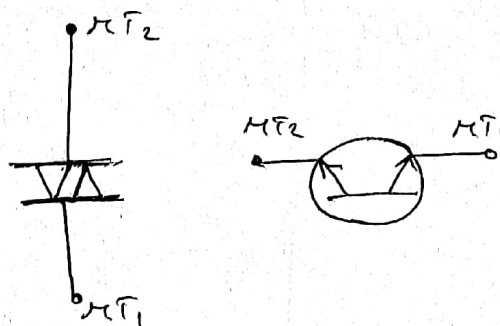


fig (b) schematic symbols.

Construction

A diac is a P-N-P-N structured four layer, two terminal semiconductor device, as shown in fig (a). MT_2 & MT_1 are the two main terminals of the device. There is no control terminal in this device. From the diagram, a diac unlike a diode, resembles a bipolar junction transistor (BJT) but with the following exceptions.

- (i) there is no terminal attached to the middle layer (base).
- (ii) the three regions are nearly identical in size.
- (iii) the doping level at the two end p-layers is the same so that the device gives symmetrical switching characteristics for either polarity of the applied voltage.

Characteristics

Volt-ampere (V-I) characteristics of a diac is shown in fig (c). It resembles the English letter Z because of the symmetrical switching characteristics for either polarity of the applied voltage. The diac acts like an open circuit until its switching or breakover voltage is exceeded.

As the forward bias conductance until its current reduces toward zero (below the level of the holding current of the device.) The diac, because of its peculiar construction, does not switch sharply into a low voltage condition at a low current level like the SCR or triac.

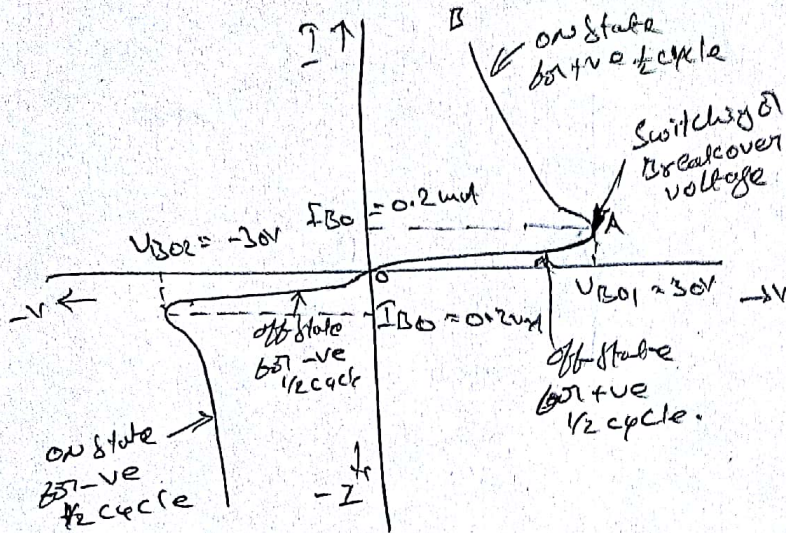


Fig (c): V-I characteristics of a DIAC

Instead, once it goes into conduction, the diac maintains an almost continuous -ve resistance characteristics i.e voltage decreases with the increase in current. This means that, unlike the SCR or the triac, the diac cannot be expected to maintain a low (on) voltage drop until its current falls below a holding current level.

UNIT – 3

RECTIFIERS AND FILTERS

UNIT III

RECTIFIERS & FILTERS:

3.0 INTRODUCTION

For the operation of most of the electronics devices and circuits, a d.c. source is required. So it is advantageous to convert domestic a.c. supply into d.c.voltages. The process of converting a.c. voltage into d.c. voltage is called as rectification. This is achieved with i) Step-down Transformer, ii) Rectifier, iii) Filter and iv) Voltage regulator circuits.

These elements constitute d.c. regulated power supply shown in the fig 1 below.

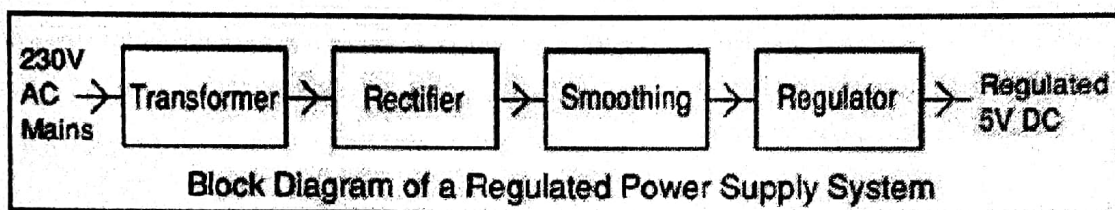


fig1 . Block diagram of Regulated D.C. Power Supply

- ✓ Transformer – steps down 230V AC mains to low voltage AC.
- ✓ Rectifier – converts AC to DC, but the DC output is varying.
- ✓ Smoothing – smooth the DC from varying greatly to a small ripple.
- ✓ Regulator – eliminates ripple by setting DC output to a fixed voltage.

The block diagram of a regulated D.C. power supply consists of step-down transformer, rectifier, filter, voltage regulator and load. An ideal regulated power supply is an electronics circuit designed to provide a predetermined d.c. voltage V_o which is independent of the load current and variations in the input voltage and temperature. If the output of a regulator circuit is a AC voltage then it is termed as voltage stabilizer, whereas if the output is a DC voltage then it is termed as voltage regulator.

3.1 RECTIFIER:

Any electrical device which offers a low resistance to the current in one direction but a high resistance to the current in the opposite direction is called rectifier. Such a device is capable of converting a sinusoidal input waveform, whose average value is zero, into a unidirectional Waveform, with a non-zero average component. A rectifier is a device, which converts a.c. voltage (bi-directional) to pulsating d.c. voltage (Unidirectional).

Characteristics of a Rectifier Circuit:

Any electrical device which offers a low resistance to the current in one direction but a high resistance to the current in the opposite direction is called rectifier. Such a device is capable of converting a sinusoidal input waveform, whose average value is zero, into a unidirectional waveform, with a non-zero average component.

A rectifier is a device, which converts a.c. voltage (bi-directional) to pulsating d.c.. Load currents: They are two types of output current. They are average or d.c. current and RMS currents.

Average or DC current: The average current of a periodic function is defined as the area of one cycle of the curve divided by the base.

It is expressed mathematically as

i) Average value/dc value/mean value = $\frac{\text{Area over one period}}{\text{Total time period}}$

$$V_{dc} = \frac{1}{T} \int_0^T V d(\omega t)$$

ii) Effective (or) R.M.S current:

The effective (or) R.M.S. current squared of a periodic function of time is given by the area of one cycle of the curve, which represents the square of the function divided by the base.

$$V_{rms} = \sqrt{\frac{1}{T} \int_0^T V^2 d(\omega t)}$$

iii) Peak factor:

It is the ratio of peak value to Rms value

$$\text{Peak factor} = \frac{\text{peakvalue}}{\text{rmsvalue}}$$

iv) Form factor:

It is the ratio of Rms value to average value

$$\text{Form factor} = \frac{\text{Rmsvalue}}{\text{averagevalue}}$$

v) Ripple Factor (Γ) : It is defined as ration of R.M.S. value of a.c. component to the d.c. component in the output is known as "Ripple Factor".

$$\Gamma = \frac{V_{ac}}{V_{dc}}$$

$$V_{ac} = \sqrt{V_{rms}^2 - V_{dc}^2}$$

vi) Efficiency (η):

It is the ratio of d.c output power to the a.c. input power. It signifies, how efficiently the rectifier circuit converts a.c. power into d.c. power.

$$\eta = \frac{o / p \text{ power}}{i / p \text{ power}}$$

vii) Peak Inverse Voltage (PIV):

It is defined as the maximum reverse voltage that a diode can withstand without destroying the junction.

viii) Transformer Utilization Factor (UTF):

The d.c. power to be delivered to the load in a rectifier circuit decides the rating of the Transformer used in the circuit. So, transformer utilization factor is defined as

$$TUF = \frac{P_{dc}}{P_{ac(rated)}}$$

ix) % Regulation:

The variation of the d.c. output voltage as a function of d.c. load current is called regulation. The percentage regulation is defined as

$$\% \text{ Regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} * 100$$

For an ideal power supply, % Regulation is zero.

3.2 CLASSIFICATION OF RECTIFIERS:

Using one or more diodes in the circuit, following rectifier circuits can be designed.

- 1) Half - Wave Rectifier
- 2) Full - Wave Rectifier
- 3) Bridge Rectifier

3.2.1) HALF-WAVE RECTIFIER:

A Half - wave rectifier as shown in fig 2 is one, which converts a.c. voltage into a pulsating voltage using only one half cycle of the applied a.c. voltage.

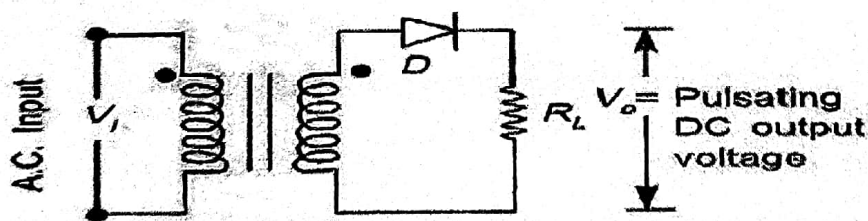


fig 2 Basic structure of Half-Wave Rectifier

The a.c. voltage is applied to the rectifier circuit using step-down transformer-rectifying element i.e., p-n junction diode and the source of a.c. voltage, all connected in series. The a.c. voltage is applied to the rectifier circuit using step-down transformer

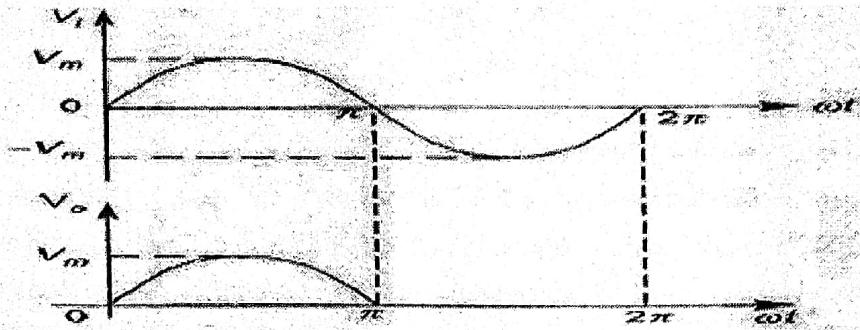


fig 3 Input and output waveforms of a Half wave rectifier

$$V = V_m \sin(\omega t)$$

The input to the rectifier circuit, Where V_m is the peak value of secondary a.c. voltage.

Operation:

For the positive half-cycle of input a.c. voltage, the diode D is forward biased and hence it conducts. Now a current flows in the circuit and there is a voltage drop across R_L . The waveform of the diode current (or) load current is shown in **fig 3**.

For the negative half-cycle of input, the diode D is reverse biased and hence it does not Conduct. Now no current flows in the circuit i.e., $i=0$ and $V_o=0$. Thus for the negative half- cycle no power is delivered to the load.

Analysis:

In the analysis of a HWR, the following parameters are to be analyzed.

1. DC output current
2. DC Output voltage
3. R.M.S. Current
4. R.M.S. voltage
5. Rectifier Efficiency (η)
6. Ripple factor (γ)
7. Peak Factor

8. % Regulation
9. Transformer Utilization Factor (TUF)
10. form factor
11. o/p frequency

Let a sinusoidal voltage V_i be applied to the input of the rectifier.

Then $V = V_m \sin(\omega t)$ Where V_m is the maximum value of the secondary voltage. Let the diode be idealized to piece-wise linear approximation with resistance R_f in the forward direction i.e., in the ON state and $R_r (= \infty)$ in the reverse direction i.e., in the OFF state. Now the current 'i' in the diode (or) in the load resistance R_L is given by $V = V_m \sin(\omega t)$

i) AVERAGE VOLTAGE

$$V_{dc} = \frac{1}{T} \int_0^T V d(\omega t)$$

$$V_{dc} = \frac{1}{T} \int_0^{2\pi} V(\alpha) d\alpha$$

$$V_{dc} = \frac{1}{2\pi} \int_{\pi}^{2\pi} V(\alpha) d\alpha$$

$$V_{dc} = \frac{1}{2\pi} \int_0^{\pi} V_m \sin(\omega t) d(\omega t)$$

$$V_{dc} = \frac{V_m}{\pi}$$

ii). AVERAGE CURRENT:

$$I_{dc} = \frac{I_m}{\pi}$$

iii) RMS VOLTAGE:

$$V_{rms} = \sqrt{\frac{1}{T} \int_0^T V^2 d(\omega t)}$$

$$V_{rms} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} (V_m \sin(\omega t))^2 d(\omega t)}$$

$$V_{rms} = \frac{V_m}{2}$$

IV) RMS CURRENT

V) PEAK FACTOR

$$I_{rms} = \frac{I_m}{\pi}$$

$$\text{Peak factor} = \frac{\text{peakvalue}}{\text{rmsvalue}}$$

$$\text{Peak Factor} = \frac{V_m}{(V_m / 2)}$$

$$\text{Peak Factor} = 2$$

vi) FORM FACTOR

$$\text{Form factor} = \frac{\text{Rmsvalue}}{\text{averagevalue}}$$

$$\text{Form factor} = \frac{(V_m / 2)}{V_m / \pi}$$

$$\text{Form Factor} = 1.57$$

vii) Ripple Factor:

$$\Gamma = \frac{V_{ac}}{V_{dc}}$$

$$V_{ac} = \sqrt{V_{rms}^2 - V_{dc}^2}$$

$$\Gamma = \frac{\sqrt{V_{rms}^2 - V_{dc}^2}}{V_{ac}}$$

$$\Gamma = \sqrt{\frac{V_{rms}^2}{V_{dc}^2} - 1}$$

$$\Gamma = 1.21$$

viii) Efficiency (η):

$$\eta = \frac{o / p_{power}}{i / p_{power}} * 100$$

$$\eta = \frac{P_{ac}}{P_{dc}} * 100$$

$$\eta = 40.8$$

ix) Transformer Utilization Factor (TUF):

The d.c. power to be delivered to the load in a rectifier circuit decides the rating of the transformer used in the circuit. Therefore, transformer utilization factor is defined as

$$TUF = \frac{P_{dc}}{P_{ac(rated)}}$$

$$TUF = 0.286.$$

The value of TUF is low which shows that in half-wave circuit, the transformer is not fully utilized.

If the transformer rating is 1 KVA (1000VA) then the half-wave rectifier can deliver

$$1000 \times 0.287 = 287 \text{ watts to resistance load.}$$

x) Peak Inverse Voltage (PIV):

It is defined as the maximum reverse voltage that a diode can withstand without destroying the junction. The peak inverse voltage across a diode is the peak of the negative half-cycle. For half-wave rectifier, PIV is V_m .

DISADVANTAGES OF HALF-WAVE RECTIFIER:

1. The ripple factor is high.
2. The efficiency is low.
3. The Transformer Utilization factor is low.

Because of all these disadvantages, the half-wave rectifier circuit is normally not used as a power rectifier circuit.

3.2.2) FULL WAVE RECTIFIER:

A full-wave rectifier converts an ac voltage into a pulsating dc voltage using both half cycles of the applied ac voltage. In order to rectify both the half cycles of ac input, two diodes are used in this circuit. The diodes feed a common load R_L with the help of a center-tap transformer. A center-tap transformer is the one, which produces two sinusoidal waveforms of same magnitude and frequency but out of phase with respect to the ground in the secondary winding of the transformer. The full wave rectifier is shown in the fig 4 below

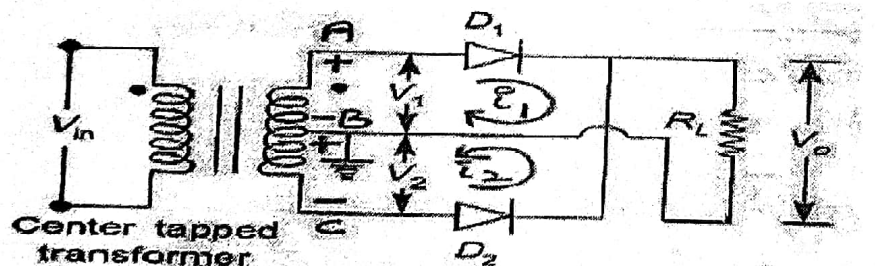


fig 4 Full-Wave Rectifier.

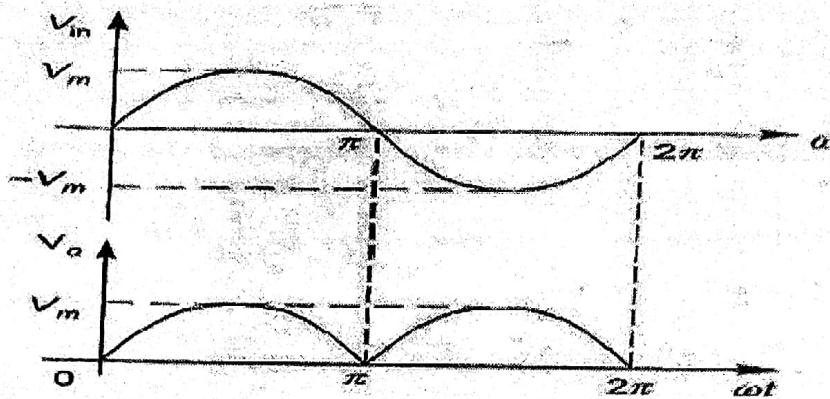


Fig. 5 input and output waveforms of Fullwave rectifier

Fig. 5 shows the input and output wave forms of the ckt.

During positive half of the input signal, anode of diode D_1 becomes positive and at the same time the anode of diode D_2 becomes negative. Hence D_1 conducts and D_2 does not conduct. The load current flows through D_1 and the voltage drop across R_L will be equal to the input voltage.

During the negative half cycle of the input, the anode of D_1 becomes negative and the anode of D_2 becomes positive. Hence, D_1 does not conduct and D_2 conducts. The load current flows through D_2 and the voltage drop across R_L will be equal to the input voltage. It is noted that the load current flows in the both the half cycles of ac voltage and in the same direction through the load resistance.

i) AVERAGE VOLTAGE

$$V_{dc} = I_{dc} \cdot R_L = \frac{2I_m}{\pi} \cdot R_L \quad \text{We know } I_m = \frac{V_m}{R_s + R_f + R_L}$$

$$\therefore V_{dc} = \frac{2V_m R_L}{\pi(R_s + R_f + R_L)}$$

$$\text{If } (R_s + R_f) \ll R_L$$

$$V_{dc} = \frac{2V_m}{\pi} = 0.637 V_m$$

ii) AVERAGE CURRENT

$$\begin{aligned}
 \frac{1}{2\pi} \int_0^{2\pi} i d\theta &= \frac{1}{2\pi} \int_0^{2\pi} I_m \sin \theta d\theta \\
 I_{dc} &= \frac{I_m}{2\pi} \left[\int_0^{\pi} \sin \theta d\theta - \int_{\pi}^{2\pi} \sin \theta d\theta \right] \\
 &= \frac{I_m}{2\pi} [(-2)(-2)] \\
 &= \frac{I_m}{2\pi} \cdot 4 = \frac{2I_m}{\pi} = 0.637 I_m
 \end{aligned}$$

$$I_{dc} = 0.637 I_m$$

$$\therefore I_{dc} \text{ FWR} = 2 I_{dc} \text{ HWR}$$

iii) RMS VOLTAGE:

$$V_{rms} = \sqrt{\frac{1}{T} \int_0^T V^2 d(\omega t)}$$

$$V_{rms} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} (V_m \sin(\omega t))^2 d(\omega t)}$$

$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

IV) RMS CURRENT

$$I_{rms} = \frac{2I_m}{\pi}$$

V) PEAK FACTOR

$$\text{Peak factor} = \frac{\text{peakvalue}}{\text{rmsvalue}}$$

$$\text{Peak Factor} = \frac{V_m}{(V_m / 2)}$$

$$\text{Peak Factor} = 2$$

vi) FORM FACTOR

$$\text{Form factor} = \frac{\text{Rms value}}{\text{average value}}$$

$$\text{Form factor} = \frac{(V_m / \sqrt{2})}{2V_m / \pi}$$

$$\text{Form Factor} = 1.11$$

vii) Ripple Factor:

$$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

for FWR,

$$I_{rms} = \frac{I_m}{\sqrt{2}} \quad \& \quad I_{DC} = \frac{2I_m}{\pi}$$

$$\therefore \gamma_{FWR} = \sqrt{\left(\frac{I_m / \sqrt{2}}{2I_m / \pi}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{\pi}{2\sqrt{2}}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{3.1416}{2 \times 1.414}\right)^2 - 1} = 0.483$$

viii) Efficiency (η):

$$\eta = \frac{o / \text{power}}{i / \text{power}} * 100$$

$$\eta = \frac{P_{dc}}{P_{ac}} \times 100\%$$

$$\text{For FWR, } P_{dc} = I_{dc}^2 \cdot R_L = \left(\frac{2}{\pi} \cdot I_m \right)^2 \cdot R_L$$

$$P_{ac} = I_{rms}^2 (R_f + R_s + R_L) = \left(\frac{I_m}{\sqrt{2}} \right)^2 (R_f + R_s + R_L)$$

$$\eta = \frac{\frac{I_m^2 \cdot 4}{\pi^2} \cdot R_L}{\frac{I_m^2}{2} \cdot (R_f + R_s + R_L)}$$

$$\text{If } (R_f + R_s) \ll R_L$$

$$\eta = \frac{4}{\pi^2} \cdot \frac{2}{1} = \frac{8}{\pi^2} = 0.812 = 81.2\%$$

ix) Transformer Utilization Factor (TUF):

The d.c. power to be delivered to the load in a rectifier circuit decides the rating of the transformer used in the circuit. So, transformer utilization factor is defined as

$$TUF = \frac{P_{dc}}{P_{ac(rated)}}$$

$$\text{a) TUF (Secondary)} = \frac{P_{dc} \text{ delivered to load}}{AC \text{ power rating of transformer secondary}}$$

$$\text{b) Since both the windings are used } TUF_{FWR} = 2 TUF_{HWR} = 2 \times 0.287 = 0.574$$

$$\text{c) TUF primary} = \text{Rated efficiency} = \frac{P_{dc}}{P_{ac}} \times 100 = 81.2\%$$

$$\text{d) Average} = \frac{0.812 + 0.574}{2} = 0.693$$

x) Peak Inverse Voltage (PIV):

It is defined as the maximum reverse voltage that a diode can withstand without destroying the junction. The peak inverse voltage across a diode is the peak of the negative half-cycle. For half-

wave rectifier, PIV is $2V_m$

xi) % Regulation

$$\text{Voltage regulation} = \frac{I_{dc}(R_s + R_f)}{\frac{2V_m}{\pi} - I_{dc}(R_f + R_s)}$$

Advantages

- 1) Ripple factor = 0.482 (against 1.21 for HWR)
- 2) Rectification efficiency is 0.812 (against 0.405 for HWR)
- 3) Better TUF (secondary) is 0.574 (0.287 for HWR)
- 4) No core saturation problem

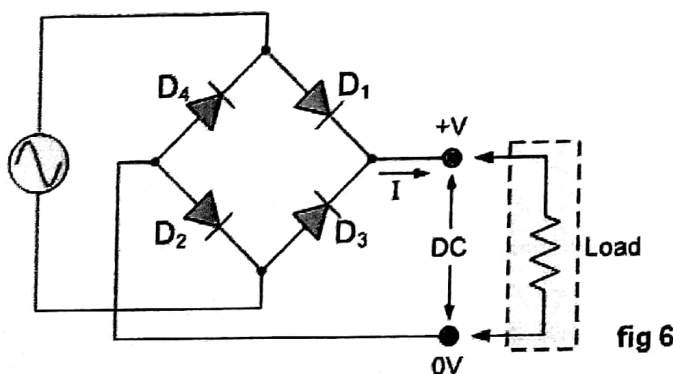
Disadvantages:

- 1) Requires center tapped transformer.

3.2.3) BRIDGE RECTIFIER.

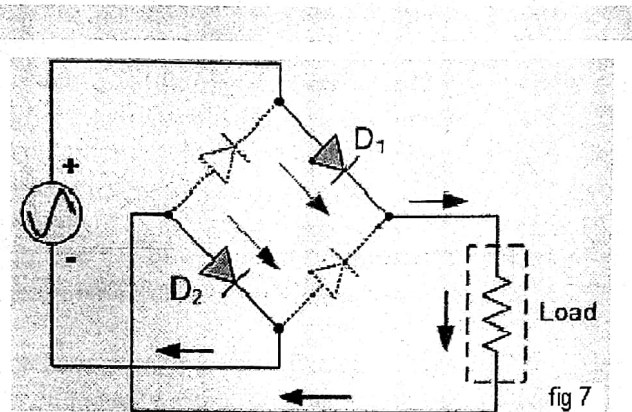
Another type of circuit that produces the same output waveform as the full wave rectifier circuit above, is that of the **Full Wave Bridge Rectifier**. This type of single phase rectifier uses four individual rectifying diodes connected in a closed loop "bridge" configuration to produce the desired output. The main advantage of this bridge circuit is that it does not require a special centre tapped transformer, thereby reducing its size and cost. The single secondary winding is connected to one side of the diode bridge network and the load to the other side as shown below.

The Diode Bridge Rectifier



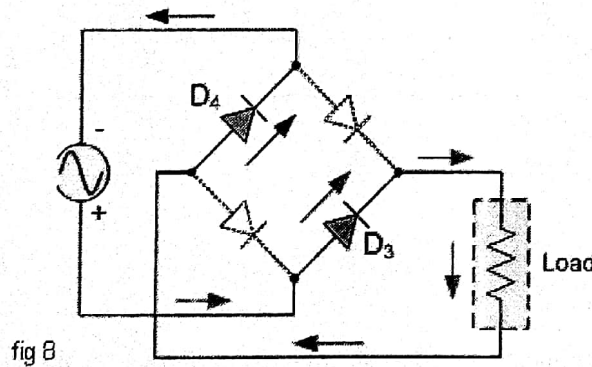
The four diodes labelled D_1 to D_4 are arranged in "series pairs" with only two diodes conducting current during each half cycle. During the positive half cycle of the supply, diodes D_1 and D_2 conduct in series while diodes D_3 and D_4 are reverse biased and the current flows through the load as shown below (fig 7).

The Positive Half-cycle



The Negative Half-cycle

During the negative half cycle of the supply, diodes D_3 and D_4 conduct in series (fig 8), but diodes D_1 and D_2 switch "OFF" as they are now reverse biased. The current flowing through the load is the same direction as before.



As the current flowing through the load is unidirectional, so the voltage developed across the load is also unidirectional the same as for the previous two diode full-wave rectifier, therefore the average DC voltage across the load is $0.637V_{max}$. However in reality, during each half cycle the current flows through two diodes instead of just one so the amplitude of the output voltage is two voltage drops ($2 \times 0.7 = 1.4V$) less than the input V_{MAX} amplitude. The ripple frequency is now twice the supply frequency (e.g. 100Hz for a 50Hz supply)

Therefore, the following expressions are same as that of full wave rectifier.

a) Average current $I_{dc} = \frac{2I_m}{\pi}$

b) RMS current $I_{rms} = \frac{I_m}{\sqrt{2}}$

c) DC output voltage (no.load) $V_{DC} = \frac{2V_m}{\pi}$

d) Ripple factor $\gamma = 0.482$

e) Rectification efficiency $\eta = 0.812$

f) DC output voltage full load.

$$= V_{DCFL} = \frac{2V_m}{\pi} - I_{dc}(R_s + 2R_f); \quad \text{i.e., less by one diode loss.}$$

TUF of both primary & secondary are 0.812 therefore TUF overall is 0.812 (better than FWR with 0.693)

Comparison:

Sl No.	Parameter	HWR	FWR	BR
1	No. of diodes	1	2	4
2	PIV of diodes	V_m	$2V_m$	V_m
3	Secondary voltage (rms)	V	$V/0.7$	V
4	DC output voltage at no load	$\frac{V_m}{\pi} = 0.318 V_m$	$\frac{2V_m}{\pi} = 0.636 V_m$	$\frac{2V_m}{\pi} = 0.636 V_m$
5	Ripple factor γ	1.21	0.482	0.482
6	Ripple frequency	f	$2f$	$2f$
7	Rectification efficiency η	0.406	0.812	0.812
8	TUF	0.287	0.693	0.812

3.3 FILTERS

The output of a rectifier contains dc component as well as ac component. Filters are used to minimize the undesirable ac i.e., ripple leaving only the dc component to appear at the output.

Some important filters are:

1. Inductor filter
2. Capacitor filter

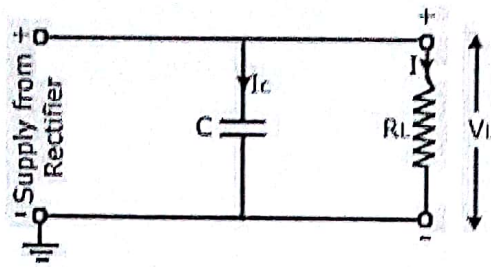
3. LC or L section filter
4. CLC or Π -type filter

3.3.1 CAPACITOR FILTER

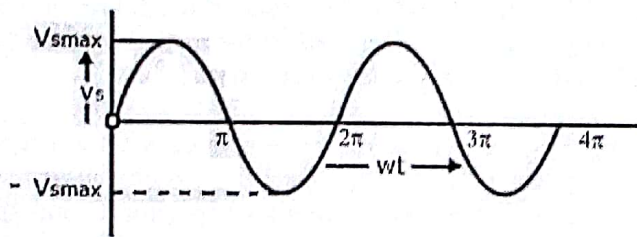
This is the most simple form of the filter circuit and in this arrangement a high value capacitor C is placed directly across the output terminals, as shown in figure. During the conduction period it gets charged and stores up energy to it during non-conduction period. Through this process, the time duration during which F_t is to be noted here that the capacitor C gets charged to the peak because there is no resistance (except the negligible forward resistance of diode) in the charging path. But the discharging time is quite large (roughly 100 times more than the charging time depending upon the value of RL) because it discharges through load resistance RL .

The function of the capacitor filter may be viewed in terms of impedances. The large value capacitor C offers a low impedance shunt path to the ac components or ripples but offers high impedance to the dc component. Thus ripples get bypassed through capacitor C and only dc component flows through the load resistance RL .

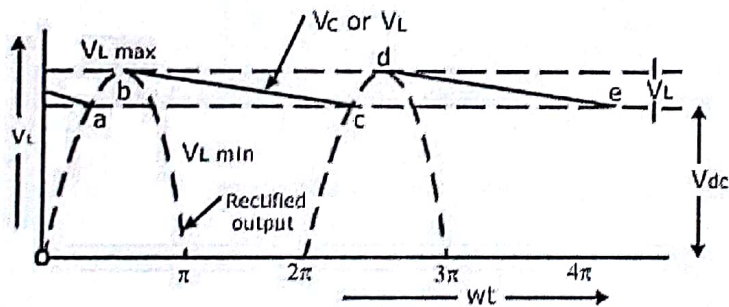
Capacitor filter is very popular because of its low cost, small size, light weight and good characteristics.



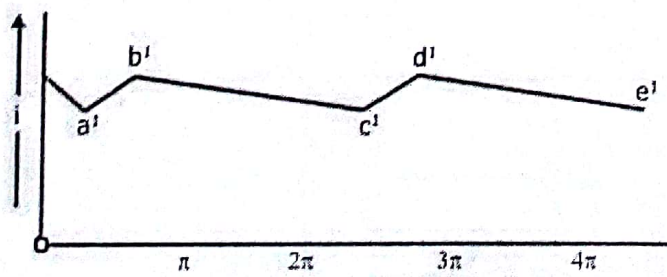
Circuit Diagram



Input voltage Waveform to Rectifier



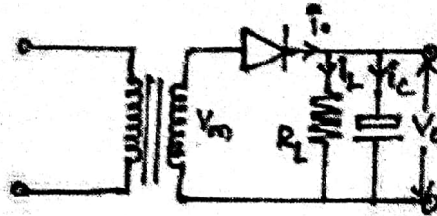
Rectified and filtered Output Voltage Waveform



Load Current Waveform
Half-wave Rectifier With Shunt Capacitor Filter

www.CircuitsToday.com

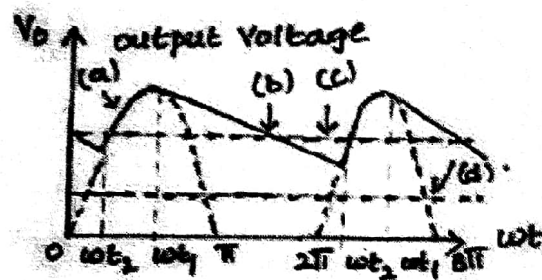
CAPACITOR FILTER WITH HWR



Cut In angle - ωt_2

Cut out angle = ωt_1

$$\omega t_1 = \pi - \tan^{-1} \omega C R_L$$



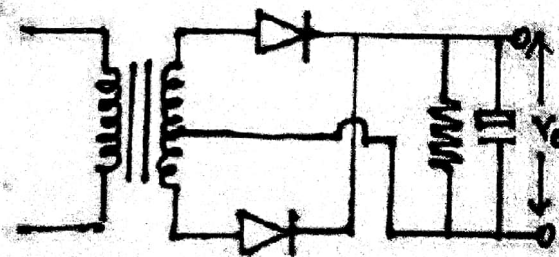
(a) Capacitor charging through diode
($\omega t_2 - \omega t_1$)

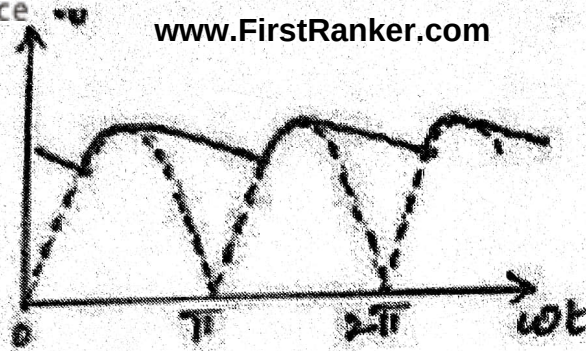
(b) Capacitor discharging through R_L
(ωt_1 to ωt_2)

(c) Average (DC) voltage with filter

(d) Average (DC) voltage without filter.

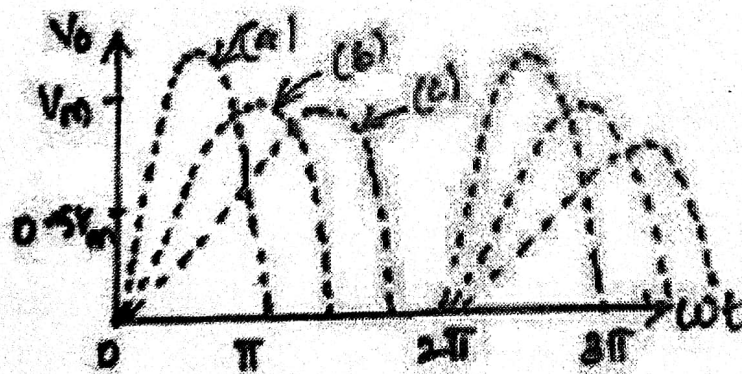
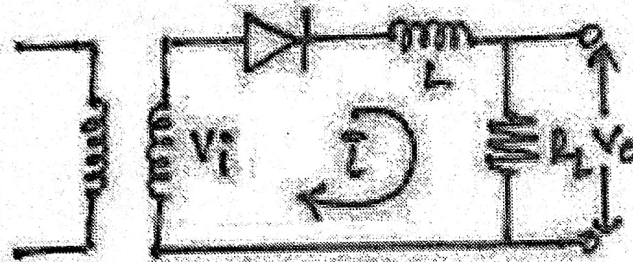
CAPACITOR FILTER WITH FWR





$$\text{Ripple factor } r = \frac{1}{4\sqrt{3}fCR_L}$$

Ripple freq_{FWR} = 2 ripple freq_{HWR}.



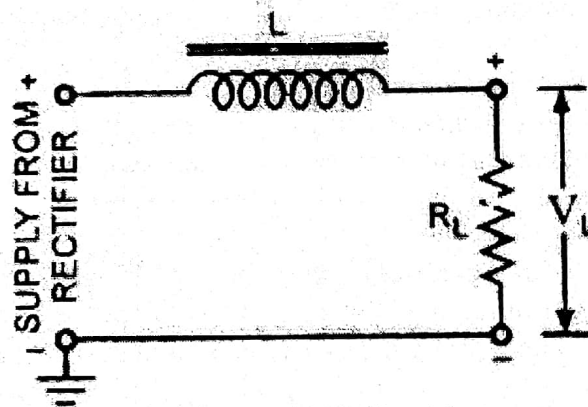
$$(a) \frac{W_L}{R_L} = 0 \quad (b) \frac{W_L}{R_L} = 1 \quad (c) \frac{W_L}{R_L} = 5.$$

The worthnoting points about shunt capacitor filter are:

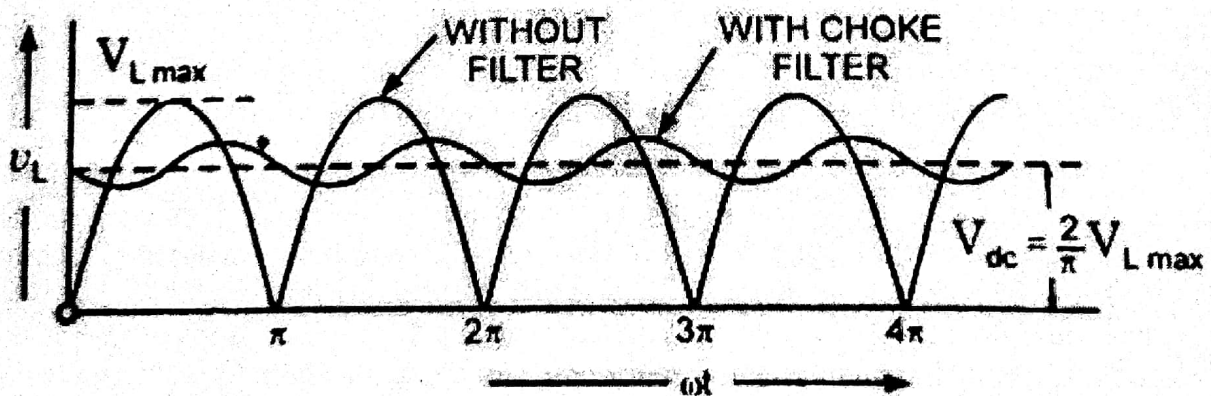
1. For a fixed-value filter capacitance larger the load resistance R_L larger will be the discharge time constant $C R_L$ and therefore, lower the ripples and more the output voltage. On the other hand lower the load resistance (or more the load current), lower will be the output voltage.

2. Similarly smaller the filter capacitor, the less charge it can hold and more it will discharge. Thus the peak-to-peak value of the ripple will increase, and the average dc level will decrease. Larger the filter capacitor, the more charge it can hold and the less it will discharge. Hence the peak-to-peak value of the ripple will be less, and the average dc level will increase. But, the maximum value of the capacitance that can be employed is limited by another factor. The larger the capacitance value, the greater is the current required to charge the capacitor to a given voltage. The maximum current that can be handled by a diode is limited by the figure quoted by the manufacturer. Thus the maximum value of the capacitance, that can be used in the shunt filter capacitor is limited.

3.3.2 Series Inductor Filter.



Circuit Diagram



*Output Voltage Waveforms
Full-Wave Rectifier With Series Inductor Filter*

In this arrangement a high value inductor or choke L is connected in series with the rectifier element and the load, as illustrated in figure. The filtering action of an inductor filter depends upon its property of opposing any change in the current flowing through it. When the output current of the rectifier increases above a certain value, energy is stored in it in the form of magnetic field and this energy is given up when the output current falls below the average value. Thus by placing a choke coil in series with the rectifier output and load, any sudden change in current that might have occurred in the circuit without an inductor is smoothed out by the presence of the inductor L .

The function of the inductor filter may be viewed in terms of impedances. The choke offers high impedance to the ac components but offers almost zero resistance to the desired dc components. Thus ripples are removed to a large extent. Nature of the output voltage without filter and with choke filter is shown in figure.

For dc (zero frequency), the choke resistance R_c in series with the load resistance R_L forms a voltage divider and dc voltage across the load is given as

where V_{dc} is dc voltage output from a full-wave rectifier. Usually choke coil resistance R_c , is much small than R_L and, therefore, almost entire of the dc voltage is available across the load resistance R_L .

Since the reactance of inductor increases with the increase in frequency, better filtering of the higher harmonic components takes place, so effect of third and higher harmonic voltages can be neglected.

As obvious from equation, if choke coil resistance R_c is negligible in comparison to load resistance R_L , then the entire dc component of rectifier output is available across R_L and is equal to $V_{L \max}$. The ac voltage partly drops across X_L and partly over R_L .

3.3.3 L-SECTION FILTER:

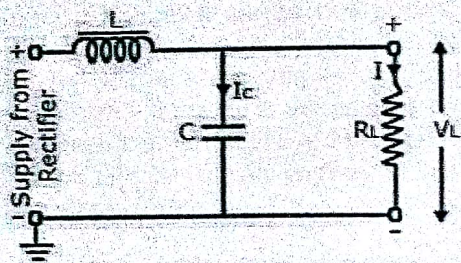
A simple series inductor reduces both the peak and effective values of the output current and output voltage. On the other hand a simple shunt capacitor filter reduces the ripple voltage but increases the diode current. The diode may get damaged due to large current and at the same time it causes greater heating of supply transformer resulting in reduced efficiency.

In an inductor filter, ripple factor increases with the increase in load resistance R_L while in a capacitor filter it varies inversely with load resistance R_L .

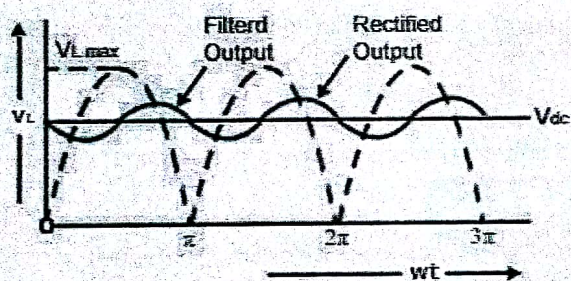
From economical point of view also, neither series inductor nor shunt capacitor type filters are suitable.

Practical filter-circuits are derived by combining the voltage stabilizing action of shunt capacitor with the current smoothing action of series choke coil. By using combination of inductor and capacitor ripple factor can be lowered, diode current can be restricted and simultaneously ripple

factor can be made almost independent of load resistance (or load current). Two types of most commonly used combinations are choke-input or L-section filter and capacitor-input or Pi-Filter.



Circuit Diagram

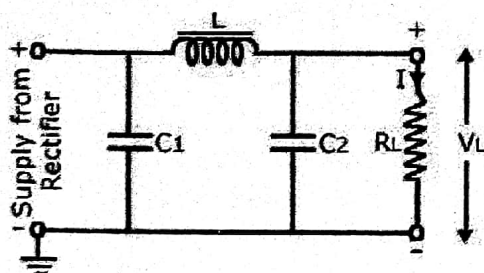


Rectified and Filtered Output Voltage Waveform
Full-wave Rectifier With Choke-Input Filter

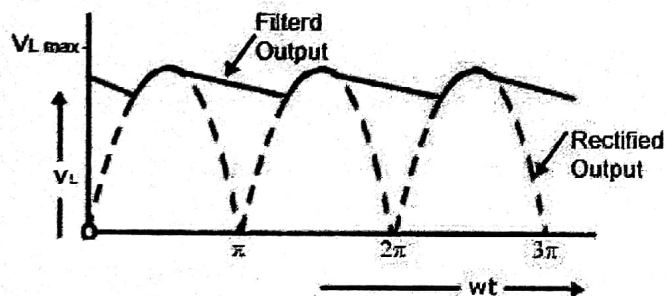
Choke-input filter is explained below:

Choke-input filter consists of a choke L connected in series with the rectifier and a capacitor C connected across the load. This is also sometimes called the L-section filter because in this arrangement inductor and capacitor are connected, as an inverted L. In figure only one filter section is shown. But several identical sections are often employed to improve the smoothing action. (The choke L on the input side of the filter readily allows dc to pass but opposes the flow of ac components because its dc resistance is negligibly small but ac impedance is large. Any fluctuation that remains in the current even after passing through the choke are largely by-passed around the load by the shunt capacitor because X_c is much smaller than R_L . Ripples can be reduced effectively by making X_L greater than X_c at ripple frequency. However, a small ripple still remains in the filtered output and this is considered negligible if it is less than 1%. The rectified and filtered output voltage waveforms from a full-wave rectifier with choke-input filter are shown in figure.

3.3.4 Π -SECTION FILTER:



Circuit Diagram



Rectified and Filtered Output Voltage Waveform
Full-wave Rectifier With capacitor Input Filter

Capacitor-Input or Pi-Filter.

Such a filter consists of a shunt capacitor C_1 at the input followed by an L-section filter formed by series inductor L and shunt capacitor C_2 . This is also called the n -filter because the shape of the circuit diagram for this filter appears like Greek letter n (π). Since the rectifier feeds directly into the capacitor so it is also called *capacitor input filter*.

As the rectified output is fed directly into a capacitor C_1 . Such a filter can be used with a half-wave rectifier (series inductor and L-section filters cannot be used with half-wave rectifiers). Usually electrolytic capacitors are used even though their capacitances are large but they occupy minimum space. Usually both capacitors C_1 and C_2 are enclosed in one metal container. The metal container serves as, the common ground for the two capacitors.

A capacitor-input or π -filter is characterized by a high voltage output at low current drains. Such a filter is used, if, for a given transformer, higher voltage than that can be obtained from an L-section filter is required and if low ripple than that can be obtained from a shunt capacitor filter or L-section filter is desired. In this filter, the input capacitor C_1 is selected to offer very low reactance to the ripple frequency. Hence major part of filtering is accomplished by the input

capacitor C_1 . Most of the remaining ripple is removed by the L-section filter consisting of a choke L and capacitor C_2 .)

The action of this filter can *best* be understood by considering the action of L-section filter, formed by L and C_2 , upon the triangular output voltage wave from the input capacitor C_1 . The charging and discharging action of input capacitor C_1 has already been discussed. The output voltage is roughly the same as across input capacitor C_1 less the dc voltage drop in inductor. The ripples contained in this output are reduced further by L-section filter. The output voltage of pi-filter falls off rapidly with the increase in load-current and, therefore, the voltage regulation with this filter is very poor.

SALIENT FEATURES OF L-SECTION AND PI-FILTERS.

1. In pi-filter the dc output voltage is much larger than that can be had from an L-section filter with the same input voltage.
2. In pi-filter ripples are less in comparison to those in shunt capacitor or L-section filter. So smaller valued choke is required in a pi-filter in comparison to that required in L-section filter.
3. In pi-filter, the capacitor is to be charged to the peak value hence the rms current in supply transformer is larger as compared in case of L-section filter.
4. Voltage regulation in case of pi-filter is very poor, as already mentioned. So π -filters are suitable for fixed loads whereas L-section filters can work satisfactorily with varying loads provided a minimum current is maintained.
5. In case of a pi-filter PIV is larger than that in case of an L-section filter.

COMPARISON OF FILTERS

- 1) A capacitor filter provides V_m volts at less load current. But regulation is poor.
- 2) An Inductor filter gives high ripple voltage for low load currents. It is used for high load currents
- 3) L – Section filter gives a ripple factor independent of load current. Voltage Regulation can be improved by use of bleeder resistance
- 4) Multiple L – Section filter or π filters give much less ripple than the single L – Section Filter.

Consider a half-wave rectifier circuit with a sinusoidal a.c input voltage, we know that the instantaneous value of the sinusoidal a.c. i/p voltage is given by the relation,

$$v = V_m \sin \omega t$$

$$= V_m \sin \theta \quad \because \theta = \omega t$$

where V_m = Maximum value of the AC i/p voltage

now let I_m = Maximum value of diode current or load current.

It is the current through the resistor R_L .

$V_{av} = V_{dc}$ = Average or dc value of o/p (or load) voltage across the load resistor

$I_{av} = I_{dc}$ = Average or DC value of load current.

By observing the o/p voltage of a Half-wave rectifier, it indicates that there is an o/p voltage (varying sinusoidal) for a period from 0 to π & nothing for a period from π to 2π .

The average or DC value of the o/p voltage is given by the relation

$$V_{dc} = \frac{\text{Area under the curve over the full cycle}}{\text{Base}}$$

$$= \int_0^{2\pi} \frac{v d\omega t}{2\pi}$$

$$= \int_0^{\pi} \frac{v d\omega t}{2\pi} + \int_{\pi}^{2\pi} \frac{v d\omega t}{2\pi}$$

$$= \int_0^{\pi} \frac{v d\omega t}{2\pi}$$

$$= \int_0^{\pi} \frac{V_m \sin \omega t d\omega t}{2\pi}$$

$$= \frac{V_m}{2\pi} \left(-\cos \omega t \right) \Big|_0^{\pi}$$

$$= \frac{V_m}{2\pi} (+1 - (-1))$$

$$\because v = V_m \sin \omega t \quad \pi \leq \omega t \leq 2\pi$$

$$= 0 \quad 2\pi \leq \omega t \leq 2\pi$$

$$\boxed{V_{dc} = \frac{V_m}{\pi}}$$

$$I_{dc} = \frac{V_{dc}}{R_L}$$

$$= \frac{V_m}{\pi R_L} = \frac{I_m}{\pi} \quad \therefore I_m = \frac{V_m}{R_L}$$

$$\boxed{I_{dc} = \frac{I_m}{\pi}}$$

If we consider diode forward resistance (R_f), secondary winding resistance (R_s) then

$$I_m = \frac{V_m}{R_L + R_s + R_f}$$

Ex. 2.2

$$\boxed{I_{dc} = \frac{V_{dc}}{R_L + R_s + R_f} = \frac{V_m}{\pi(R_f + R_s + R_L)}}$$

$$\boxed{V_{dc} = \frac{V_m}{\pi} - I_{dc} \cdot (R_f + R_s)}$$

RIPPLE FACTOR (γ)

The load voltage V_L contains rectified alternate half cycle, and can be represented by Fourier series.

$$V_L = V_m \left[\underbrace{\frac{1}{\pi}}_{\text{DC Component}} + \underbrace{\frac{1}{2} \cos \omega t - \frac{2}{\pi} \sum_{k=1}^{\infty} \frac{\cos 2k\omega t}{2(k+1)(2k-1)}}_{\text{AC Component}} \right]$$

From the above equation we can find the load voltage V_L consists of DC component & sinusoidal component.

$$V_{rms} = \sqrt{V_{rms1}^2 + V_{rms2}^2 + \dots}$$

where V_{rms1} & V_{rms2} etc are the rms value of each ~~freq~~ component.

$$V_{rms}^2 = V_{dc}^2 + V_{s(rms)}^2$$

where $V_{s(rms)}$ is the rms value of the ac component.

The ripple factor is the ratio of rms value of ac component to the dc value.

$$\text{Ripple factor } (r) = \frac{\text{rms value of ac component}}{\text{dc value of component}} = \frac{V_r(\text{rms})}{V_{dc}}$$

$$\text{CART} \quad V_{rms}^2 = V_{dc}^2 + V_r(\text{rms})^2$$

$$\frac{V_{rms}^2}{V_{dc}^2} = \frac{V_{dc}^2}{V_{dc}^2} + \frac{V_r(\text{rms})^2}{V_{dc}^2}$$

$$\frac{V_{rms}^2}{V_{dc}^2} - 1 = \frac{V_r(\text{rms})^2}{V_{dc}^2}$$

$$\therefore \frac{V_r(\text{rms})^2}{V_{dc}^2} = \frac{V_{rms}^2}{V_{dc}^2} - 1$$

$$\frac{V_r(\text{rms})}{V_{dc}} = \sqrt{\frac{V_{rms}^2}{V_{dc}^2} - 1}$$

$$r = \sqrt{\frac{V_{rms}^2}{V_{dc}^2} - 1}$$

RMS value of Voltage

$$V_{rms} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} v^2 d(\omega t)}$$

$$= \sqrt{\frac{1}{2\pi} \int_0^{\pi} V_m^2 \sin^2 \omega t d(\omega t)}$$

$$= \sqrt{\frac{V_m^2}{2\pi} \int_0^{\pi} \left[\frac{1 - \cos 2\omega t}{2} \right] d(\omega t)}$$

$$= \sqrt{\frac{V_m^2}{4\pi} \int_0^{\pi} (1 - \cos 2\omega t) d(\omega t)}$$

$$= \frac{V_m}{2} \sqrt{\frac{1}{\pi}}$$

$$= V_m \sqrt{\frac{1}{2\pi} \int_0^{\pi} \frac{1 - \cos(2\omega t)}{2} d\omega t}$$

$$= V_m \sqrt{\frac{1}{2\pi} \left[\frac{\omega t}{2} - \frac{\sin 2\omega t}{2 \times 2} \right]_0^{\pi}}$$

$$= V_m \sqrt{\frac{1}{2\pi} \cdot \frac{\pi}{2}}$$

$$= V_m \sqrt{\frac{1}{4}}$$

$$\boxed{V_{rms} = \frac{V_m}{2}}$$

$$\Gamma = \sqrt{\left(\frac{V_{rms}}{V_{dc}} \right)^2 - 1}$$

$$= \sqrt{\left(\frac{V_m/2}{V_m/\pi} \right)^2 - 1}$$

$$= \sqrt{\left(\frac{\pi}{2} \right)^2 - 1}$$

$$\boxed{\Gamma = 1.21}$$

EFFICIENCY (η)

The ratio of dc power to ac power is known as rectifier efficiency (η)

$$\eta = \frac{\text{dc o/p power}}{\text{AC i/p power}}$$

$$= \frac{P_{dc}}{P_{ac}}$$

$$P_{dc} = \frac{(V_{dc})^2}{R_L} = \left(\frac{V_m}{\pi} \right)^2 / R_L$$

$$P_{ac} = \frac{(V_{rms})^2}{R_L} = \frac{(V_m/2)^2}{R_L}$$

$$\therefore \eta = \frac{P_{ac}}{P_{dc}}$$

$$= \frac{\left(\frac{V_m}{\pi}\right)^2 / R_L}{\left(\frac{V_m}{2}\right)^2 / R_L} = \frac{\left(\frac{V_m}{\pi}\right)^2}{\left(\frac{V_m}{2}\right)^2}$$

$$= \frac{V_m^2}{\pi^2} \bigg/ \frac{V_m^2}{4}$$

$$= \frac{4}{\pi^2} = 0.406$$

$$\boxed{\eta = 40.6\%}$$

Form Factor

$$\text{Form Factor} = \frac{\text{RMS Value}}{\text{Average Value}}$$

$$= \frac{V_m/2}{V_m/\pi} = \pi/2 = \underline{\underline{1.57}}$$

Peak Factor

$$\text{Peak Factor} = \frac{\text{Peak Value}}{\text{RMS Value}}$$

$$= \frac{V_m}{V_m/2} = \underline{\underline{2}}$$

Problem: A Half wave Rectifier, having a resistive load of 1000Ω , rectifies an alternating voltage of $325V$ peak value and the diode has a forward resistance of 100Ω . Calculate

(a) Peak, average & RMS value of current

(b) D.C power output

(c) AC i/p power

(d) Efficiency of the rectifier.

Sol Given: $R_L = 1000\Omega$, $V_m = 325V$, $R_f = 100\Omega$

(a) Peak value of current

$$I_m = \frac{V_m}{R_f + R_L} = \frac{325}{100 + 1000} = 295.45 \text{ mA}$$

Average current

$$I_{dc} = \frac{I_m}{\pi} = \frac{295.45}{\pi} = 94.046 \text{ mA}$$

RMS value of current

$$I_{rms} = \frac{I_m}{2} = \frac{295.45}{2} = 147.725 \text{ mA}$$

(b) D.C power output

$$P_{dc} = I_{dc}^2 \times R_L$$

$$= (94.046 \times 10^{-3})^2 \times 1000$$

$$= 8.845 \text{ W}$$

(c) AC input power

$$P_{ac} = (I_{rms})^2 \times (R_f + R_L)$$

$$= (147.725 \times 10^{-3})^2 \times 1000$$

$$= 24 \text{ W}$$

(d) Efficiency of rectification $= \eta = \frac{P_{dc}}{P_{ac}} = \frac{8.845}{24} = 36.85\%$

Inductor Filter



$$V_o = \frac{2V_m}{\pi} - \frac{4V_m}{3\pi} \cos \theta$$

Current due to AC Component

$$= \frac{\frac{4V_m}{3\pi}}{\sqrt{R^2 + X_L^2}}$$

Since we consider only harmonic $X_L = 2\omega L$

$$\Rightarrow I_x = \frac{\frac{4V_m}{3\pi}}{\sqrt{R^2 + (2\omega L)^2}}$$

Current due to DC Component

$$= \frac{2V_m}{\pi R_L}$$

Total load current

$$i = \frac{2V_m}{\pi R_L} - \frac{4V_m}{3\pi \sqrt{R_L^2 + 4\omega^2 L^2}}$$

The RMS value of AC Component

$$I_o(rms) = \frac{\frac{4V_m}{3\pi}}{\sqrt{R_L^2 + 4\omega^2 L^2}}$$

$$\text{Ripple Factor} = \frac{I_o(rms)}{I_{dc}}$$

$$= \frac{\frac{4V_m}{3\pi \sqrt{R_L^2 + 4\omega^2 L^2}}}{\frac{2V_m}{\pi R_L}}$$

$$= \frac{2}{3\sqrt{R_L^2 + 4\omega^2 L^2}} \cdot \frac{\pi R_L}{\pi R_L}$$

$$= \frac{2R_L}{3\sqrt{R_L^2 + 4\omega^2 L^2}}$$

$$= \frac{2R_L}{3\sqrt{R_L^2 + 4\omega^2 L^2}}$$

$$= \frac{2}{3\sqrt{1 + \frac{4\omega^2 L^2}{R_L^2}}}$$

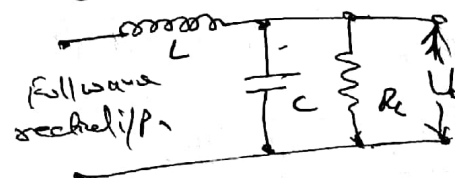
$$\frac{4\omega^2 L^2}{R_L^2} \gg 1$$

$$\therefore \frac{2}{3\sqrt{1 + \frac{4\omega^2 L^2}{R_L^2}}}$$

$$\frac{2R_L}{3\sqrt{4\omega^2 L^2}}$$

$$X = \frac{R_L}{3\sqrt{4\omega^2 L^2}}$$

L-Section filter



$$V_o = \frac{2V_m}{\pi} - \frac{4V_m}{3\pi} \cos \theta$$

$$\text{The dc voltage } V_{dc} = \frac{2V_m}{\pi}$$

$$\therefore I_{rms} = \frac{4V_m}{3\pi \sqrt{2}} \cdot \frac{1}{X_L}$$

$$= \frac{\sqrt{2}}{3} \cdot \frac{V_{dc}}{X_L}$$

$$V_{rms} = I_{rms} \cdot X_C$$

$$= \frac{\sqrt{2}}{3} \cdot V_{dc} \cdot \frac{X_C}{X_L}$$

The ripple factor

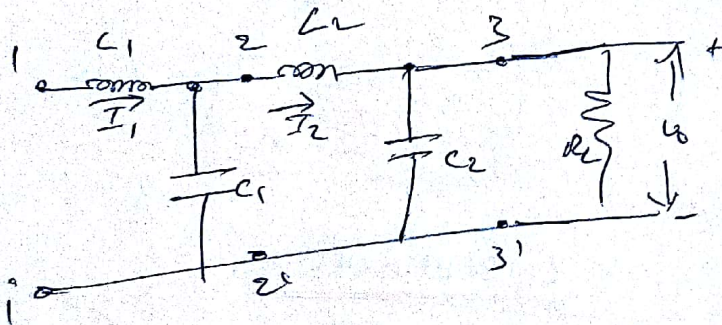
$$\begin{aligned} r &= \frac{V_{rms}}{V_{dc}} \\ &= \frac{\frac{\sqrt{2}}{3} \cdot \frac{X_C}{X_L}}{\frac{\sqrt{2}}{3} \cdot \frac{1}{4\omega^2 CL}} \end{aligned}$$

$$\therefore X_C = \frac{1}{2\omega C} \text{ and } X_L = 2\omega L$$

$$r = \frac{\sqrt{2}}{3} \cdot \frac{1}{4\omega^2 CL}$$

AC
filter

L-section filter



The alternating current I_1 through L_1 is given by

$$I_1 = \frac{\sqrt{2} V_{dc}}{3} \cdot \frac{1}{X_{L1}}$$

The AC voltage across C_1 is given by

$$V_{22'} = I_1 X_{C1}$$

The alternating current I_2 through L_2 is given by

$$I_2 = \frac{V_{22'}}{X_{L2}}$$

The AC current across C_2 and hence across the load is given by

$$V_{33'} = I_2 X_{C2}$$

$$= I_1 \frac{X_{C2} X_{C1}}{X_{L2}}$$

$$= \frac{\sqrt{2} V_{dc}}{3} \cdot \frac{X_{C1}}{X_{L1}} \cdot \frac{X_{C2}}{X_{L2}}$$

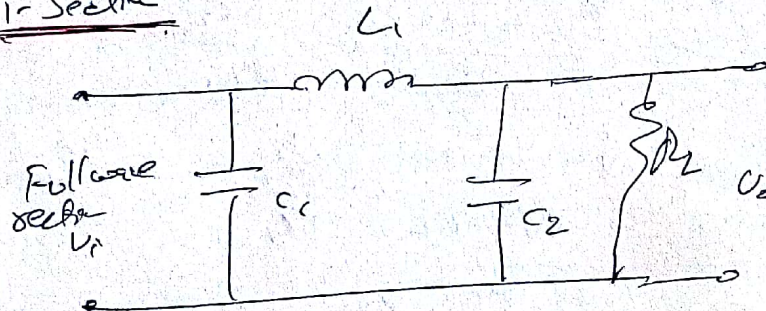
The ripple factor is obtained by dividing the above eqⁿ by V_{dc} . Hence

$$\Gamma = \frac{\sqrt{2}}{3} \cdot \frac{X_{C1}}{X_{L1}} \cdot \frac{X_{C2}}{X_{L2}}$$

$$\Gamma_n = \frac{\sqrt{2}}{3} \left(\frac{X_C}{X_L} \right)^n$$

$$\Gamma_n = \frac{\sqrt{2}}{3} \cdot \frac{1}{(16\pi^2 f^2 Z_C)^n}$$

II-Section



$$V_{rpp} = \frac{I_{dc}}{2fC_1}$$

$$V_{rms} = V_2' = \frac{V_{rpp}}{\pi\sqrt{2}} = \frac{I_{dc}}{2\pi f C_1 \sqrt{2}} = \frac{I_{dc}}{\sqrt{2}} \cdot \frac{1}{2\pi f C_1} = \frac{I_{dc} X_{C1}}{\sqrt{2}}$$

$$= \frac{I_{dc} X_{C1}}{\sqrt{2}}$$

$$= \frac{I_{dc}}{\sqrt{2}} \cdot \frac{2}{2} \cdot \frac{1}{2\pi f C_1}$$

$$= \frac{I_{dc}^2}{\sqrt{2}} \cdot \frac{1}{2 \cdot 2\pi f C_1} = \frac{2 I_{dc}}{\sqrt{2}} \cdot X_{C1}$$

$$= \frac{2 I_{dc} X_{C1}}{\sqrt{2}} = \frac{\sqrt{2}}{\sqrt{2}} \cdot \frac{2 I_{dc} X_{C1}}{\sqrt{2}}$$

$$V_{rms} = \frac{\sqrt{2} I_{dc} X_{C1}}{\sqrt{2}}$$

for

The voltage V_2' is impressed on an L section, the r.m.s. value of ripple is

$V_2' \cdot X_{C2} / X_{L1}$ Hence the ripple factor is

$$\Gamma = \frac{V_{rms}}{V_{dc}} = \frac{\sqrt{2} I_{dc} X_{C1}}{V_{dc}}$$

$$\Gamma = \frac{V_{rms}}{V_{dc}} \cdot \frac{X_{C2}}{X_{L1}}$$

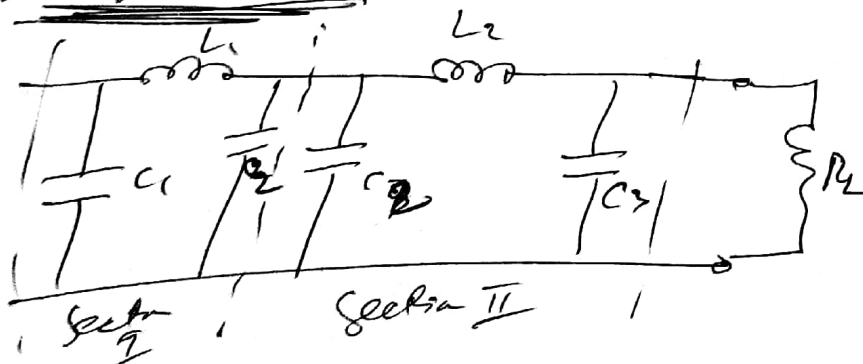
$$= \frac{\sqrt{2} I_{dc} X_{C1}}{V_{dc}} \cdot \frac{X_{C2}}{X_{L1}}$$

$$= \frac{\sqrt{2} V_{dc} X_{C1}}{V_{dc} \cdot R_L} \cdot \frac{X_{C2}}{X_{L1}}$$

$$\therefore I_{dc} = \frac{V_{dc}}{R_L}$$

$$\boxed{\Gamma = \frac{\sqrt{2} X_{C1}}{R_L} \cdot \frac{X_{C2}}{X_{L1}}}$$

Multiple π Section



$$\Gamma = \sqrt{2} \frac{X_{C1}}{R_L} \cdot \frac{X_{C2}}{X_{L1}} \cdot \frac{X_{C3}}{X_{L2}} \cdots \frac{X_{Cn}}{X_{L(n-1)}}$$

Comparison of Various Filter circuits in terms of
Ripple factor:

	Type of Filter				
	none	L	C	LC	π
V_{dc} at no load	$0.636 V_m$	$0.636 V_m$	V_m	V_m	V_m
V_{dc} at load I_{dc}	$0.636 V_m$	$0.636 V_m$	$V_m - \frac{4.170 I_{dc}}{C}$	$0.636 V_m$	$V_m - \frac{4.170 I_{dc}}{C}$
Ripple factor	0.48	$\frac{R_L}{16000L}$	$\frac{2610}{CR_L}$	$\frac{0.83}{LC}$	$\frac{3330}{LCR_L}$
Peak inverse voltage PIV	$2V_m$	$2V_m$	$2V_m$	$2V_m$	$2V_m$

UNIT – 4

TRANSISTOR CHARACTERISTICS

UNIT IV

TRANSISTOR CHARACTERISTICS

4.1 INTRODUCTION

A bipolar junction transistor (BJT) is a three terminal device in which operation depends on the interaction of both majority and minority carriers and hence the name bipolar. The BJT is analogous to vacuum triode and is comparatively smaller in size. It is used in amplifier and oscillator circuits, and as a switch in digital circuits. It has wide applications in computers, satellites and other modern communication systems.

4.2 CONSTRUCTION OF BJT AND ITS SYMBOLS

The **Bipolar Transistor** basic construction consists of two PN-junctions producing three connecting terminals with each terminal being given a name to identify it from the other two. These three terminals are known and labelled as the Emitter (E), the Base (B) and the Collector (C) respectively. There are two basic types of bipolar transistor construction, PNP and NPN, which basically describes the physical arrangement of the P-type and N-type semiconductor materials from which they are made.

Transistors are three terminal active devices made from different semiconductor materials that can act as either an insulator or a conductor by the application of a small signal voltage. The transistor's ability to change between these two states enables it to have two basic functions: "switching" (digital electronics) or "amplification" (analogue electronics). Then bipolar transistors have the ability to operate within three different regions:

- 1. Active Region - the transistor operates as an amplifier and $I_c = \beta \cdot I_b$
- 2. Saturation - the transistor is "fully-ON" operating as a switch and $I_c = I(\text{saturation})$
- 3. Cut-off - the transistor is "fully-OFF" operating as a switch and $I_c = 0$

Bipolar Transistors are current regulating devices that control the amount of current flowing through them in proportion to the amount of biasing voltage applied to their base terminal acting like a current-controlled switch. The principle of operation of the two transistor types PNP and NPN, is exactly the same the only difference being in their biasing and the polarity of the power supply for each type (fig 1).

Bipolar Transistor Construction

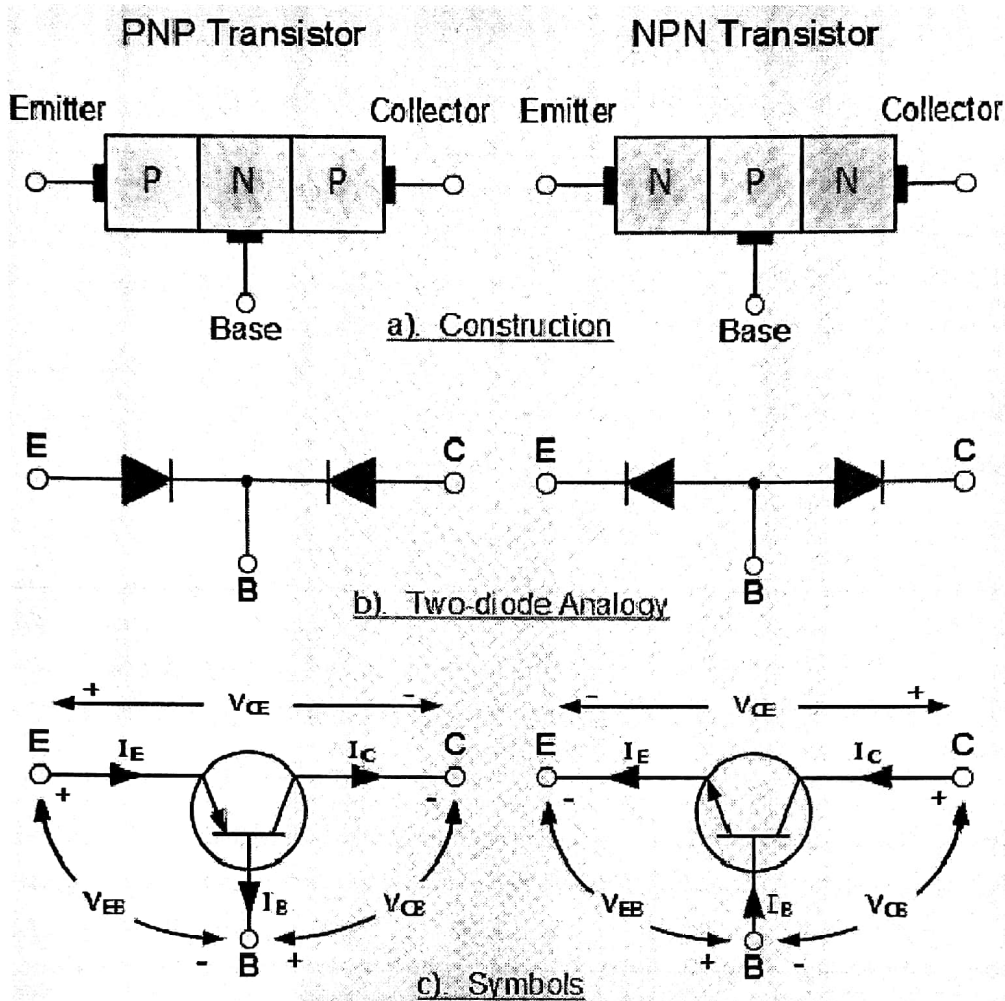


Fig:1

The construction and circuit symbols for both the PNP and NPN bipolar transistor are given above with the arrow in the circuit symbol always showing the direction of "conventional current flow" between the base terminal and its emitter terminal. The direction of the arrow always points from the positive P-type region to the negative N-type region for both transistor types, exactly the same as for the standard diode symbol.

4.3 TRANSISTOR CURRENT COMPONENTS:

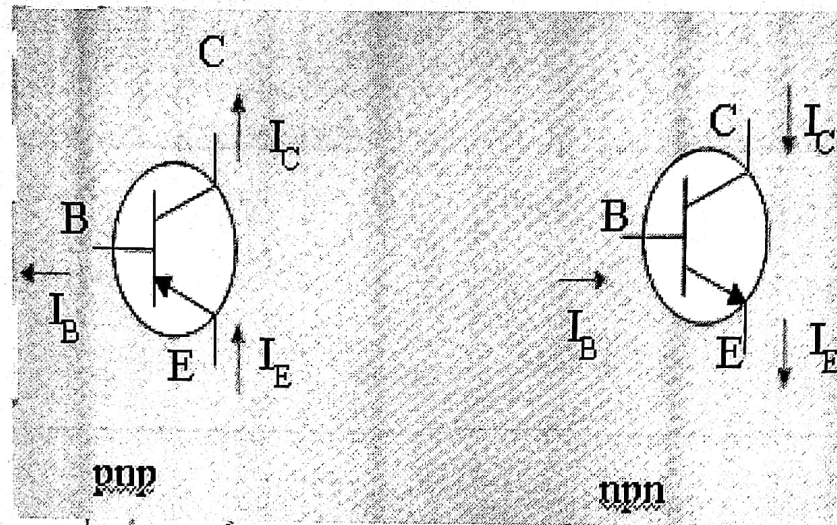


FIG 2

The above fig 2 shows the various current components, which flow across the forward biased emitter junction and reverse- biased collector junction. The emitter current I_E consists of hole current I_{pE} (holes crossing from emitter into base) and electron current I_{nE} (electrons crossing from base into emitter). The ratio of hole to electron currents, I_{pE} / I_{nE} , crossing the emitter junction is proportional to the ratio of the conductivity of the p material to that of the n material. In a transistor, the doping of that of the emitter is made much larger than the doping of the base. This feature ensures (in p-n-p transistor) that the emitter current consists an almost entirely of holes. Such a situation is desired since the current which results from electrons crossing the emitter junction from base to emitter does not contribute carriers, which can reach the collector.

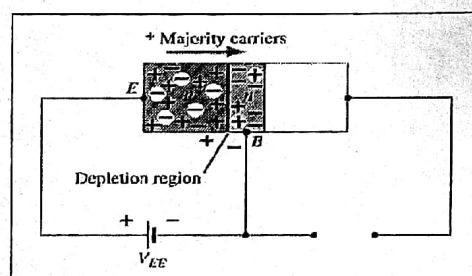
Not all the holes crossing the emitter junction J_E reach the the collector junction J_C Because some of them combine with the electrons in n-type base. If I_{pC} is hole current at junction J_C there must be a bulk recombination current ($I_{pE} - I_{pC}$) leaving the base.

Actually, electrons enter the base region through the base lead to supply those charges, which have been lost by recombination with the holes injected in to the base across J_E . If the emitter were open circuited so that $I_E=0$ then I_{pC} would be zero. Under these circumstances, the base and collector current I_C would equal the reverse saturation current I_{CO} . If $I_E \neq 0$ then

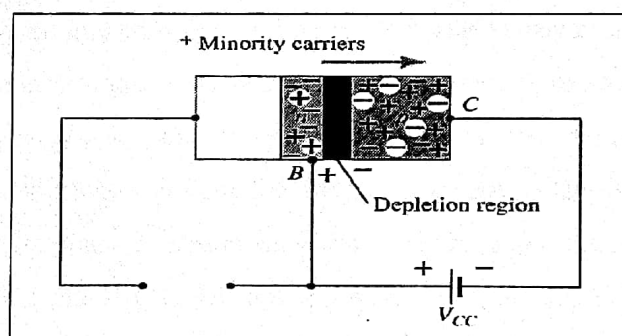
$$I_C = I_{CO} - I_{pC}$$

For a p-n-p transistor, I_{CO} consists of holes moving across J_C from left to right (base to collector) and electrons crossing J_C in opposite direction. Assumed referenced direction for I_{CO} i.e. from right to left, then for a p-n-p transistor, I_{CO} is negative. For an n-p-n transistor, I_{CO} is positive. The basic operation will be described using the pnp transistor. The operation of the pnp transistor is exactly the same if the roles played by the electron and hole are interchanged.

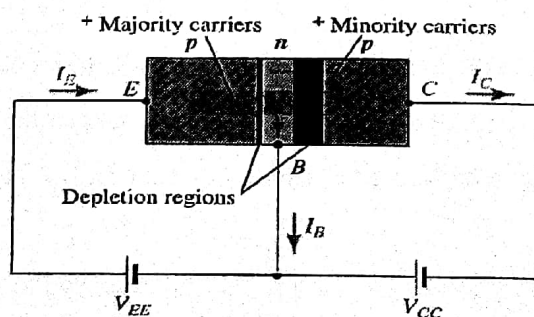
One p-n junction of a transistor is reverse-biased, whereas the other is forward-biased.



Forward-biased junction of a pnp transistor



Reverse-biased junction of a pnp transistor



Both biasing potentials have been applied to a pnp transistor and resulting majority and minority carrier flows indicated.

Majority carriers (+) will diffuse across the forward-biased p-n junction into the n-type material.

A very small number of carriers (+) will through n-type material to the base terminal. Resulting I_B is typically in order of microamperes.

The large number of majority carriers will diffuse across the reverse-biased junction into the p-type material connected to the collector terminal

Applying KCL to the transistor :

$$I_E = I_C + I_B$$

The comprises of two components – the majority and minority carriers

$$I_C = I_{Cmajority} + I_{Cminority}$$

$I_{CO} - I_C$ current with emitter terminal open and is called leakage current

Various parameters which relate the current components is given below

Emitter efficiency:

$$\gamma = \frac{\text{current of injected carriers at } J_E}{\text{total emitter current}}$$

$$\gamma = \frac{I_{pE}}{I_{pE} + I_{nE}} = \frac{I_{pE}}{I_{nE}}$$

Transport Factor:

$$\beta^* = \frac{\text{injected carrier current reaching } J_C}{\text{injected carrier current at } J_E}$$

$$\beta^* = \frac{I_{pC}}{I_{nE}}$$

Large signal current gain:

The ratio of the negative of collector current increment to the emitter current change from zero (cut-off) to I_E the large signal current gain of a common base transistor.

$$\alpha = \frac{-(I_C - I_{C0})}{I_E}$$

Since I_C and I_E have opposite signs, then α , as defined, is always positive. Typically numerical values of α lies in the range of 0.90 to 0.995

$$\alpha = \frac{I_{pC}}{I_E} = \frac{I_{pC}}{I_{nE}} * \frac{I_{pE}}{I_E} \quad \alpha = \beta * \gamma$$

The transistor alpha is the product of the transport factor and the emitter efficiency. This statement assumes that the collector multiplication ratio α^* is unity. α^* is the ratio of total current crossing J_C to hole arriving at the junction.

4.4 Bipolar Transistor Configurations

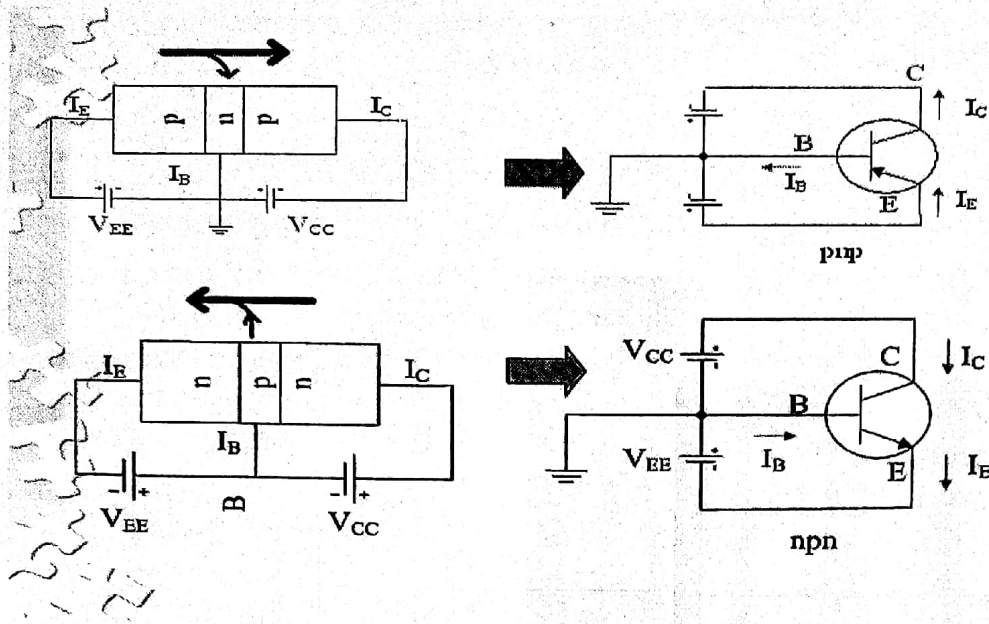
As the **Bipolar Transistor** is a three terminal device, there are basically three possible ways to connect it within an electronic circuit with one terminal being common to both the input and output. Each method of connection responding differently to its input signal within a circuit as the static characteristics of the transistor vary with each circuit arrangement.

- 1. Common Base Configuration - has Voltage Gain but no Current Gain.
- 2 Common Emitter Configuration - has both Current and Voltage Gain.
- 3. Common Collector Configuration - has Current Gain but no Voltage Gain.

4.5 COMMON-BASE CONFIGURATION

Common-base terminology is derived from the fact that the : base is common to both input and output of t configuration. base is usually the terminal closest to or at ground potential. Majority carriers can cross the reverse-biased junction because the injected majority carriers will appear as minority carriers in the n-type material. All current directions will refer to conventional (hole) flow and the arrows in all electronic symbols have a direction defined by this convention.

Note that the applied biasing (voltage sources) are such as to establish current in the direction indicated for each branch.

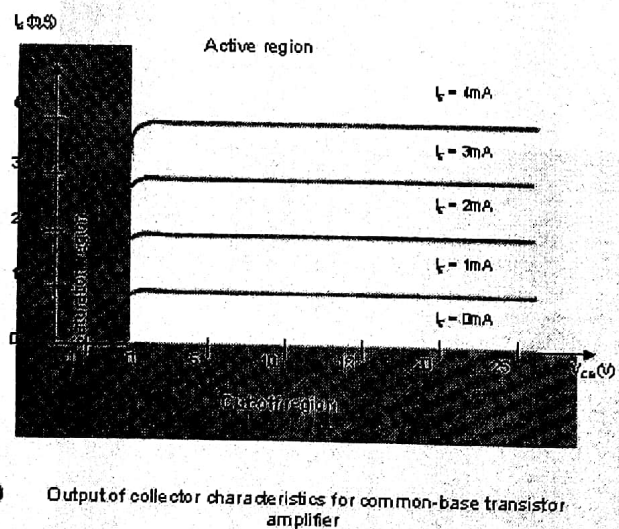
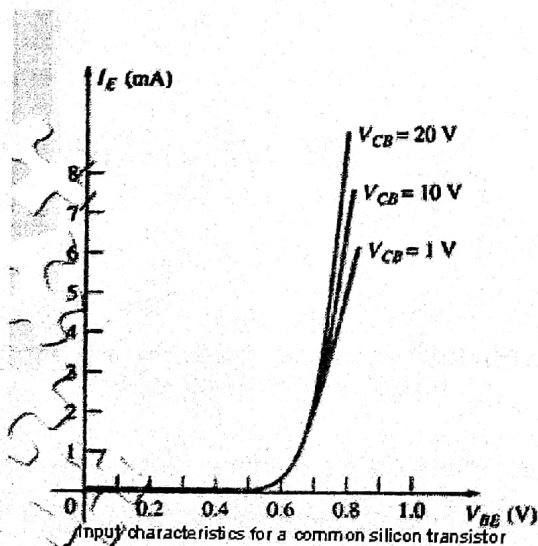


To describe the behavior of common-base amplifiers requires two set of characteristics:

1. Input or driving point characteristics.
2. Output or collector characteristics

The output characteristics has 3 basic regions:

- Active region –defined by the biasing arrangements
- Cutoff region – region where the collector current is 0A
- Saturation region- region of the characteristics to the left of $V_{CB} = 0V$

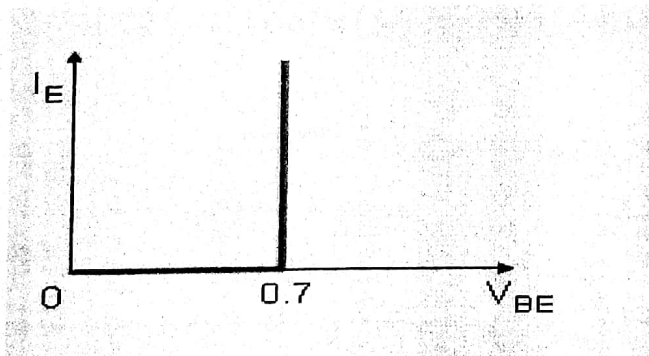


Active region	Saturation region	Cut-off region
• I_E increased, I_C increased • BE junction forward bias and CB junction reverse bias • Refer to the graf, $I_C \approx I_E$ • I_C not depends on V_{CB} • Suitable region for the transistor working as amplifier	• BE and CB junction is forward bias • Small changes in V_{CB} will cause big different to I_C • The allocation for this region is to the left of $V_{CB} = 0$ V.	• Region below the line of $I_E = 0$ A • BE and CB is reverse bias • no current flow at collector, only leakage current

The curves (output characteristics) clearly indicate that a first approximation to the relationship between I_E and I_C in the active region is given by

$$I_C \approx I_E$$

Once a transistor is in the 'on' state, the base-emitter voltage will be assumed to be $V_{BE} = 0.7$ V



In the dc mode the level of I_C and I_E due to the majority carriers are related by a quantity called alpha $\alpha = \alpha_{dc}$

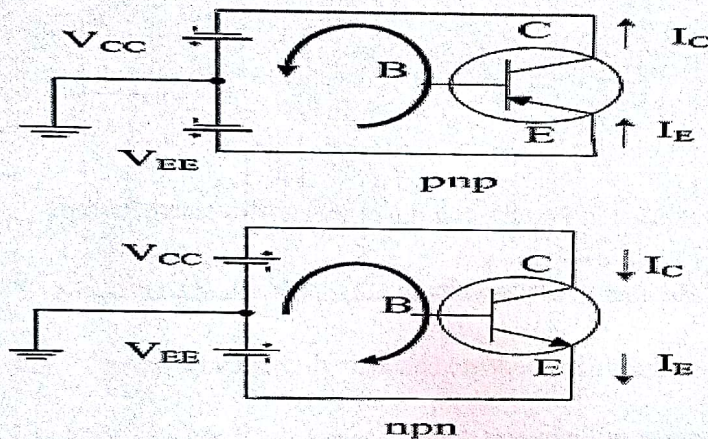
$$I_C = \alpha I_E + I_{CBO}$$

It can then be summarize to $I_C = \alpha I_E$ (ignore I_{CBO} due to small value)

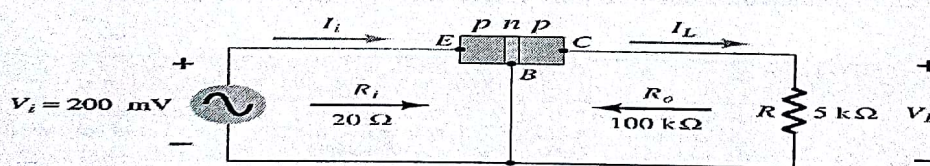
For ac situations where the point of operation moves on the characteristics curve, an ac alpha defined by α_{ac}

Alpha a common base current gain factor that shows the efficiency by calculating the current percent from current flow from emitter to collector. The value of α is typical from 0.9 ~ 0.998.

Biasing: Proper biasing CB configuration in active region by approximation $I_C \approx I_E$ ($I_B \approx 0$ uA)



4.6 TRANSISTOR AS AN AMPLIFIER



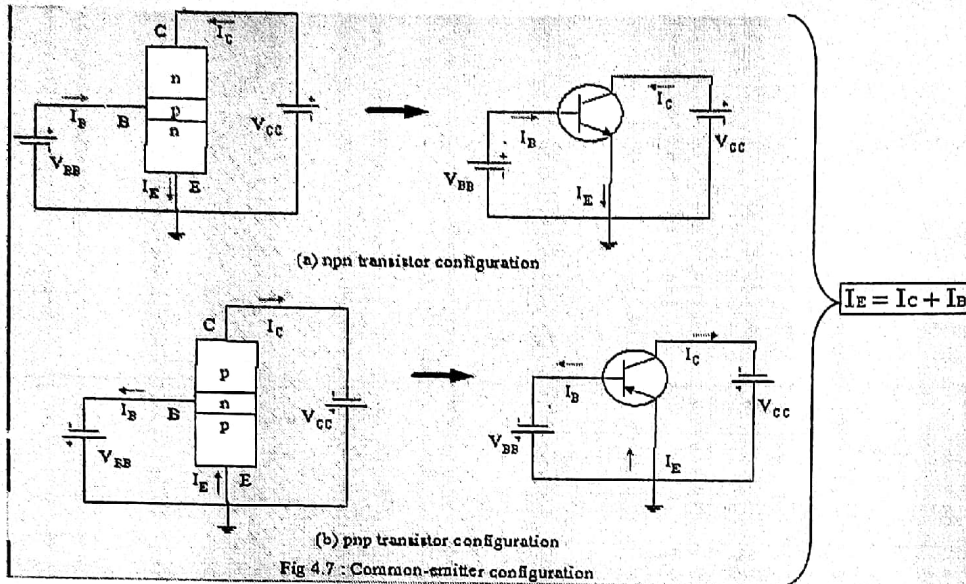
Common-Emitter Configuration

It is called common-emitter configuration since : emitter is common or reference to both input and output terminals. emitter is usually the terminal closest to or at ground potential.

Almost amplifier design is using connection of CE due to the high gain for current and voltage.

Two set of characteristics are necessary to describe the behavior for CE ;input (base terminal) and output (collector terminal) parameters.

Proper Biasing common-emitter configuration in active region

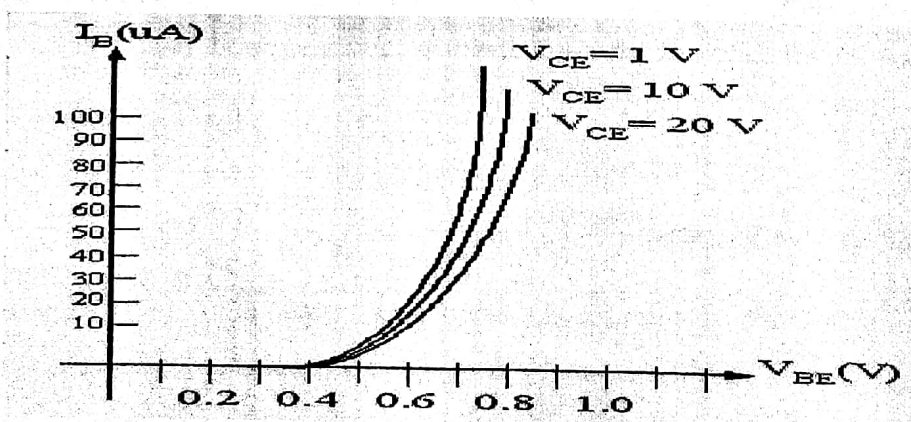


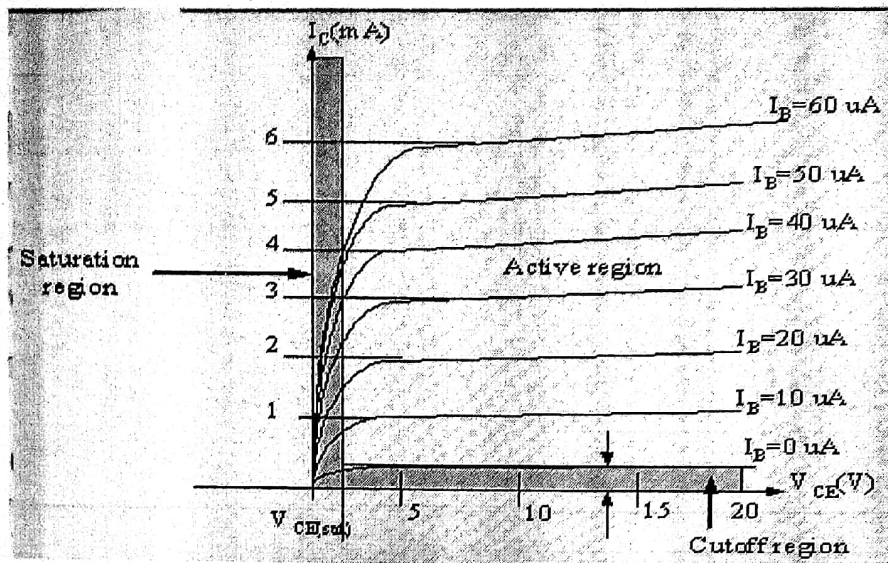
I_B is microamperes compared to miliamperes of I_C .

I_B will flow when $V_{BE} > 0.7V$ for silicon and $0.3V$ for germanium

Before this value I_B is very small and no I_B .

Base-emitter junction is forward bias Increasing V_{CE} will reduce I_B for different values.





Output characteristics for a common-emitter npn transistor

For small V_{CE} ($V_{CE} < V_{CE(sat)}$, I_C increase linearly with increasing of V_{CE}

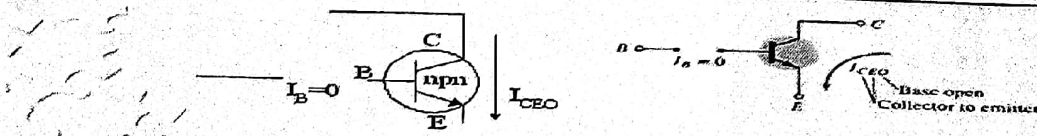
$V_{CE} > V_{CE(sat)}$ I_C not totally depends on $V_{CE} \rightarrow$ constant I_C

I_B (uA) is very small compare to I_C (mA). Small increase in I_B cause big increase in I_C

$I_B = 0$ A $\rightarrow I_{CEO}$ occur.

Noticing the value when $I_C = 0$ A. There is still some value of current flows.

Active region	Saturation region	Cut-off region
- B-E junction is forward bias - C-B junction is reverse bias - can be employed for voltage, current and power amplification	- B-E and C-B junction is forward bias, thus the values of I_B and I_C is too big. - The value of V_{CE} is so small. - Suitable region when the transistor as a logic switch. - NOT and avoid this region when the transistor as an amplifier.	- region below $I_B = 0 \mu A$ is to be avoided if an undistorted o/p signal is required - B-E junction and C-B junction is reverse bias $I_B = 0$, I_C not zero, during this condition $I_C = I_{CEO}$ where is this current flow when B-E is reverse bias.

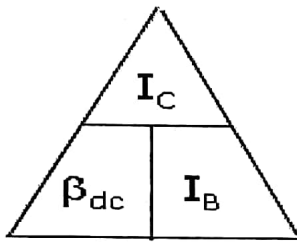


Beta (β) or amplification factor

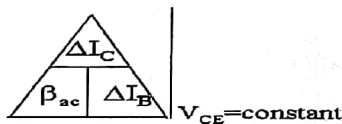
The ratio of dc collector current (I_C) to the dc base current (I_B) is dc beta (β_{dc}) which is dc current gain where I_C and I_B are determined at a particular operating point, Q-point (quiescent point). It's define by the following equation:

$$30 < \beta_{dc} < 300 \rightarrow 2N3904$$

On data sheet, $\beta_{dc}=h_{fe}$ with h is derived from ac hybrid equivalent cct. FE are derived from forward-current amplification and common-emitter configuration respectively.



For ac conditions, an ac beta has been defined as the changes of collector current (I_C) compared to the changes of base current (I_B) where I_C and I_B are determined at operating point. On data sheet, $\beta_{ac}=h_{fe}$ It can defined by the following equation:



From output characteristics of commonemitter configuration, find β_{ac} and β_{dc} with an

Operating point at $I_B=25 \mu A$ and $V_{CE}=7.5V$

$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B} \bigg|_{V_{CE} = \text{constant}}$$

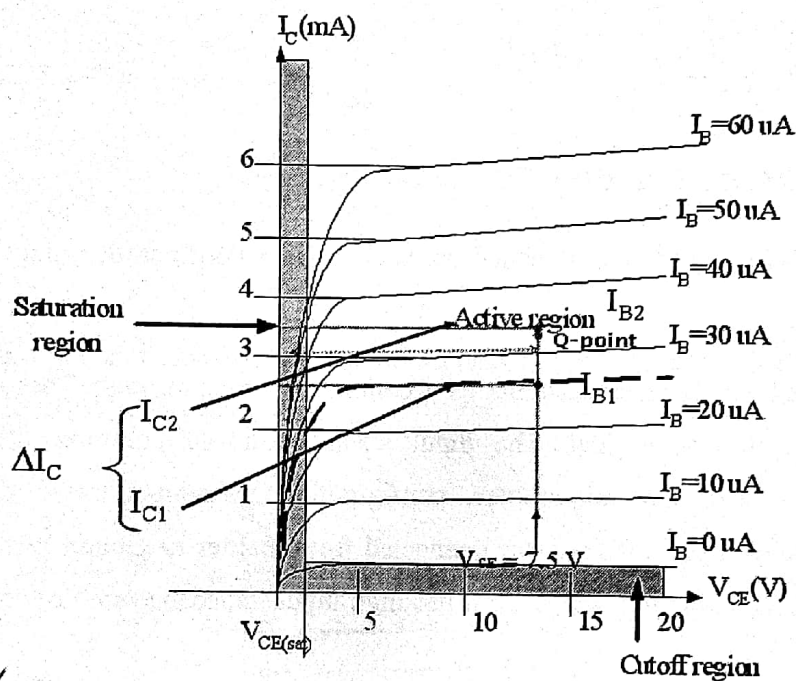
$$= \frac{I_{C2} - I_{C1}}{I_{B2} - I_{B1}} = \frac{3.2 \text{ mA} - 2.2 \text{ mA}}{30 \mu\text{A} - 20 \mu\text{A}}$$

$$= \frac{1 \text{ mA}}{10 \mu\text{A}} = 100$$

$$\beta_{dc} = \frac{I_C}{I_B}$$

$$= \frac{2.7 \text{ mA}}{25 \mu\text{A}}$$

$$= 108$$



Relationship analysis between α and β

CASE 2

$$\text{known} : \alpha = \frac{I_C}{I_E} \Rightarrow I_E = \frac{I_C}{\alpha} \quad (2)$$

$$\text{known} : \beta = \frac{I_C}{I_B} \Rightarrow I_B = \frac{I_C}{\beta} \quad (3)$$

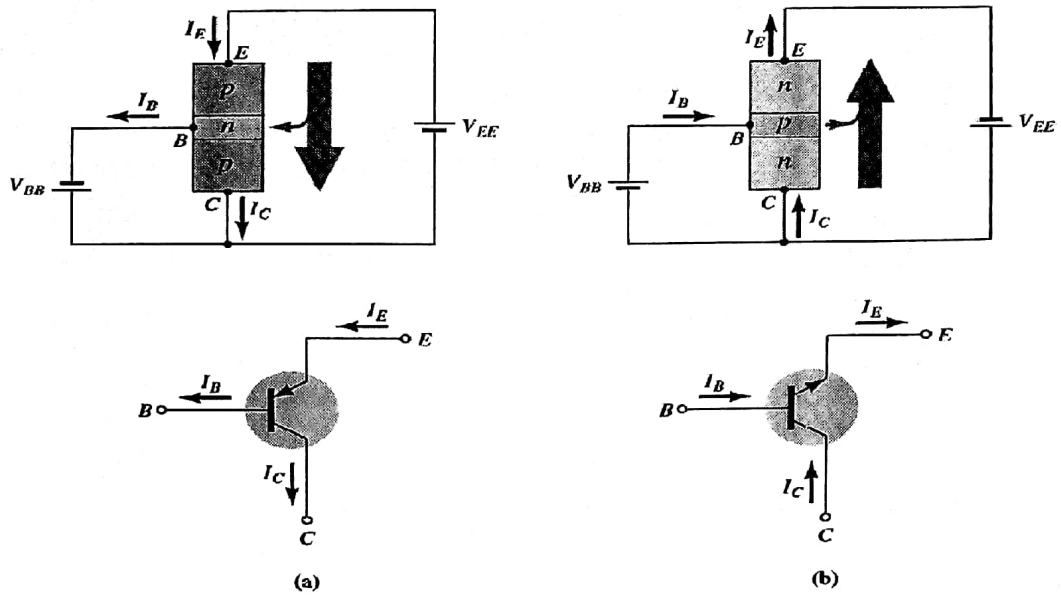
substitute (2) and (3) into (1) we get,

$$\alpha = \frac{\beta}{\beta + 1} \quad \text{and} \quad \beta = \frac{\alpha}{1 - \alpha}$$

4.7 COMMON – COLLECTOR CONFIGURATION

Also called emitter-follower (EF). It is called common-emitter configuration since both the signal

source and the load share the collector terminal as a common connection point. The output voltage is obtained at emitter terminal. The input characteristic of common-collector configuration is similar with common-emitter. configuration. Common-collector circuit configuration is provided with the load resistor connected from emitter to ground. It is used primarily for impedance-matching purpose since it has high input impedance and low output impedance.



For the common-collector configuration, the output characteristics are a plot of I_E vs V_{CE} for a range of values of I_B .

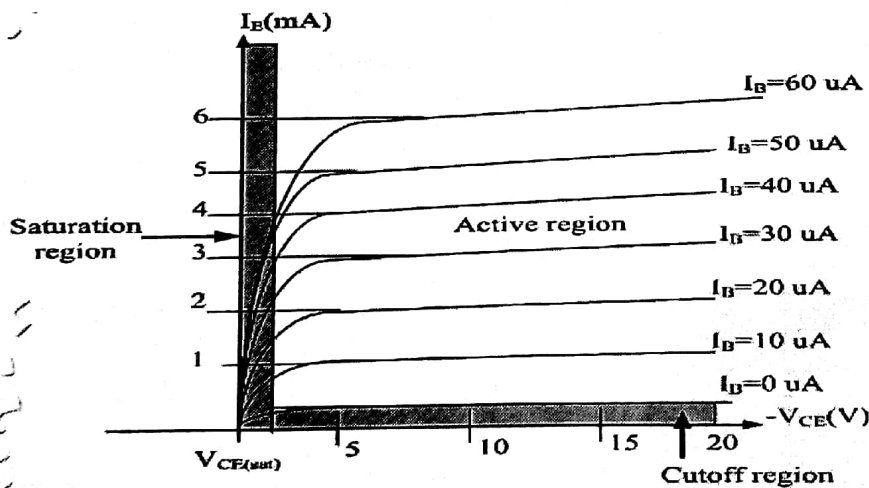


Fig 4.9 : Output characteristic in CC configuration for npn transistor

Limits of operation

Many BJT transistor used as an amplifier. Thus it is important to notice the limits of operations. At least 3 maximum values is mentioned in data sheet.

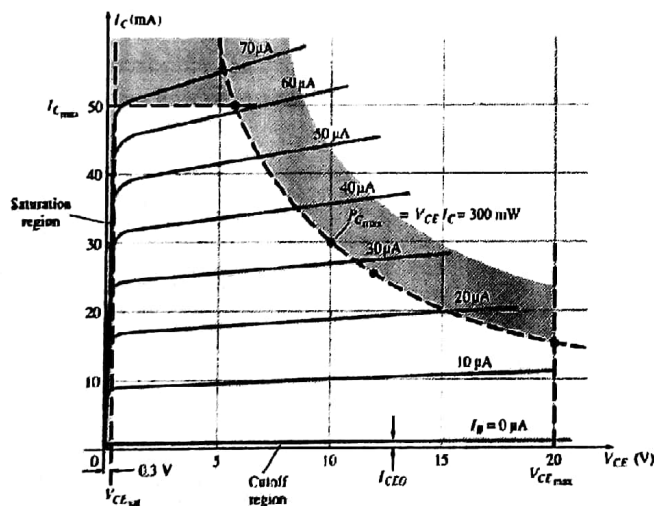
There are:

- Maximum power dissipation at collector: P_{Cmax} or P_D
- Maximum collector-emitter voltage: V_{CEmax} sometimes named as $V_{BR(CEO)}$ or V_{CEO} .
- Maximum collector current: I_{Cmax}

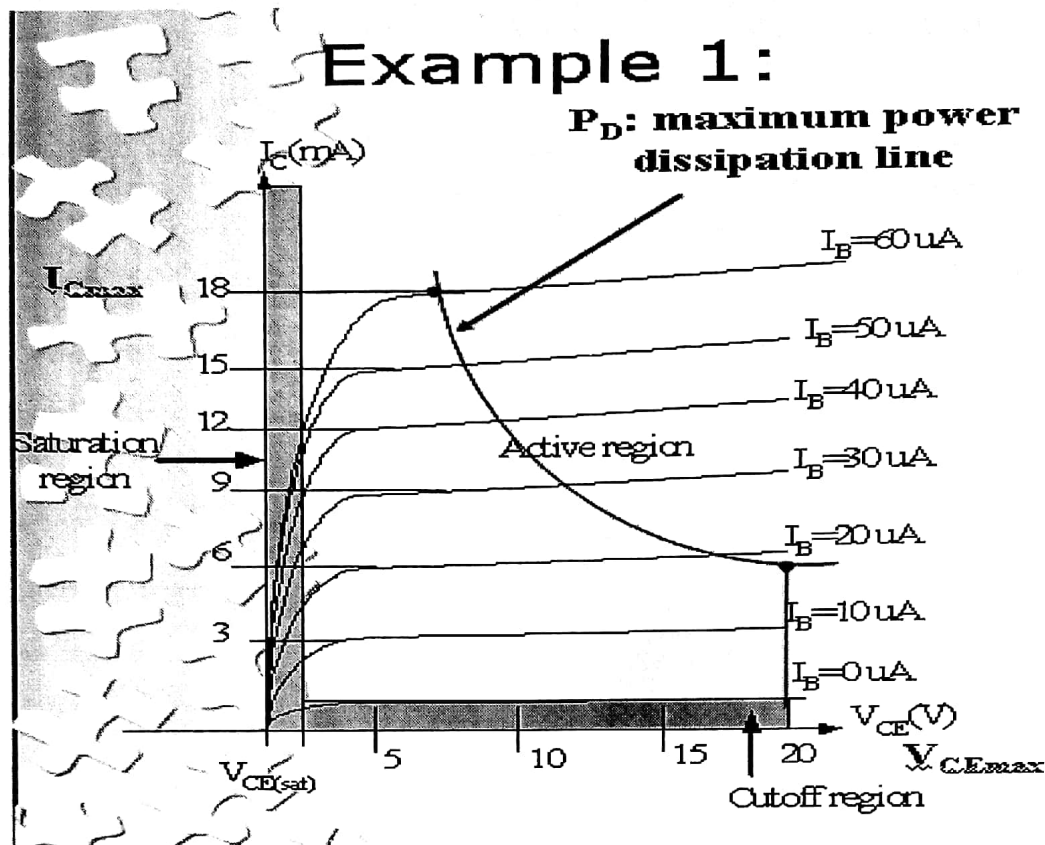
There are few rules that need to be followed for BJT transistor used as an amplifier. The rules are: transistor need to be operate in active region!

$$I_C < I_{Cmax}$$

$$P_C < P_{Cmax}$$



Note: V_{CE} is at maximum and I_C is at minimum ($I_{Cmax}=I_{CEO}$) in the cutoff region. I_C is at maximum and V_{CE} is at minimum ($V_{CE max} = V_{cesat} = V_{CEO}$) in the saturation region. The transistor operates in the active region between saturation and cutoff.



Refer to the fig. Example; A derating factor of 2mW/°C indicates the power dissipation is reduced 2mW each degree centigrade increase of temperature.

Step 1:

The maximum collector power dissipation,

$$P_D = I_{Cmax} \times V_{CEmax} = 18\text{m} \times 20 = 360 \text{ mW}$$

Step 2:

At any point on the characteristics the product of and must be equal to 360 mW.

Ex. 1. If choose $I_{Cmax} = 5 \text{ mA}$, substitute into the (1), we get

$$V_{CEmax} I_{Cmax} = 360 \text{ mW}$$

$$V_{CEmax}(5 \text{ m}) = 360/5 = \underline{7.2 \text{ V}}$$

Ex.2. If choose $V_{CEmax}=18\text{ V}$, substitute into (1), we get

$$V_{CEmax}I_{Cmax} = 360\text{ mW}$$

$$(10) I_{Cmax} = 360\text{m}/18 = \underline{20\text{ mA}}$$

Derating P_{Dmax}

P_{Dmax} is usually specified at 25°C .

The higher temperature goes, the less is P_{Dmax}

Example; A derating factor of $2\text{mW}/^{\circ}\text{C}$ indicates the power dissipation is reduced 2mW each degree centigrade increase of temperature.

Comparison of Transistor Configurations

Characteristics	Common Base	Common Emitter	Common Collector
Input Resistance (R_i)	Very low ($\approx 1\Omega$)	Low ($\approx 1k\Omega$)	High ($\approx 100k\Omega$)
Output Resistance (R_o)	Very high ($\approx 1M\Omega$)	High ($\approx 10k\Omega$)	Low ($\approx 1\Omega$)
Input Current	I_E	I_B	I_C
Output Current	I_C	I_C	I_E
Input voltage applied between	Emitter & base	Base & Emitter	Base & Collector
Output voltage taken between	Collector & base	Collector & Emitter	Emitter & Collector
Current Amplification factor	$\alpha = \frac{I_C}{I_E}$	$\beta = \frac{I_C}{I_B}$	$\gamma = \frac{I_E}{I_B}$
Current gain (A_i)	Less than unity	High (20 to few hundred)	High (20 to few hundred)
Voltage gain (A_v)	Medium $\approx 360^\circ$	Medium 180°	Less than unity $\approx 360^\circ$
Phase shift Applications	As a 1/2 stage of multistage amp	For audio signal amp.	For impedance matching.

Transistor Typical Junction Voltage Values

Type	$V_{BE sat}$	$V_{BE sat}$	$V_{BE active}$	$V_{BE cut in}$	$V_{BE cut off}$
Si	0.3	0.7	0.6	0.5	0.0 -0.1
Ge	0.1	0.3	0.2	0.1	

N-P-N transistor Junction voltages at $25^\circ C$

FIELD EFFECT TRANSISTOR

INTRODUCTION

1. The Field effect transistor is abbreviated as FET , it is an another semiconductor device like a BJT which can be used as an amplifier or switch.
2. The Field effect transistor is a voltage operated device. Whereas Bipolar junction transistor is a current controlled device. Unlike BJT a FET requires virtually no input current.
3. This gives it an extremely high input resistance , which is its most important advantage over a bipolar transistor.
4. FET is also a three terminal device, labeled as source, drain and gate.
5. The source can be viewed as BJT's emitter, the drain as collector, and the gate as the counter part of the base.
6. The material that connects the source to drain is referred to as the channel.
7. FET operation depends only on the flow of majority carriers ,therefore they are called uni polar devices. BJT operation depends on both minority and majority carriers.
8. As FET has conduction through only majority carriers it is less noisy than BJT.
9. FETs are much easier to fabricate and are particularly suitable for ICs because they occupy less space than BJTs.
10. FET amplifiers have low gain bandwidth product due to the junction capacitive effects and produce more signal distortion except for small signal operation.
11. The performance of FET is relatively unaffected by ambient temperature changes. As it has a negative temperature coefficient at high current levels, it prevents the FET from thermal breakdown. The BJT has a positive temperature coefficient at high current levels which leads to thermal breakdown.

CLASSIFICATION OF FET:

There are two major categories of field effect transistors:

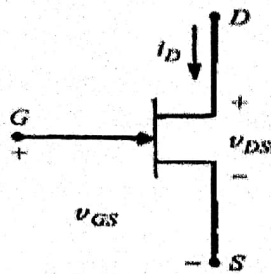
1. Junction Field Effect Transistors
2. MOSFETs

These are further sub divided in to P- channel and N-channel devices.

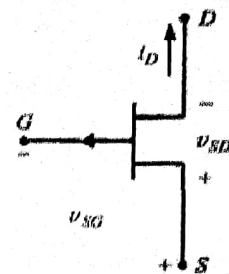
MOSFETs are further classified in to two types Depletion MOSFETs and Enhancement . MOSFETs

When the channel is of N-type the JFET is referred to as an N-channel JFET ,when the channel is of P-type the JFET is referred to as P-channel JFET.

The schematic symbols for the P-channel and N-channel JFETs are shown in the figure.



N-channel FET

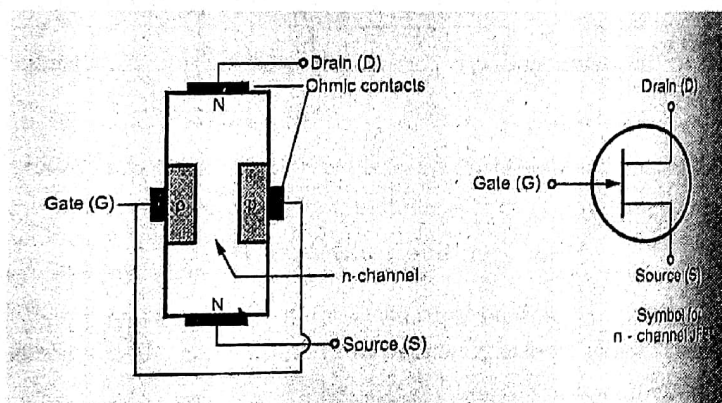


P-channel FET

CONSTRUCTION AND OPERATION OF N- CHANNEL FET

If the gate is an N-type material, the channel must be a P-type material.

CONSTRUCTION OF N-CHANNEL JFET



A piece of N- type material, referred to as channel has two smaller pieces of P-type material attached to its sides, forming PN junctions. The channel ends are designated as the drain and source . And the two pieces of P-type material are connected together and their terminal is called the gate. Since this channel is in the N-type bar, the FET is known as N-channel JFET.

OPERATION OF N-CHANNEL JFET:-

The overall operation of the JFET is based on varying the width of the channel to control the drain current.

A piece of N type material referred to as the channel, has two smaller pieces of P type material attached to its sites, farming PN -Junctions. The channel's ends are designated the

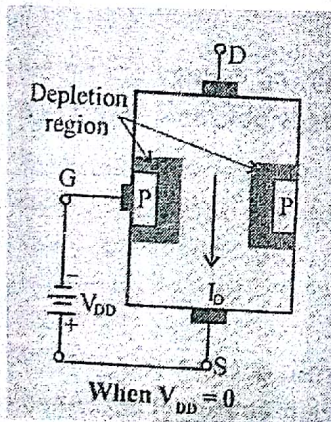
drain and the source. And the two pieces of P type material are connected together and their terminal is called the gate. With the gate terminal not connected and the potential applied positive at the drain negative at the source a drain current I_d flows. When the gate is biased negative with respect to the source the PN junctions are reverse biased and depletion regions are formed. The channel is more lightly doped than the P type gate blocks, so the depletion regions penetrate deeply into the channel. Since depletion region is a region depleted of charge carriers it behaves as an Insulator. The result is that the channel is narrowed. Its resistance is increased and I_d is reduced. When the negative gate bias voltage is further increased, the depletion regions meet at the center and I_d is cut off completely.

There are two ways to control the channel width

1. By varying the value of V_{gs}
2. And by Varying the value of V_{ds} holding V_{gs} constant

1 By varying the value of V_{gs} :-

We can vary the width of the channel and in turn vary the amount of drain current. This can be done by varying the value of V_{gs} . This point is illustrated in the fig below. Here we are dealing with N channel FET. So channel is of N type and gate is of P type that constitutes a PN junction. This PN junction is always reverse biased in JFET operation. The reverse bias is applied by a battery voltage V_{gs} connected between the gate and the source terminal i.e positive terminal of the battery is connected to the source and negative terminal to gate.

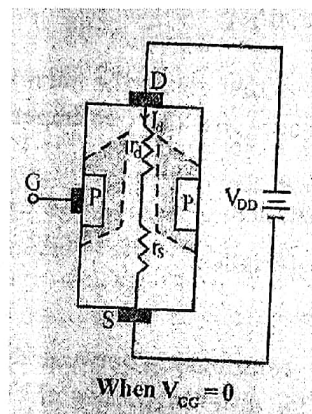
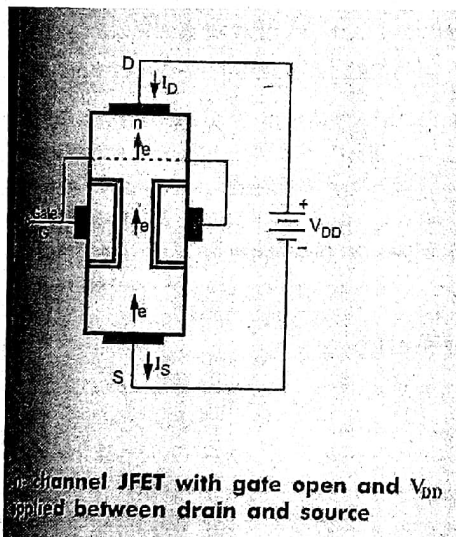


- 1) When a PN junction is reverse biased the electrons and holes diffuse across junction by leaving immobile ions on the N and P sides, the region containing these immobile ions is known as depletion regions.
- 2) If both P and N regions are heavily doped then the depletion region extends symmetrically on both sides.
- 3) But in N channel FET P region is heavily doped than N type thus depletion region extends more in N region than P region.

- 4) So when no V_{ds} is applied the depletion region is symmetrical and the conductivity becomes Zero. Since there are no mobile carriers in the junction.
- 5) As the reverse bias voltage is increases the thickness of the depletion region also increases. i.e. the effective channel width decreases .
- 6) By varying the value of V_{gs} we can vary the width of the channel.

2 Varying the value of V_{ds} holding V_{gs} constant :-

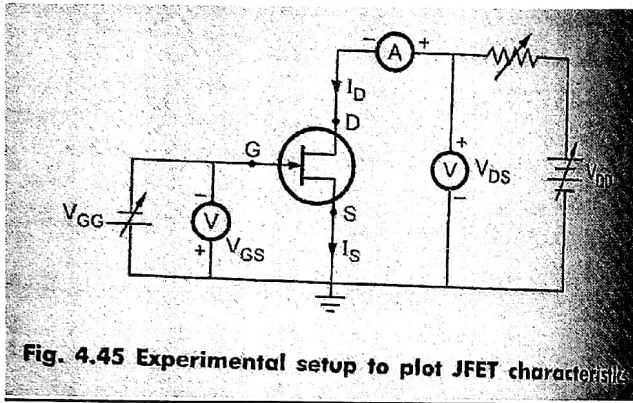
- 1) When no voltage is applied to the gate i.e. $V_{gs}=0$, V_{ds} is applied between source and drain the electrons will flow from source to drain through the channel constituting drain current I_d .
- 2) With $V_{gs}=0$ for $I_d=0$ the channel between the gate junctions is entirely open .In response to a small applied voltage V_{ds} , the entire bar acts as a simple semi conductor resistor and the current I_d increases linearly with V_{ds} .
- 3) The channel resistances are represented as r_d and r_s as shown in the fig.



- 4) This increasing drain current I_d produces a voltage drop across r_d which reverse biases the gate to source junction, ($r_d > r_s$) .Thus the depletion region is formed which is not symmetrical .
- 5) The depletion region i.e. developed penetrates deeper in to the channel near drain and less towards source because $V_{rd} \gg V_{rs}$. So reverse bias is higher near drain than at source.
- 6) As a result growing depletion region reduces the effective width of the channel. Eventually a voltage V_{ds} is reached at which the channel is pinched off. This is the voltage where the current I_d begins to level off and approach a constant value.

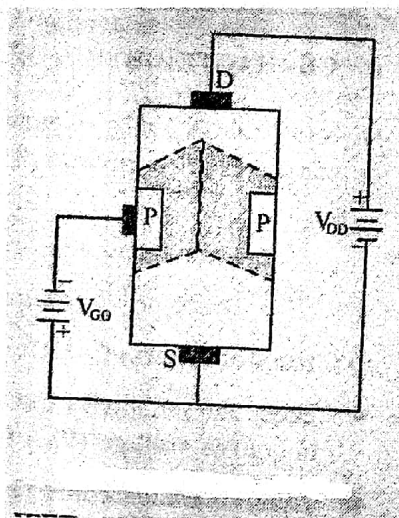
- 7) So, by varying the value of V_{ds} we can vary the width of the channel holding V_{gs} constant.

When both V_{gs} and V_{ds} is applied:-



It is of course in principle not possible for the channel to close Completely and there by reduce the current I_d to Zero for, if such indeed, could be the case the gate voltage V_{gs} is applied in the direction to provide additional reverse bias

- 1) When voltage is applied between the drain and source with a battery V_{dd} , the electrons flow from source to drain through the narrow channel existing between the depletion regions. This constitutes the drain current I_d , its conventional direction is from drain to source.
- 2) The value of drain current is maximum when no external voltage is applied between gate and source and is designated by I_{dss} .



- 3) When V_{GS} is increased beyond Zero the depletion regions are widened. This reduces the effective width of the channel and therefore controls the flow of drain current through the channel.
- 4) When V_{GS} is further increased a stage is reached at which the depletion regions touch each other that means the entire channel is closed with depletion region. This reduces the drain current to Zero.

CHARACTERISTICS OF N-CHANNEL JFET :-

The family of curves that shows the relation between current and voltage are known as characteristic curves.

There are two important characteristics of a JFET.

- 1) Drain or V_I Characteristics
- 2) Transfer characteristics

1. Drain Characteristics:-

Drain characteristics shows the relation between the drain to source voltage V_{DS} and drain current I_D . In order to explain typical drain characteristics let us consider the curve with $V_{GS} = 0.V$.

- 1) When V_{DS} is applied and it is increasing the drain current I_D also increases linearly up to knee point.
- 2) This shows that FET behaves like an ordinary resistor. This region is called as ohmic region.

- 3) I_D increases with increase in drain to source voltage. Here the drain current is increased slowly as compared to ohmic region.

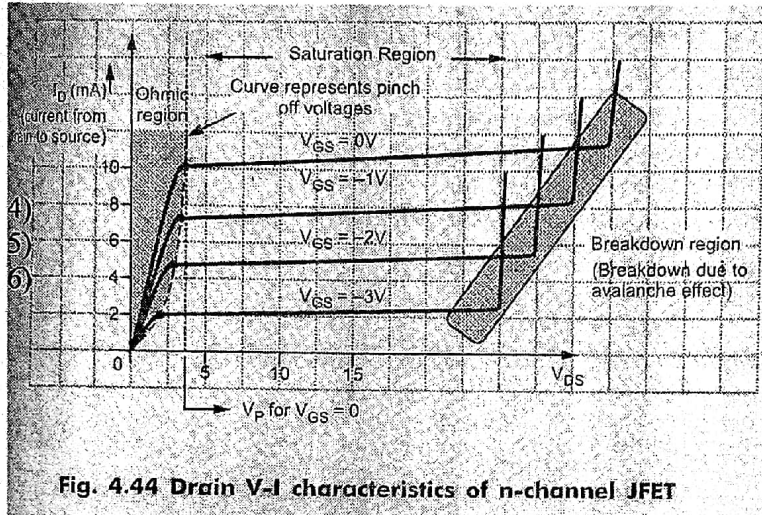


Fig. 4.44 Drain V-I characteristics of n-channel JFET

- 4) It is because of the fact that there is an increase in V_{DS} . This in turn increases the reverse bias voltage across the gate source junction. As a result of this depletion region grows in size thereby reducing the effective width of the channel.
- 5) All the drain to source voltage corresponding to point the channel width is reduced to a minimum value and is known as pinch off.
- 6) The drain to source voltage at which channel pinch off occurs is called pinch off voltage (V_P).

PINCH OFF Region:-

- 1) This is the region shown by the curve as saturation region.
- 2) It is also called as saturation region or constant current region. Because of the channel is occupied with depletion region, the depletion region is more towards the drain and less towards the source, so the channel is limited, with this only limited number of carriers are only allowed to cross this channel from source drain causing a current that is constant in this region. To use FET as an amplifier it is operated in this saturation region.
- 3) In this drain current remains constant at its maximum value I_{DSS} .
- 4) The drain current in the pinch off region depends upon the gate to source voltage and is given by the relation

$$I_d = I_{dss} [1 - V_{gs}/V_p]^2$$

This is known as shokley's relation.

BREAKDOWN REGION:-

- 1) The region is shown by the curve .In this region, the drain current increases rapidly as the drain to source voltage is increased.
- 2) It is because of the gate to source junction due to avalanche effect.
- 3) The avalanche break down occurs at progressively lower value of VDS because the reverse bias gate voltage adds to the drain voltage thereby increasing effective voltage across the gate junction
This causes

1. The maximum saturation drain current is smaller
2. The ohmic region portion decreased.
- 4) It is important to note that the maximum voltage VDS which can be applied to FET is the lowest voltage which causes available break down.

2. TRANSFER CHARACTERISTICS:-

These curves shows the relationship between drain current I_D and gate to source voltage V_{GS} for different values of V_{DS} .

- 1) First adjust the drain to source voltage to some suitable value , then increase the gate to source voltage in small suitable value.
- 2) Plot the graph between gate to source voltage along the horizontal axis and current I_D on the vertical axis. We shall obtain a curve like this.

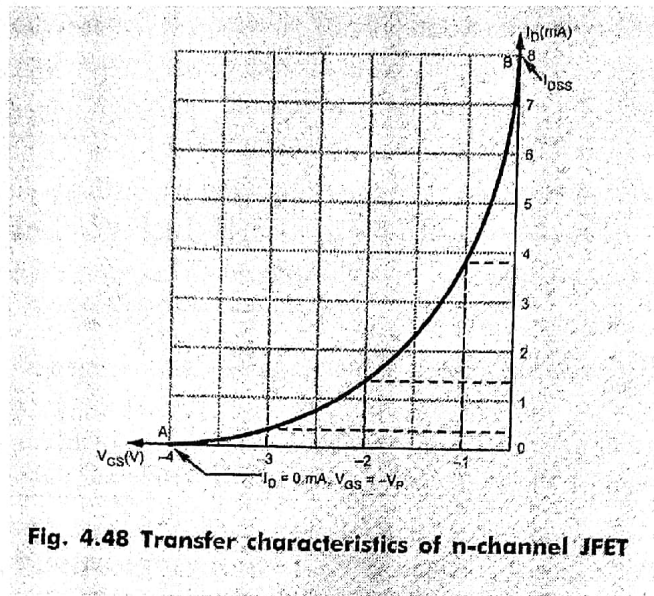


Fig. 4.48 Transfer characteristics of n-channel JFET

- 3) As we know that if V_{gs} is more negative curves drain current to reduce. where V_{gs} is made sufficiently negative, I_d is reduced to zero. This is caused by the widening of the depletion region to a point where it is completely closes the channel. The value of V_{gs} at the cutoff point is designed as $V_{gs\text{off}}$
- 4) The upper end of the curve as shown by the drain current value is equal to I_{dss} that is when $V_{gs} = 0$ the drain current is maximum.
- 5) While the lower end is indicated by a voltage equal to $V_{gs\text{off}}$
- 6) If V_{gs} continuously increasing, the channel width is reduced, then $I_d = 0$
- 7) It may be noted that curve is part of the parabola; it may be expressed as $I_d = I_{dss} [1 - V_{gs}/V_{gs\text{off}}]^2$

DIFFERENCE BETWEEN V_p AND $V_{gs\text{off}}$ -

V_p is the value of V_{gs} that causes the JFET to become constant current component, It is measured at $V_{gs} = 0V$ and has a constant drain current of $I_d = I_{dss}$. Where $V_{gs\text{off}}$ is the value of V_{gs} that reduces I_d to approximately zero.

Why the gate to source junction of a JFET be always reverse biased ?

The gate to source junction of a JFET is never allowed to become forward biased because the gate material is not designed to handle any significant amount of current. If the junction is allowed to become forward biased, current is generated through the gate material. This current may destroy the component.

There is one more important characteristic of JFET reverse biasing i.e. J FET 's have extremely high characteristic gate input impedance. This impedance is typically in the high mega ohm range. With the advantage of extremely high input impedance it draws no current from the source. The high input impedance of the JFET has led to its extensive use in integrated circuits. The low current requirements of the component makes it perfect for use in ICs. Where thousands of transistors must be etched on to a single piece of silicon. The low current draw helps the IC to remain relatively cool, thus allowing more components to be placed in a smaller physical area.

JFET PARAMETERS

The electrical behavior of JFET may be described in terms of certain parameters. Such parameters are obtained from the characteristic curves.

A C Drain resistance(r_d):

It is also called dynamic drain resistance and is the a.c.resistance between the drain and source terminal,when the JFET is operating in the pinch off or saturation region.It is given by the ratio of small change in drain to source voltage ΔV_{ds} to the corresponding change in drain current ΔI_d for a constant gate to source voltage V_{gs} .

Mathematically it is expressed as $r_d = \Delta V_{ds} / \Delta I_d$ where V_{gs} is held constant.

TRANSCONDUCTANCE (g_m):

It is also called forward transconductance . It is given by the ratio of small change in drain current (ΔI_d) to the corresponding change in gate to source voltage (ΔV_{gs})

Mathematically the transconductance can be written as

$$g_m = \Delta I_d / \Delta V_{gs}$$

AMPLIFICATION FACTOR (μ)

It is given by the ratio of small change in drain to source voltage (ΔV_{ds}) to the corresponding change in gate to source voltage (ΔV_{gs})for a constant drain current (I_d).

Thus $\mu = \Delta V_{ds} / \Delta V_{gs}$ when I_d held constant

The amplification factor μ may be expressed as a product of transconductance (g_m)and ac drain resistance (r_d)

$$\mu = \Delta V_{ds} / \Delta V_{gs} = g_m r_d$$

THE FET SMALL SIGNAL MODEL:-

The linear small signal equivalent circuit for the FET can be obtained in a manner similar to that used to derive the corresponding model for a transistor.

We can express the drain current i_D as a function f of the gate voltage and drain voltage V_{ds} .

$$I_d = f(V_{gs}, V_{ds}) \text{------(1)}$$

The transconductance g_m and drain resistance r_d :-

If both gate voltage and drain voltage are varied, the change in the drain current is approximated by using taylor's series considering only the first two terms in the expansion

$$\Delta i_d = \left. \frac{\partial i_d}{\partial V_{gs}} \right|_{V_{ds}=\text{constant}} \Delta V_{gs} + \left. \frac{\partial i_d}{\partial V_{ds}} \right|_{V_{gs}=\text{constant}} \Delta V_{ds}$$

we can write $\Delta i_d = i_d$

$$\Delta V_{gs} = V_{gs}$$

$$\Delta V_{ds} = V_{ds}$$

$$I_d = g_m V_{gs} + \frac{1}{r_d} V_{ds} \rightarrow (1)$$

$$\text{Where } g_m = \left. \frac{\partial i_d}{\partial V_{gs}} \right|_{V_{ds}} \approx \left. \frac{\Delta i_d}{\Delta V_{gs}} \right|_{V_{ds}}$$

$$g_m = \left. \frac{i_d}{V_{gs}} \right|_{V_{ds}}$$

Is the mutual conductance or transconductance .It is also called as g_{fs} or y_{fs} common source forward conductance .

The second parameter r_d is the drain resistance or output resistance is defined as

$$r_d = \left. \frac{\partial V_{ds}}{\partial i_d} \right|_{V_{gs}} \approx \left. \frac{\Delta V_{ds}}{\Delta i_d} \right|_{V_{gs}} = \left. \frac{V_{ds}}{i_d} \right|_{V_{gs}}$$

$$r_d = \left. \frac{V_{ds}}{i_d} \right|_{V_{gs}}$$

The reciprocal of the r_d is the drain conductance g_d .It is also designated by Y_{os} and G_{os} and called the common source output conductance . So the small signal equivalent circuit for FET can be drawn in two different ways.

1. small signal current –source model

2. small signal voltage-source model.

A small signal current -source model for FET in common source configuration can be drawn satisfying Eq $\Rightarrow$ (1) as shown in the figure(a)

This low frequency model for FET has a Norton's output circuit with a dependent current generator whose magnitude is proportional to the gate-to -source voltage. The proportionality factor is the transconductance ' g_m '. The output resistance is ' r_d '. The input resistance between the gate and source is infinite, since it is assumed that the reverse biased gate draws no current. For the same reason the resistance between gate and drain is assumed to be infinite.

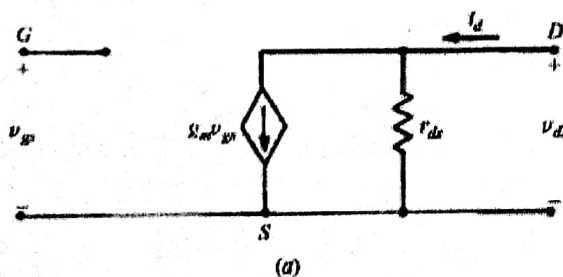
The small signal voltage-source model is shown in the figure(b).

This can be derived by finding the Thevenin's equivalent for the output part of fig(a) .

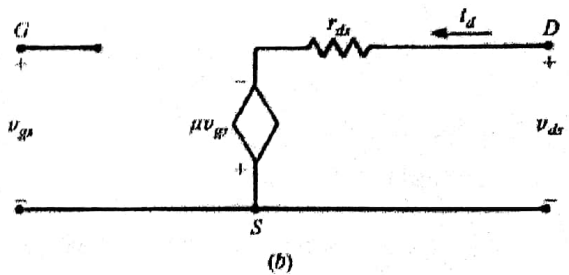
These small signal models for FET can be used for analyzing the three basic FET amplifier configurations:

1. common source (CS) 2. common drain (CD) or source follower
3. common gate(CG).

(a) Small Signal Current source model for FET



(b) Small Signal voltage source model for



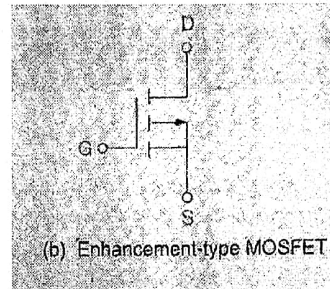
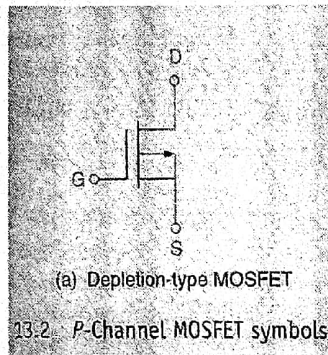
FET

Here the input circuit is kept open because of having high input impedance and the output circuit satisfies the equation for I_D

MOSFET:-

We now turn our attention to the insulated gate FET or metal oxide semi conductor FET which is having the greater commercial importance than the junction FET.

Most MOSFETs however are triodes, with the substrate internally connected to the source. The circuit symbols used by several manufacturers are indicated in the Fig below.



(a) Depletion type MOSFET

(b) Enhancement type MOSFET

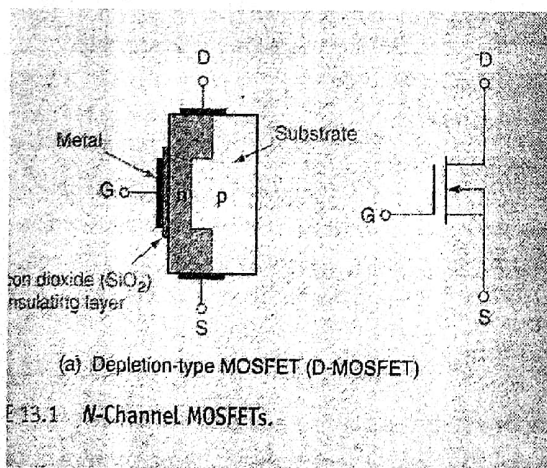
Both of them are P- channel

Here are two basic types of MOSFETS

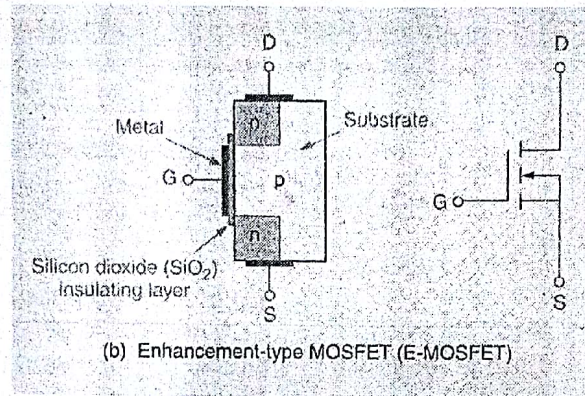
- (1) Depletion type (2) Enhancement type MOSFET.

D-MOSFETS can be operated in both the depletion mode and the enhancement mode. E MOSFETS are restricted to operate in enhancement mode. The primary difference between them is their physical construction.

The construction difference between the two is shown in the fig given below.



As we can see the D MOSFET have physical channel between the source and drain terminals(Shaded area)



The E MOSFET on the other hand has no such channel physically. It depends on the gate voltage to form a channel between the source and the drain terminals.

Both MOSFETS have an insulating layer between the gate and the rest of the component. This insulating layer is made up of SiO₂ a glass like insulating material. The gate material is made up of metal conductor. Thus going from gate to substrate, we can have metal oxide semiconductor which is where the term MOSFET comes from.

Since the gate is insulated from the rest of the component, the MOSFET is sometimes referred to as an insulated gate FET or IGFET.

The foundation of the MOSFET is called the substrate. This material is represented in the schematic symbol by the center line that is connected to the source.

In the symbol for the MOSFET, the arrow is placed on the substrate. As with JFET an arrow pointing in represents an N-channel device, while an arrow pointing out represents p-channel device.

CONSTRUCTION OF AN N-CHANNEL MOSFET:-

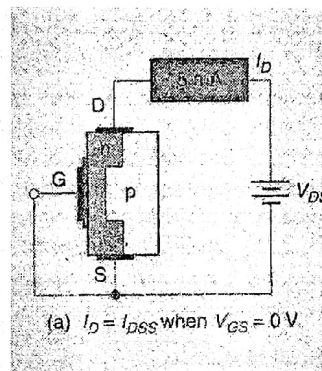
The N- channel MOSFET consists of a lightly doped p type substance into which two heavily doped n+ regions are diffused as shown in the Fig. These n+ sections, which will act as source and drain. A thin layer of insulation silicon dioxide (SiO₂) is grown over the surface of the structure, and holes are cut into oxide layer, allowing contact with the source and drain. Then the gate metal area is overlaid on the oxide, covering the entire channel region. Metal

contacts are made to drain and source and the contact to the metal over the channel area is the gate terminal. The metal area of the gate, in conjunction with the insulating dielectric oxide layer and the semiconductor channel, forms a parallel plate capacitor. The insulating layer of SiO_2

is the reason why this device is called the insulated gate field effect transistor. This layer results in an extremely high input resistance (10^{10} to 10^{15} ohms) for MOSFET.

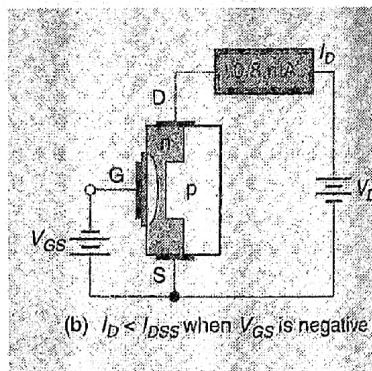
DEPLETION MOSFET

The basic structure of D-MOSFET is shown in the fig. An N-channel is diffused between source and drain with the device an appreciable drain current I_{DSS} flows for zero gate to source voltage, $V_{GS}=0$.



Depletion mode operation:-

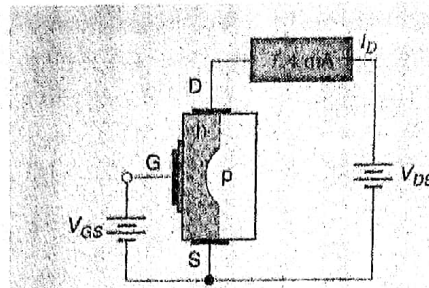
- 1) The above fig shows the D-MOSFET operating conditions with gate and source terminals shorted together ($V_{GS}=0V$)
- 2) At this stage $I_D = I_{DSS}$ where $V_{GS}=0V$, with this voltage V_{DS} , an appreciable drain current I_{DSS} flows.
- 3) If the gate to source voltage is made negative i.e. V_{GS} is negative. Positive charges are induced in the channel through the SiO_2 of the gate capacitor.
- 4) Since the current in a FET is due to majority carriers (electrons for an N-type material), the induced positive charges make the channel less conductive and the drain current drops as V_{GS} is made more negative.
- 5) The redistribution of charge in the channel causes an effective depletion of majority carriers, which accounts for the designation depletion MOSFET.
- 6) That means biasing voltage V_{GS} depletes the channel of free carriers. This effectively reduces the width of the channel, increasing its resistance.
- 7) Note that negative V_{GS} has the same effect on the MOSFET as it has on the JFET.



- 8) As shown in the fig above, the depletion layer generated by V_{GS} (represented by the white space between the insulating material and the channel) cuts into the channel, reducing its width. As a result, $I_D < I_{DSS}$. The actual value of I_D depends on the value of I_{DSS} , $V_{GS(off)}$ and V_{GS} .

Enhancement mode operation of the D-MOSFET:-

- 1) This operating mode is a result of applying a positive gate to source voltage V_{GS} to the device.
- 2) When V_{GS} is positive the channel is effectively widened. This reduces the resistance of the channel allowing I_D to exceed the value of I_{DSS}
- 3) When V_{GS} is given positive the majority carriers in the p-type are holes. The holes in the p type substrate are repelled by the +ve gate voltage.
- 4) At the same time, the conduction band electrons (minority carriers) in the p type material are attracted towards the channel by the +gate voltage.
- 5) With the build up of electrons near the channel, the area to the right of the physical channel effectively becomes an N type material.
- 6) The extended n type channel now allows more current, $I_D > I_{DSS}$



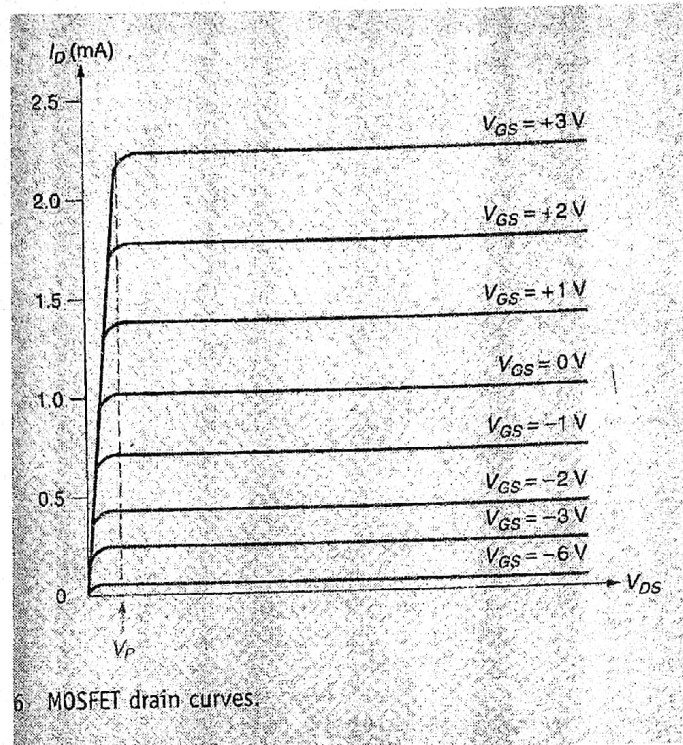
(c) $I_D > I_{DSS}$ when V_{GS} is positive

FIGURE 13.4 D-MOSFET operation.

Characteristics of Depletion MOSFET:-

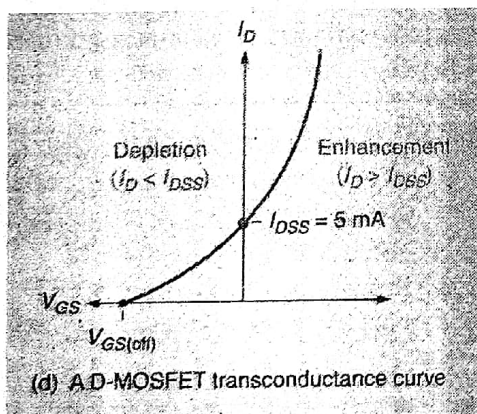
The fig. shows the drain characteristics for the N channel depletion type MOSFET

- 1) The curves are plotted for both V_{GS} positive and V_{GS} negative voltages
- 2) When $V_{GS}=0$ and negative the MOSFET operates in depletion mode when V_{GS} is positive, the MOSFET operates in the enhancement mode.
- 3) The difference between JFET and D MOSFET is that JFET does not operate for positive values of V_{GS} .
- 4) When $V_{DS}=0$, there is no conduction takes place between source to drain, if $V_{GS}<0$ and $V_{DS}>0$ then I_D increases linearly.
- 5) But as $V_{GS}=0$ induces positive charges holes in the channel, and controls the channel width. Thus the conduction between source to drain is maintained as constant, i.e. I_D is constant.
- 6) If $V_{GS}>0$ the gate induces more electrons in channel side, it is added with the free electrons generated by source. again the potential applied to gate determines the channel width and maintains constant current flow through it as shown in Fig



TRANSFER CHARACTERISTICS:-

The combination of 3 operating states i.e. $V_{GS}=0V$, $V_{GS}<0V$, $V_{GS}>0V$ is represented by the D MOSFET transconductance curve shown in Fig.



- 1) Here in this curve it may be noted that the region AB of the characteristics similar to that of JFET.
- 2) This curve extends for the positive values of V_{GS}

- 3) Note that $I_d = I_{dss}$ for $V_{gs} = 0V$ when V_{gs} is negative, $I_d < I_{dss}$ when $V_{gs} = V_{gs(off)}$, I_d is reduced to approximately $0mA$. Where V_{gs} is positive $I_d > I_{dss}$. So obviously I_{dss} is not the maximum possible value of I_d for a MOSFET.
- 4) The curves are similar to JFET so that the D MOSFET have the same transconductance equation.

APPLICATION OF MOSFET

One of the primary contributions to electronics made by MOSFETs can be found in the area of digital (computer electronics). The signals in digital circuits are made up of rapidly switching dc levels. This signal is called as a rectangular wave, made up of two dc levels (or logic levels). These logic levels are 0V and +5V.

A group of circuits with similar circuitry and operating characteristics is referred to as a logic family. All the circuits in a given logic family respond to the same logic levels, have similar speed and power-handling capabilities, and can be directly connected together. One such logic family is complementary MOS (or CMOS) logic. This logic family is made up entirely of MOSFETs.

COMPARISON OF MOSFET WITH JFET

- a. In enhancement and depletion types of MOSFET, the transverse electric field induced across an insulating layer deposited on the semiconductor material controls the conductivity of the channel.
- b. In the JFET the transverse electric field across the reverse biased PN junction controls the conductivity of the channel.
- c. The gate leakage current in a MOSFET is of the order of $10^{-12}A$. Hence the input resistance of a MOSFET is very high in the order of 10^{10} to $10^{15} \Omega$. The gate leakage current of a JFET is of the order of $10^{-9}A$, and its input resistance is of the order of $10^8 \Omega$.
- d. The output characteristics of the JFET are flatter than those of the MOSFET, and hence the drain resistance of a JFET (0.1 to $1M\Omega$) is much higher than that of a MOSFET (1 to $50k\Omega$).
- e. JFETs are operated only in the depletion mode. The depletion type MOSFET may be operated in both depletion and enhancement mode.
- f. Comparing to JFET, MOSFETs are easier to fabricate.

- g. Special digital CMOS circuits are available which involve near zero power dissipation and very low voltage and current requirements. This makes them suitable for portable systems.

UNIT – 5

TRANSISTOR BIASING

AND

THERMAL STABILIZATION

UNIT-V

TRANSISTOR BIASING AND STABILIZATION

5.1 NEED FOR TRANSISTOR BIASING:

If the o/p signal must be a faithful reproduction of the i/p signal, the transistor must be operated in active region. That means an operating point has to be established in this region. To establish an operating point (proper values of collector current I_c and collector to emitter voltage V_{CE}) appropriate supply voltages and resistances must be suitably chosen in the ckt. This process of selecting proper supply voltages and resistance for obtaining desired operating point or Q point is called as biasing and the ckt used for transistor biasing is called as biasing ckt.

There are four conditions to be met by a transistor so that it acts as a faithful ampr:

- 1) Emitter base junction must be forward biased ($V_{BE}=0.7V$ for Si, $0.2V$ for Ge) and collector base junction must be reverse biased for all levels of i/p signal.
- 2) V_{ce} voltage should not fall below $V_{CE(sat)}$ ($0.3V$ for Si, $0.1V$ for Ge) for any part of the i/p signal. For V_{CE} less than $V_{CE(sat)}$ the collector base junction is not probably reverse biased.
- 3) The value of the signal I_c when no signal is applied should be at least equal to the max. collector current I_{c0} due to signal alone.
- 4) Max. rating of the transistor $I_{c(max)}$, $V_{CE(max)}$ and $P_{D(max)}$ should not be exceeded at any value of i/p signal.

Consider the fig shown in fig1. If operating point is selected at A, A represents a condition when no bias is applied to the transistor i.e, $I_c=0$, $V_{CE}=0$. It does not satisfy the above said conditions necessary for faithful amplification.

Point C is too close to $P_{D(max)}$ curve of the transistor. Therefore the o/p voltage swing in the positive direction is limited.

Point B is located in the middle of active region. It will allow both positive and negative half cycles in the o/p signal. It also provides linear gain and larger possible o/p voltages and currents

Hence operating point for a transistor amplifier is selected to be in the middle of active region.

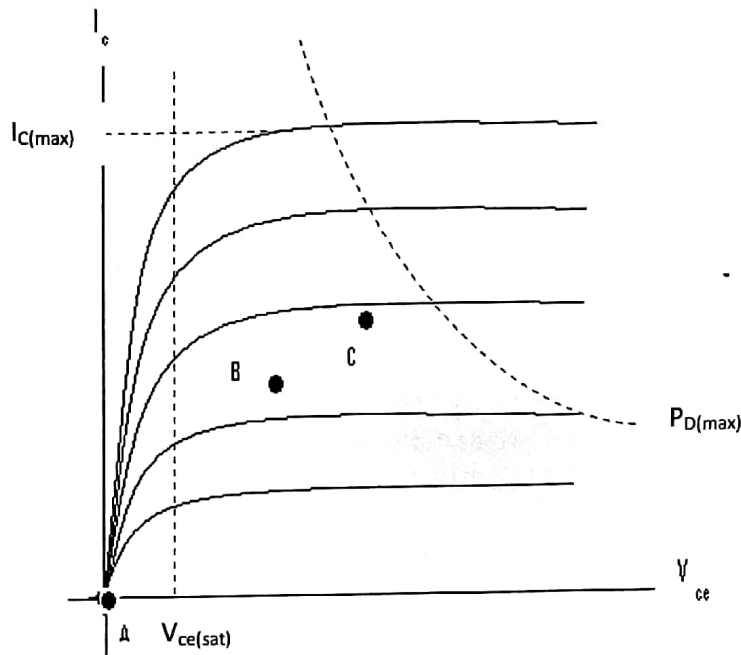


fig1

5.2 DC LOAD LINE:

Referring to the biasing circuit of fig 4.2a, the values of V_{CC} and R_C are fixed and I_C and V_{CE} are dependent on R_B .

Applying Kirchhoff's voltage law to the collector circuit in fig. 4.2a, we get

$$V_{CC} = I_C R_C + V_{CE}$$

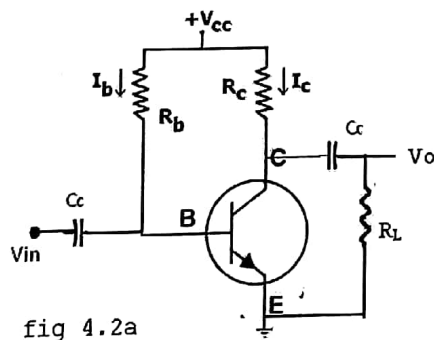


fig 4.2a

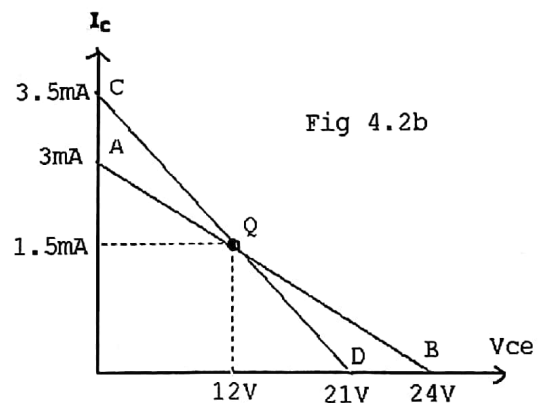


Fig 4.2b

The straight line represented by AB in fig4.2b is called the dc load line. The coordinates of the end point A are obtained by substituting $V_{CE} = 0$ in the above equation. Then $I_C = \frac{V_{CC}}{R_C}$.

Therefore The coordinates of A are $V_{CE} = 0$ and $I_C = \frac{V_{CC}}{R_C}$.

The coordinates of B are obtained by substituting $I_c=0$ in the above equation. Then $V_{ce} = V_{cc}$. Therefore the coordinates of B are $V_{CE} = V_{cc}$ and $I_c=0$. Thus the dc load line AB can be drawn if the values of R_c and V_{cc} are known.

As shown in the fig4.2b, the optimum POINT IS LOCATED AT THE MID POINT OF THE MIDWAY BETWEEN a AND b. In order to get faithful amplification, the Q point must be well within the active region of the transistor.

Even though the Q point is fixed properly, it is very important to ensure that the operating point remains stable where it is originally fixed. If the Q point shifts nearer to either A or B, the output voltage and current get clipped, thereby o/p signal is distorted.

In practice, the Q-point tends to shift its position due to any or all of the following three main factors.

- 1) Reverse saturation current, I_{co} , which doubles for every 10°C raise in temperature
- 2) Base emitter Voltage, V_{BE} , which decreases by $2.5 \text{ mV per } ^\circ\text{C}$
- 3) Transistor current gain, h_{FE} or β which increases with temperature.

If base current I_B is kept constant since I_B is approximately equal to V_{cc}/R_B . If the transistor is replaced by another one of the same type, one cannot ensure that the new transistor will have identical parameters as that of the first one. Parameters such as β vary over a range. This results in the variation of collector current I_c for a given I_B . Hence, in the o/p characteristics, the spacing between the curves might increase or decrease which leads to the shifting of the Q-point to a location which might be completely unsatisfactory.

5.3 AC LOAD LINE:

After drawing the dc load line, the operating point Q is properly located at the center of the dc load line. This operating point is chosen under zero input signal condition of the circuit. Hence the ac load line should also pass through the operating point Q. The effective ac load resistance R_{ac} , is a combination of R_c parallel to R_L i.e. $R_{ac} = R_L || R_c$. So the slope of the ac load line CQD will be $\left(\frac{-1}{R_{ac}}\right)$. To draw the ac load line, two end points, i.e. $V_{CE(max)}$ and $I_{C(max)}$ when the signal is applied are required.

$$V_{CE(max)} = V_{CEQ} + I_{CQ}R_{ac}, \text{ which locates point D on the } V_{ce} \text{ axis.}$$

$$I_{C(max)} = I_{CQ} + \frac{V_{CEQ}}{R_{ac}}, \text{ which locates the point C on the } I_c \text{ axis.}$$

By joining points c and D, ac load line CD is constructed. As $R_c > R_{ac}$, The dc load line is less steep than ac load line.

5.4 STABILITY FACTOR (S):

The rise of temperature results in increase in the value of transistor gain β and the leakage current I_{CO} . So, I_C also increases which results in a shift in operating point. Therefore, The biasing network should be provided with thermal stability. Maintenance of the operating point is specified by S , which indicates the degree of change in operating point due to change in temperature.

The extent to which I_C is stabilized with varying I_C is measured by a stability factor S

$$S = \frac{\partial I_C}{\partial I_{CO}} \approx \frac{dI_C}{dI_{CO}} \approx \frac{\Delta I_C}{\Delta I_{CO}}, \beta \text{ and } I_B \text{ constant}$$

$$\text{For CE configuration } I_C = \beta I_B + (1 + \beta) I_{CO}$$

Differentiate the above equation w.r.t I_C , We get

$$1 = \beta \frac{dI_B}{dI_C} + (1 + \beta) \frac{dI_{CO}}{dI_C}$$

$$\therefore \left(1 - \beta \frac{dI_B}{dI_C}\right) = \frac{(\beta + 1)}{S}$$

$$\therefore S = \frac{1 + \beta}{1 - \beta \frac{dI_B}{dI_C}}$$

S should be small to have better thermal stability.

Stability factor S' and S'' :

S' is defined as the rate of change of I_C with V_{BE} , keeping I_C and V_{BE} constant.

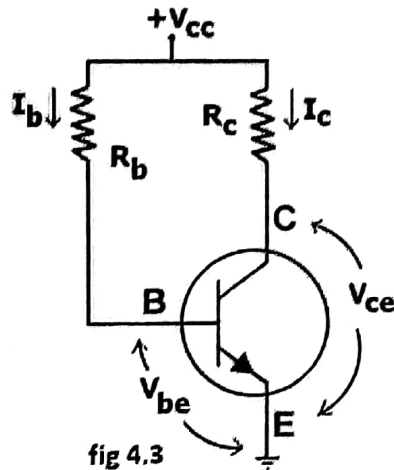
$$S' = \frac{\partial I_C}{\partial V_{BE}}$$

S'' is defined as the rate of change of I_C with β , keeping I_{CO} and V_{BE} constant.

$$S'' = \frac{\partial I_C}{\partial \beta}$$

5.5 METHODS OF TRANSISTOR BIASING:

1) Fixed bias (base bias)



This form of biasing is also called *base bias*. In the fig 4.3 shown, the single power source (for example, a battery) is used for both collector and base of a transistor, although separate batteries can also be used.

In the given circuit,

$$V_{cc} = I_B R_B + V_{be}$$

$$\text{Therefore, } I_B = (V_{cc} - V_{be})/R_B$$

Since the equation is independent of current $I_C R$, $dI_B/dI_C R = 0$ and the stability factor is given by the equation..... reduces to

$$S = 1 + \beta$$

Since β is a large quantity, this is very poor biasing circuit. Therefore in practice the circuit is not used for biasing.

For a given transistor, V_{be} does not vary significantly during use. As V_{cc} is of fixed value, on selection of R_B , the base current I_B is fixed. Therefore this type is called *fixed bias* type of circuit.

$$\text{Also for given circuit, } V_{cc} = I_C R_C + V_{ce}$$

$$\text{Therefore, } V_{ce} = V_{cc} - I_C R_C$$

Merits:

- It is simple to shift the operating point anywhere in the active region by merely changing the base resistor (R_B).
- A very small number of components are required.

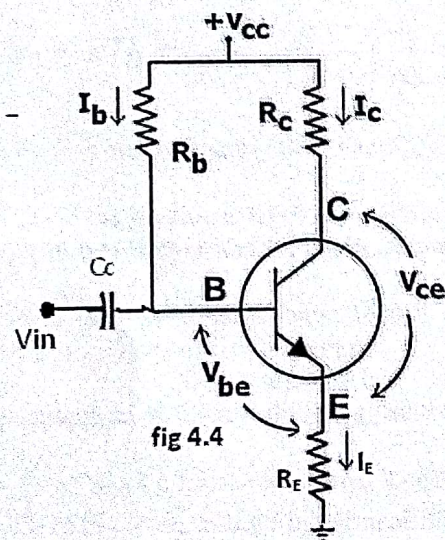
Demerits:

- The collector current does not remain constant with variation in temperature or power supply voltage. Therefore the operating point is unstable.
- Changes in V_{be} will change I_B and thus cause R_E to change. This in turn will alter the gain of the stage.
- When the transistor is replaced with another one, considerable change in the value of β can be expected. Due to this change the operating point will shift.

2) EMITTER-FEEDBACK BIAS:

The emitter feedback bias circuit is shown in the fig 4.4. The fixed bias circuit is modified by attaching an external resistor to the emitter. This resistor introduces negative feedback that stabilizes the Q-point. From Kirchhoff's voltage law, the voltage across the base resistor is

$$V_{Rb} = V_{CC} - I_e R_e - V_{be}.$$



From Ohm's law, the base current is

$$I_b = V_{Rb} / R_b.$$

The way feedback controls the bias point is as follows. If V_{be} is held constant and temperature increases, emitter current increases. However, a larger I_e increases the emitter voltage $V_e = I_e R_e$, which in turn reduces the voltage V_{Rb} across the base resistor. A lower base-resistor voltage drop reduces the base current, which results in less collector current because $I_c = \beta I_B$. Collector current and emitter current are related by $I_c = \alpha I_e$ with $\alpha \approx 1$, so increase in emitter current with temperature is opposed, and operating point is kept stable.

Similarly, if the transistor is replaced by another, there may be a change in I_C (corresponding to change in β -value, for example). By similar process as above, the change is negated and operating point kept stable.

For the given circuit,

$$I_B = (V_{CC} - V_{be}) / (R_B + (\beta + 1)R_E).$$

Merits:

The circuit has the tendency to stabilize operating point against changes in temperature and β -value.

Demerits:

- In this circuit, to keep I_C independent of β the following condition must be met:

$$I_C = \beta I_B = \frac{\beta(V_{CC} - V_{be})}{R_B + (\beta + 1)R_E} \approx \frac{(V_{CC} - V_{be})}{R_E}$$

which is approximately the case if $(\beta + 1)R_E \gg R_B$.

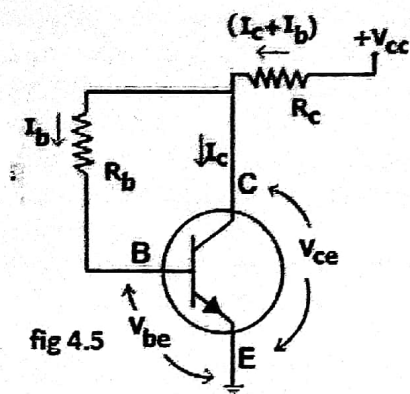
- As β -value is fixed for a given transistor, this relation can be satisfied either by keeping R_E very large, or making R_B very low.

- If R_E is of large value, high V_{CC} is necessary. This increases cost as well as precautions necessary while handling.

- If R_B is low, a separate low voltage supply should be used in the base circuit. Using two supplies of different voltages is impractical.

- In addition to the above, R_E causes ac feedback which reduces the voltage gain of the amplifier.

3) COLLECTOR TO BASE BIAS OR COLLECTOR FEED-BACK BIAS:



This configuration shown in fig 4.5 employs negative feedback to prevent thermal runaway and stabilize the operating point. In this form of biasing, the base resistor R_B is connected to the collector instead of connecting it to the DC source V_{cc} . So any thermal runaway will induce a voltage drop across the R_C resistor that will throttle the transistor's base current.

From Kirchhoff's voltage law, the voltage V_{R_b} across the base resistor R_b is

$$V_{R_b} = V_{cc} - \overbrace{(I_c + I_b)R_c}^{\text{Voltage drop across } R_c} - \overbrace{V_{be}}^{\text{Voltage at base}}.$$

By the Ebers-Moll model, $I_c = \beta I_b$, and so

$$V_{R_b} = V_{cc} - \overbrace{(\beta I_b + I_b)R_c}^{I_c} - V_{be} = V_{cc} - I_b(\beta + 1)R_c - V_{be}.$$

From Ohm's law, the base current $I_b = V_{R_b}/R_b$, and so

$$\overbrace{I_b R_b}^{V_{R_b}} = V_{cc} - I_b(\beta + 1)R_c - V_{be}.$$

Hence, the base current I_b is

$$I_b = \frac{V_{cc} - V_{be}}{R_b + (\beta + 1)R_c}$$

If V_{be} is held constant and temperature increases, then the collector current I_c increases. However, a larger I_c causes the voltage drop across resistor R_c to increase, which in turn reduces the voltage V_{R_b} across the base resistor R_b . A lower base-resistor voltage drop reduces the base current I_b , which results in less collector current I_c . Because an increase in collector current with temperature is opposed, the operating point is kept stable.

Merits:

- Circuit stabilizes the operating point against variations in temperature and β (i.e. replacement of transistor)

Demerits:

- In this circuit, to keep I_c independent of β , the following condition must be met:

$$I_c = \beta I_b = \frac{\beta(V_{cc} - V_{be})}{R_b + R_c + \beta R_c} \approx \frac{(V_{cc} - V_{be})}{R_c}$$

which is the case when

$$\beta R_c \gg R_b.$$

- As β -value is fixed (and generally unknown) for a given transistor, this relation can be satisfied either by keeping R_c fairly large or making R_b very low.
- If R_c is large, a high V_{cc} is necessary, which increases cost as well as precautions necessary while handling.
- If R_b is low, the reverse bias of the collector-base region is small, which limits the range of collector voltage swing that leaves the transistor in active mode.
- The resistor R_b causes an AC feedback, reducing the voltage gain of the amplifier. This undesirable effect is a trade-off for greater Q-point stability.

Usage: The feedback also decreases the input impedance of the amplifier as seen from the base, which can be advantageous. Due to the gain reduction from feedback, this biasing form is used only when the trade-off for stability is warranted.

4) COLLECTOR-EMITTER FEEDBACK BIAS:

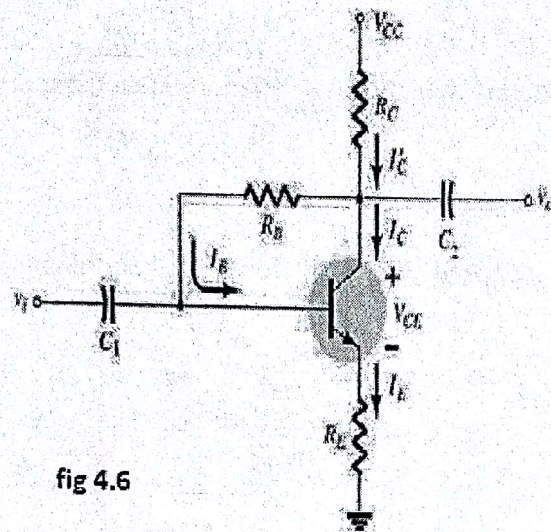
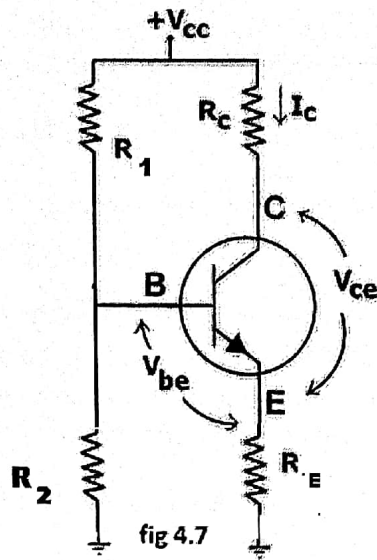


fig 4.6

The above fig4.6 shows the collector –emitter feedback bias circuit that can be obtained by applying both the collector feedback and emitter feedback. Here the collector feedback is provided by connecting a resistance R_B from the collector to the base and emitter feedback is provided by connecting an emitter R_E from emitter to ground. Both feed backs are used to control collector current and base current I_B in the opposite direction to increase the stability as compared to the previous biasing circuits.

5) VOLTAGE DIVIDER BIAS OR SELF BIAS OR EMITTER BIAS:

The voltage divider as shown in the fig 4.7 is formed using external resistors R_1 and R_2 . The voltage across R_2 forward biases the emitter junction. By proper selection of resistors R_1 and R_2 , the operating point of the transistor can be made independent of β . In this circuit, the voltage divider holds the base voltage fixed independent of base current provided the divider current is large compared to the base current. However, even with a fixed base voltage, collector current varies with temperature (for example) so an emitter resistor is added to stabilize the Q-point, similar to the above circuits with emitter resistor.



In this circuit the base voltage is given by:

$$V_B = \text{voltage across } R_2 = V_{cc} \frac{R_2}{(R_1 + R_2)} - I_B \frac{R_1 R_2}{(R_1 + R_2)}$$

$$\approx V_{cc} \frac{R_2}{(R_1 + R_2)} \text{ provided } I_B \ll I_2 = V_B / R_2.$$

$$\text{Also } V_B = V_{be} + I_E R_E$$

For the given circuit,

$$I_B = \frac{\frac{V_{CC}}{1 + R_1/R_2} - V_{be}}{(\beta + 1)R_E + R_1 \parallel R_2}.$$

Let the current in resistor R1 is I1 and this is divided into two parts – current through base and resistor R2. Since the base current is very small so for all practical purpose it is assumed that I1 also flows through R2, so we have

$$I_1 = \frac{V_{CC}}{R_1 + R_2}$$

$$V_2 = \frac{V_{CC}}{R_1 + R_2} \cdot R_2$$

Applying KVL in the circuit, we have

$$V_2 = V_{BE} + V_E$$

$$V_2 = V_{BE} + I_E R_E$$

$$I_E = \frac{V_2 - V_{BE}}{R_F}$$

$$I_C = \frac{V_2 - V_{BE}}{R_F} \quad \therefore I_C \cong I_E$$

$$I_C = \frac{\frac{V_{CC}}{R_1 + R_2} \cdot R_2 - V_{BE}}{R_E}$$

It is apparent from above expression that the collector current is independent of β thus the stability is excellent. In all practical cases the value of V_{BE} is quite small in comparison to the V_2 , so it can be ignored in the above expression so the collector current is almost independent of the transistor parameters thus this arrangement provides excellent stability.

Again applying KVL in collector circuit, we have

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$\therefore I_C \cong I_E$$

$$\therefore V_{CC} = I_C R_C + V_{CE} + I_C R_E$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

The resistor R_E provides stability to the circuit. If the current through the collector rises, the voltage across the resistor R_E also rises. This will cause V_{CE} to increase as the voltage V_2 is independent of collector current. This decreases the base current, thus collector current increases to its former value.

Stability factor for such circuit arrangement is given by

$$S = \frac{(1 + \beta)(R_{eq} + R_E)}{R_{eq} + R_E(1 + \beta)}$$

$$R_{eq} = R_1 || R_2$$

$$S = \frac{(1 + \beta) \left(1 + \frac{R_{eq}}{R_E}\right)}{\frac{R_{eq}}{R_E} + 1 + \beta}$$

If R_{eq}/R_E is very small compared to 1, it can be ignored in the above expression thus we have

$$S = \frac{1 + \beta}{1 + \beta} = 1$$

Which is excellent since it is the smallest possible value for the stability. In actual practice the value of stability factor is around 8-10, since R_{eq}/R_E cannot be ignored as compared to 1.

Merits:

- Unlike above circuits, only one dc supply is necessary.

- Operating point is almost independent of β variation.
- Operating point stabilized against shift in temperature.

Demerits:

- In this circuit, to keep I_C independent of β the following condition must be met:

$$I_C = \beta I_B = \beta \frac{\frac{V_{CC}}{1+R_1/R_2} - V_{be}}{(\beta + 1)R_E + R_1 \parallel R_2} \approx \frac{\frac{V_{CC}}{1+R_1/R_2} - V_{be}}{R_E},$$

which is approximately the case if $(\beta + 1)R_E \gg R_1 \parallel R_2$

where $R_1 \parallel R_2$ denotes the equivalent resistance of R_1 and R_2 connected in parallel.

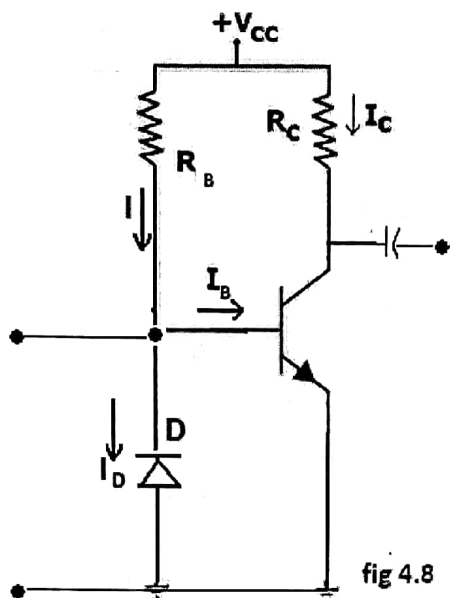
- As β -value is fixed for a given transistor, this relation can be satisfied either by keeping R_E fairly large, or making $R_1 \parallel R_2$ very low.
- If R_E is of large value, high V_{CC} is necessary. This increases cost as well as precautions necessary while handling.
- If $R_1 \parallel R_2$ is low, either R_1 is low, or R_2 is low, or both are low. A low R_1 raises V_B closer to V_C , reducing the available swing in collector voltage, and limiting how large R_C can be made without driving the transistor out of active mode. A low R_2 lowers V_{be} , reducing the allowed collector current. Lowering both resistor values draws more current from the power supply and lowers the input resistance of the amplifier as seen from the base.
- AC as well as DC feedback is caused by R_E , which reduces the AC voltage gain of the amplifier. A method to avoid AC feedback while retaining DC feedback is discussed below.

Usage: The circuit's stability and merits as above make it widely used for linear circuits.

5.6 BIAS COMPENSATION USING DIODE AND TRANSISTOR:

The various biasing circuits considered use some type of negative feedback to stabilize the operation point. Also, diodes, thermistors and sensistors can be used to compensate for variations in current.

DIODE COMPENSATION:



The following fig4.8 shows a transistor amplifier with a diode D connected across the base-emitter junction for compensation of change in collector saturation current I_{CO} . The diode is of the same material as the transistor and it is reverse biased by the emitter-base junction voltage V_{BE} , allowing the diode reverse saturation current I_O to flow through diode D. The base current $I_B = I - I_O$.

As long as temperature is constant, diode D operates as a resistor. As the temperature increases, I_{CO} of the transistor increases. Hence, to compensate for this, the base current I_B should be decreased.

The increase in temperature will also cause the leakage current I_O through D to increase and thereby decrease the base current I_B . This is the required action to keep I_C constant.

This type of bias compensation does not need a change in I_C to effect the change in I_C , as both I_O and I_{CO} can track almost equally according to the change in temperature.

THERMISTOR COMPENSATION:

The following fig4.9 a thermistor R_T , having a negative temperature coefficient is connected in parallel with R_2 . The resistance of thermistor decreases exponentially with increase of temperature. An increase of temperature will decrease the base voltage V_{BE} , reducing I_B and I_C .

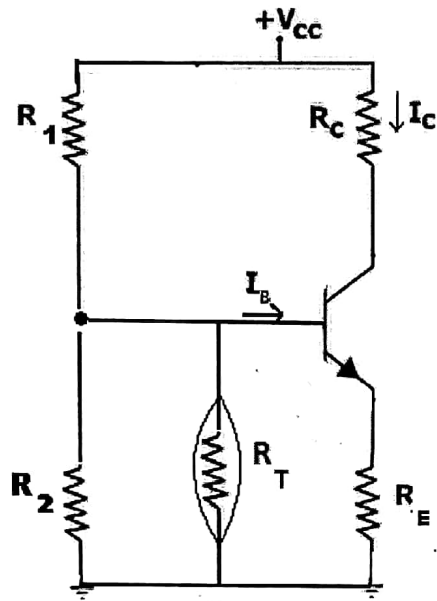


fig 4.9

SENSISTOR COMPENSATION:

In the following fig4.10 shown a sensistor R_s having a positive temperature coefficient is connected across R_1 or R_E . R_s increases with temperature. As the temperature increases, the equivalent resistance of the parallel combination of R_1 and R_s also increases and hence V_{BE} decreases, reducing I_B and I_C . This reduced I_C compensates for increased I_C caused by the increase in V_{BE} , I_{C0} and β due to temperature.

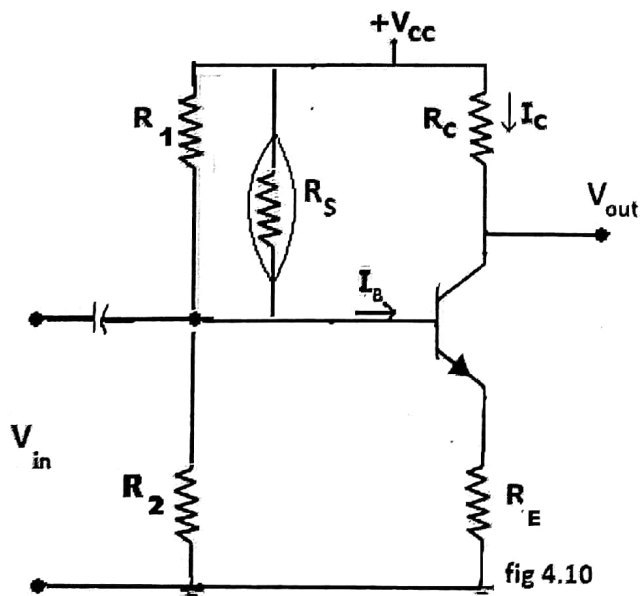


fig 4.10

5.7 THERMAL RUNAWAY AND THERMAL STABILITY:

THERMAL RUNAWAY:

The collector current for the CE circuit is given by $I_c = \beta I_B + (1 + \beta)I_{CO}$. The three variables in the equation, β , I_B , and I_{CO} increases with rise in temperature. In particular, the reverse saturation current or leakage current I_{CO} changes greatly with temperature. Specifically it doubles for every 10°C rise in temperature. The collector current I_c causes the collector base junction temperature to rise which in turn, increase I_{CO} , as a result I_c will increase still further, which will further rise the temperature at the collector base junction. This process will become cumulative leading at the collector base junction. This process will become cumulative leading to "thermal runaway". Consequently, the ratings of the transistor are exceeded which may destroy the transistor itself.

The collector is made larger in size than the emitter in order to help the heat developed at the collector junction. However if the circuit is designed such that the base current I_B is made to decrease automatically with rise in temperature, then the decrease in βI_B will compensate for increase in the $(1 + \beta)I_{CO}$, keeping I_c almost constant.

THERMAL RESISTANCE

Consider transistor used in a circuit where the ambient temperature of the air around the transistor is $T_A^\circ\text{C}$ and the temperature of the collector-base junction of the transistor is $T_J^\circ\text{C}$.

Due to heating within the transistor T_J is higher than T_A . As the temperature difference $T_J - T_A$ is greater, the power dissipated in the transistor, P_D will be greater, i.e, $T_J - T_A \propto P_D$

The equation can be written as $T_J - T_A = \theta P_D$, where θ is the constant of proportionality and is called the Thermal resistance. Rearranging the above equation $\theta = (T_J - T_A) / P_D$. Hence θ is measured in $^\circ\text{C}/\text{W}$ which may be as small as $0.2^\circ\text{C}/\text{W}$ for a high power transistor that has an efficient heat sink or up to $1000^\circ\text{C}/\text{W}$ for small signal, low power transistor which have no cooling provision.

As θ represents total thermal resistance from a transistor junction to the ambient temperature, it is referred to as θ_{J-A} . However, for power transistors, thermal resistance is given from junction to case, θ_{J-C} .

The amount resistance from junction to ambience is considered to consist of 2 parts.

$$\theta_{J-A} = \theta_{J-C} + \theta_{C-A}$$

Which indicates the heat dissipated in the junction must make its way to the surrounding air through two series paths from junction to case and from case to air. Hence the power dissipated.

$$P_D = (T_J - T_A) / \Theta_{J-A}$$

$$= (T_J - T_A) / (\Theta_{J-C} + \Theta_{C-A})$$

Θ_{J-C} is determined by the type of manufacture of the transistor and how it is located in the case, but Θ_{C-A} is determined by the surface area of the case or flange and its contact with air. If the effective surface area of the transistor case could be increased, the resistance to heat flows, or could be increased Θ_{C-A} , could be decreased. This can be achieved by the use of a heat sink.

The heat sink is a relatively large, finned, usually black metallic heat conducting device in close contact with transistor case or flange. Many versions of heat sink exist depending upon the shape and size of the transistor. Larger the heat sink smaller is the thermal resistance Θ_{HS-A} .

This thermal resistance is not added to Θ_{C-A} in series, but is instead in parallel with it and if

Θ_{HS-A} is much less than Θ_{C-A} , then Θ_{C-A} will be reduced significantly, thereby improving the dissipation capability of the transistor. Thus

$$\Theta_{J-A} = \Theta_{J-C} + \Theta_{C-A} \parallel \Theta_{HS-A}$$

5.8 CONDITION FOR THERMAL STABILITY:

For preventing thermal runaway, the required condition is the rate at which the heat is released at the collector junction should not exceed the rate at which the heat can be dissipated under steady state condition. Hence the condition to be satisfied to avoid thermal runaway is given by

$$\frac{\partial P_C}{\partial T_J} < \frac{1}{\theta}$$

If the circuit is properly designed, then the transistor cannot runaway below a specified ambient temperature or even under any conditions.

In the self biased circuit the transistor is biased in the active region. The power generated at the junction without any signal is

$$P_C = I_C V_{CE} \approx I_C V_{CE}$$

Let us assume that the quiescent collector and the emitter currents are equal. Then

$$P_c = I_c V_{CC} - I_c^2 (R_E + R_C) \dots \dots \dots (1)$$

The condition to prevent thermal runaway can be written as

$$\frac{\partial P_c}{\partial I_c} \frac{\partial I_c}{\partial T_j} < \frac{1}{\theta} \dots \dots \dots (2)$$

As θ and $\frac{\partial I_c}{\partial T_j}$ are positive, $\frac{\partial P_c}{\partial I_c}$ should be negative in order to satisfy the above condition.

Differentiating equation (1) w.r.t I_c we get

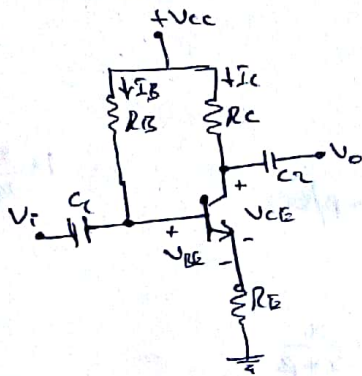
$$\frac{\partial P_c}{\partial I_c} = V_{CC} - 2I_c (R_E + R_C) \dots \dots \dots (3)$$

Hence to avoid thermal runaway it is necessary that

$$I_c > \frac{V_{CC}}{2(R_E + R_C)} \dots \dots \dots (4)$$

Since $V_{CE} = V_{CC} - I_c(R_E + R_C)$ then eq(4) implies that $V_{CE} < V_{CC}/2$. If the inequality of eq(4) is not satisfied and $V_{CE} < V_{CC}/2$, then from eq(3), $\frac{\partial P_c}{\partial I_c}$ is positive., and the corresponding eq(2) should be satisfied. Other wise thermal runaway will occur.

To improve the stability of the biasing circuit over the fixed bias circuit, the emitter resistance is connected in the biasing circuit. Such biasing circuit is known as emitter bias circuit and it is shown in the fig below



DC Analysis

Applying KVL to the base circuit we get,

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0 \rightarrow (1)$$

we have,

$$I_E = (\beta + 1) I_B$$

$$\therefore V_{CC} - I_B R_B - V_{BE} - (\beta + 1) I_B R_E$$

$$\therefore V_{CC} - V_{BE} = I_B R_B + (\beta + 1) I_B R_E$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_E} \quad \because \beta \gg 1$$

$$V_B = V_{BE} + V_E$$

(2)

$$V_B = V_{CC} - I_B R_B$$

$$\therefore V_E = I_E R_E$$

$$V_B = V_{BE} + I_E R_E$$

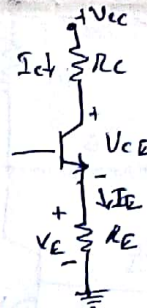
Now Applying KVL to the collector circuit we get,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$V_E = I_E R_E$$

$$V_{CE} = V_{CC} - V_E$$

$$V_C = V_{CC} - I_C R_C$$



Stability Factor:

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E$$

$$= I_B R_B + V_{BE} + (I_B + I_C) R_E$$

Differentiating w.r.t I_C and considering V_{BE} to be independent of I_C we get,

$$0 = \frac{dI_B}{dI_C} \times R_B + \frac{dI_B}{dI_C} \times R_E + R_E$$

$$\frac{dI_B}{dI_C} R_B + \frac{dI_B}{dI_C} R_E = -R_E$$

$$\frac{dI_B}{dI_C} (R_B + R_E) = -R_E$$

$$\frac{dI_B}{dI_C} = \frac{-R_E}{R_B + R_E}$$

$$S = \frac{1 + \beta}{1 - \beta \left(\frac{dI_B}{dI_C} \right)}$$

$$= \frac{1 + \beta}{1 - \beta \left(\frac{R_E}{R_F + R_B} \right)}$$

$$= (1 + \beta) \frac{1}{1 + \beta \frac{R_E / R_E}{R_F / R_E + R_B / R_E}}$$

$$= (1 + \beta) \frac{1}{1 + \beta \frac{1}{1 + \frac{R_B}{R_E}}} = (1 + \beta) \cdot \frac{1}{1 + \beta / x}$$

$$x = 1 + \frac{R_B}{R_E}$$

$$= (1 + \beta) \frac{1}{\frac{x + \beta}{x}} = (1 + \beta) = \frac{x}{x + \beta}$$

$$S = (1 + \beta) \frac{1 + (R_B / R_E)}{(1 + \beta) + (R_B / R_E)}$$

COLLECTOR-EMITTER FEEDBACK BIAS

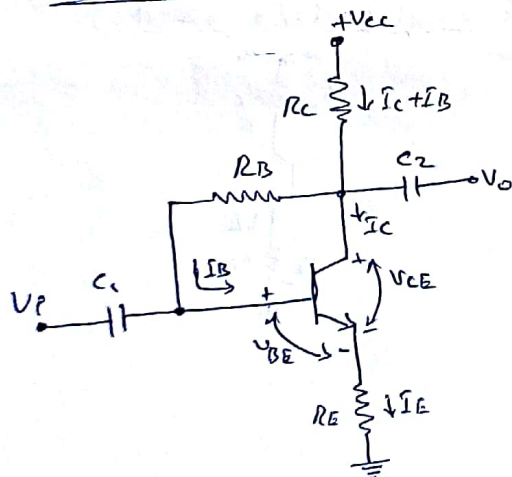


Fig: collector - emitter feedback bias circuit.

To further improve the level of stability, the emitter resistance is connected in the collector bias circuit to provide both collector and emitter feedback, as shown in the fig.)

Applying KVL to the base circuit shown in the fig we have,

$$V_{CC} = (I_C + I_B)R_C + I_B R_B + V_{BE} + I_E R_E$$

$$= I_C R_C + I_B R_C + I_B R_B + V_{BE} + I_E R_E$$

$$= I_B (R_C + R_B) + I_C R_C + V_{BE} + I_E R_E$$

$$\therefore I_B = \frac{V_{CC} - V_{BE}}{R_C + R_B + \beta R_C + V_{BE} + (1 + \beta) I_B R_E}$$

$$= \frac{V_{CC} - V_{BE}}{(1 + \beta) I_B R_C + I_B R_B + V_{BE} + (1 + \beta) I_B R_E}$$

$$\therefore V_{CC} - V_{BE} = (1 + \beta) I_B R_C + I_B R_B + (1 + \beta) I_B R_E$$

$$V_{CC} - V_{BE} = I_B [R_B + (1+\beta)R_E]$$

$$= I_B [(1+\beta)(R_C + R_E) + R_B]$$

$$= I_B (\beta(R_C + R_E) + R_B) \quad \because \beta \gg 1$$

$$\therefore I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$

Applying KVL to collector circuit we have

$$V_{CC} = V_{CE} + V_E + (I_C + I_B)R_C$$

$$= V_{CE} + I_E R_E + I_E R_C$$

$$= V_{CE} + I_E (R_C + R_E)$$

$$\because V_E = I_E R_E, I_E = I_C + I_B$$

$$\therefore V_{CE} = V_{CC} - I_E (R_C + R_E)$$

STABILITY FACTOR FOR COLLECTOR-EMITTER FEEDBACK BIAS

From Base circuit

$$V_{CC} = (I_C + I_B)R_C + I_B R_B + V_{BE} + (I_C + I_B)R_E$$

Differentiating w.r.t I_C & considering V_{BE} constant we get,

$$0 = R_C + \frac{dI_B}{dI_C} R_C + \frac{dI_B}{dI_C} R_B + 0 + R_E + \frac{dI_B}{dI_C} R_E$$

$$\therefore \frac{dI_B}{dI_C} [R_C + R_B + R_E] + R_C + R_E = 0$$

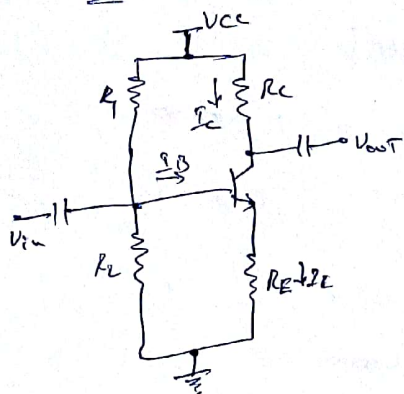
$$\frac{dI_B}{dI_C} (R_C + R_B + R_E) = - (R_C + R_E)$$

$$\frac{dI_B}{dI_C} = \frac{- (R_C + R_E)}{(R_C + R_B + R_E)}$$

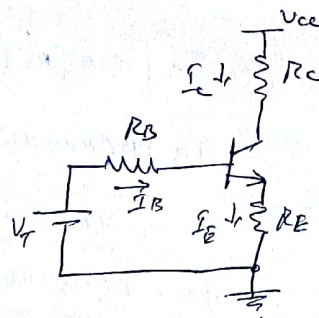
$$\text{w.r.t. } S = \frac{(1+\beta)}{1 - \beta \left(\frac{dI_B}{dI_C} \right)} = \frac{(1+\beta)}{1 + \beta \left(\frac{R_C + R_E}{R_C + R_B + R_E} \right)}$$

$$S = \frac{(1+\beta)}{1 + \beta \left(\frac{R_C + R_E}{R_C + R_B + R_E} \right)}$$

The factor $(R_C + R_E) / (R_C + R_B + R_E)$ in denominator of above eq. is always greater than the factor $R_C / (R_C + R_B)$ & $R_E / (R_E + R_B)$ in the denominator of fixed bias & with emitter resistor & collector to base bias with emitter resistor respectively. This states that the stability of the collector-emitter feedback bias circuit is always better than that of collector feedback & emitter feedback circuits.



$\equiv$



$$V_T = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2}$$

Loop eqn from the equivalent Base circuit

$$V_T = I_B R_B + V_{BE} + I_E R_E \rightarrow (1)$$

$$= I_B R_B + V_{BE} + (I_B + I_C) R_E$$

$$= I_B R_B + V_{BE} + I_B R_E + I_C R_E$$

$$= V_{BE} + I_C R_E + I_B (R_B + R_E)$$

$$\therefore I_B = \frac{V_T - V_{BE} - I_C R_E}{(R_B + R_E)} \rightarrow (2)$$

from the collector circuit

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E \rightarrow (3)$$

Stability Factor

from eqn (2)

$$I_B = \frac{V_T}{R_B + R_E} - \frac{V_{BE}}{R_B + R_E} - \frac{I_C R_E}{R_B + R_E}$$

Differentiating above eqn w.r.t I_C

$$\frac{dI_B}{dI_C} = 0 - 0 - \frac{R_E}{R_B + R_E}$$

w.k.T.

$$S = \frac{(1 + \beta)}{1 - \beta \left(\frac{dI_B}{dI_C} \right)}$$

$$S = \frac{1 + \beta}{1 + \beta \left(\frac{R_E}{R_B + R_E} \right)}$$

by dividing each term by R_E we get

$$S = (1 + \beta) \frac{1 + (R_B/R_E)}{(1 + \beta) + (R_B/R_E)}$$

$$S = \frac{1 + \left(\frac{R_B}{R_E}\right)}{(1+\beta) + \left(\frac{R_B}{R_E}\right)}$$

→ The ratio (R_B/R_E) controls value of stability factor S .

If $R_B/R_E \ll 1$ then $S = \frac{1}{(1+\beta)} = 1$

Practically $R_B/R_E \neq 0$. But to have better stability factor's we have to keep ratio R_B/R_E as small as possible.

→ To keep R_B/R_E small, it is necessary to keep R_B small. This means that R_1/R_2 must be small. Due to small value of R_1 & R_2 , potential divider circuit will draw more current from V_{CC} reducing the life of the battery. So while designing if we make R_2 much smaller than R_1 , then parallel combination results small R_B without drawing more current through V_{CC} . Another important aspect is that reducing R_B will reduce i/p impedance of the circuit, since R_B comes in parallel with the i/p. This reduction of i/p impedance in amplifier circuits is not desirable & hence R_B cannot be made very small.

→ Emitter Resistance R_E is the another parameter we can use to decrease ratio R_B/R_E . By increasing R_E we can make R_B/R_E small. But as we increase R_E , drop $I_E R_E$ will also increase & since V_{CC} is constant, drop across R_C will reduce. This shifts the operating point Q which is not desirable & hence there is limit of increasing R_E .

Thus while designing voltage divider bias circuit we have to find compromising values:

S - small

R_B - Reasonably small

R_E - Not very large

→ If ratio R_B/R_E is fixed, S increase with β . Therefore stability decreases with increasing β .

→ Stability factor S is essentially in depend of β for small values of S

To determine the stability factor S'
The stability factor S' is defined as the rate of change of I_C with V_{BE} , keeping I_{CO} & β constant.

$$S' = \frac{dI_C}{dV_{BE}} = \frac{\Delta I_C}{\Delta V_{BE}} \rightarrow (1)$$

$$V_T = I_B R_B + V_{BE} + I_E R_E \rightarrow (2)$$

$$= I_B R_B + V_{BE} + (I_C + I_B) R_E$$

$$= I_B R_B + V_{BE} + I_C R_E + I_B R_E$$

$$V_T = I_B (R_B + R_E) + V_{BE} + I_C R_E \rightarrow (3)$$

with (1)

$$I_C = \beta I_B + (1 + \beta) I_{CO} \rightarrow (4)$$

$$I_B = \frac{I_C - (1 + \beta) I_{CO}}{\beta} \rightarrow (5)$$

Substituting eq (5) in eq (3) we get

$$V_T = \left[\frac{I_C - (1 + \beta) I_{CO}}{\beta} \right] (R_B + R_E) + V_{BE} + I_C R_E$$

$$V_T = \frac{I_C}{\beta} (R_B + R_E) - \frac{(1 + \beta) I_{CO}}{\beta} (R_B + R_E) + V_{BE} + R_E I_C$$

Differentiating the above eq with V_{BE} we get

$$0 = \frac{dI_C}{dV_{BE}} \left(\frac{R_B + R_E}{\beta} \right) - 0 + 1 + \frac{dI_C}{dV_{BE}} \cdot R_E$$

$$= \frac{dI_C}{dV_{BE}} \left[\frac{R_B + R_E}{\beta} + R_E \right] + 1$$

$$-1 = \frac{dI_C}{dV_{BE}} \left[\frac{R_B + R_E}{\beta} + R_E \right]$$

$$= \frac{dI_C}{dV_{BE}} \left[\frac{R_B + R_E + \beta R_E}{\beta} \right]$$

$$\therefore \frac{dI_C}{dV_{BE}} = - \frac{\beta}{R_B + R_E + \beta R_E}$$

$$S' = \frac{-\beta}{R_B + R_E (1 + \beta)}$$

The Stability Factor S is defined as the rate of change of

I_c w.r.t to β , keeping I_{co} & V_{BE} constant. $S' = \frac{dI_c}{d\beta} \Big|_{I_{co} \& V_{BE}}$

$$V_T = I_B R_B + V_{BE} + I_E R_E \rightarrow (1)$$

$$= I_B R_B + V_{BE} + (I_B + I_C) R_E$$

$$= I_B R_B + V_{BE} + I_B R_E + I_C R_E$$

$$V_T = I_B (R_B + R_E) + I_C R_E + V_{BE} \rightarrow (2)$$

w.k.T

$$I_C = \beta I_B + (1 + \beta) I_{co}$$

$$I_B = \frac{I_C - (1 + \beta) I_{co}}{\beta} \rightarrow (3)$$

substituting eq (3) in eq (2) we get.

$$V_T = \frac{I_C}{\beta} (R_B + R_E) + V_{BE} + I_C R_E - \frac{I_{co}}{\beta} (1 + \beta) [R_B + R_E] \rightarrow (4)$$

$$V_T = \frac{I_C R_B}{\beta} + \frac{I_C R_E}{\beta} + V_{BE} + I_C R_E - \frac{I_{co}}{\beta} (1 + \beta) R_B - \frac{I_{co}}{\beta} (1 + \beta) R_E$$

$$V_T = I_C \left[\frac{R_B}{\beta} + \frac{R_E}{\beta} + R_E \right] - I_{co} \left[\frac{(1 + \beta)(R_E + R_B)}{\beta} \right] + V_{BE}$$

$$V_T = I_C \left[\frac{R_B + R_E + \beta R_E}{\beta} \right] - I_{co} \left[\frac{(1 + \beta)(R_E + R_B)}{\beta} \right] + V_{BE}$$

$$V_T = I_C \left[\frac{R_B + R_E + \beta R_E}{\beta} \right] - V' + V_{BE} \quad \text{where } V' = I_{co} \left[\frac{(1 + \beta)(R_E + R_B)}{\beta} \right]$$

$$\therefore I_C = \frac{(V_T + V' - V_{BE}) \beta}{R_B + (1 + \beta) R_E} \rightarrow (5)$$

Differentiating above eq w.r.t β & taking V' independent of β , we get

$$\frac{dI_C}{d\beta} = \frac{[R_B + R_E (1 + \beta)] (V_T + V' - V_{BE}) - \beta (V_T + V' - V_{BE}) R_E}{[R_B + (1 + \beta) R_E]^2}$$

$$\text{Hint: } \frac{d}{dt} \left(\frac{u}{v} \right) = \frac{v \frac{du}{dt} - u \frac{dv}{dt}}{v^2}$$

$$= \frac{(R_B + R_E + \beta R_E) (V_T + V' - V_{BE}) - \beta (V_T + V' - V_{BE}) R_E}{(R_B + (1 + \beta) R_E) (R_B + (1 + \beta) R_E)}$$

$$\text{let } V_T + V' - V_{BE} = X$$

$$= \frac{(R_B + R_E + \beta R_E) \cancel{R_E} - \beta R_E \cancel{R_E}}{(R_B + R_E(1+\beta)) [R_B + R_E(1+\beta)]}$$

$$= \frac{R_B \cancel{R_E} + R_E \cancel{R_E} + \beta \cancel{R_E} \cancel{R_E} - \beta R_E \cancel{R_E}}{(R_B + R_E(1+\beta)) [R_B + R_E(1+\beta)]}$$

$$\frac{dI_C}{d\beta} = \frac{(R_B + R_E) (V_T + V' - V_{BE})}{[R_B + R_E(1+\beta)] [R_B + R_E(1+\beta)]}$$

Multiplying numerator & denominator by $(1+\beta)$ we get

$$\frac{dI_C}{d\beta} = \frac{(1+\beta) (R_B + R_E) (V_T + V' - V_{BE})}{[R_B + R_E(1+\beta)] [R_B + R_E(1+\beta)] (1+\beta)}$$

$$\frac{dI_C}{d\beta} = \frac{S (V_T + V' - V_{BE})}{(1+\beta) [R_B + R_E(1+\beta)]} \rightarrow (6)$$

Multiplying numerator & denominator by β we get

$$\frac{dI_C}{d\beta} = \frac{S \beta (V_T + V' - V_{BE})}{(\cancel{1+\beta}) \beta (R_B + R_E(1+\beta))}$$

from eq (5) $I_C = \frac{\beta (V_T + V' - V_{BE})}{R_B + R_E(1+\beta)}$

$$\therefore \frac{dI_C}{d\beta} = \frac{S I_C}{(1+\beta) \beta}$$

$$S'' = \frac{S I_C}{\beta (1+\beta)}$$

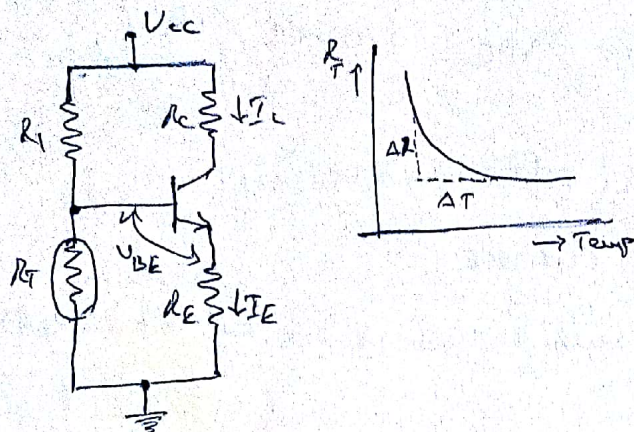
$$\therefore S = (1+\beta) \frac{\left(1 + \frac{R_B}{R_E}\right)}{\left(1+\beta + \frac{R_B}{R_E}\right)}$$

$$S = (1+\beta) \frac{\left(1 + \frac{R_B}{R_E}\right) R_E}{\left(1+\beta + \frac{R_B}{R_E}\right) R_E}$$

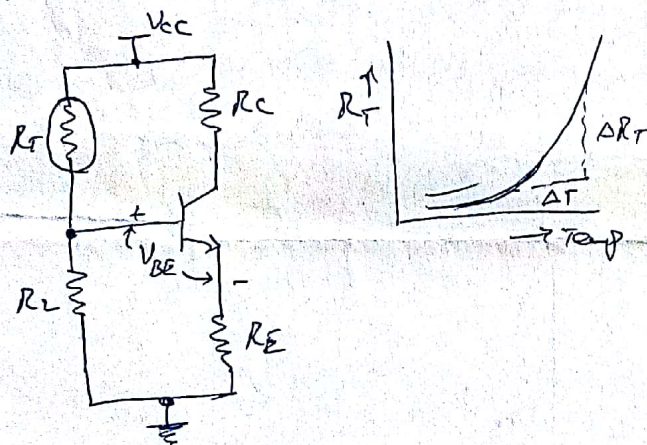
$$= (1+\beta) \frac{(R_E + R_B)}{R_E + R_E \beta + R_B}$$

$$S = (1+\beta) \frac{R_E + R_B}{R_B + R_E(1+\beta)}$$

1. Thermistor Compensation



2. Sensistor Compensation



3. Diode Compensation Techniques

① Diode in emitter circuit

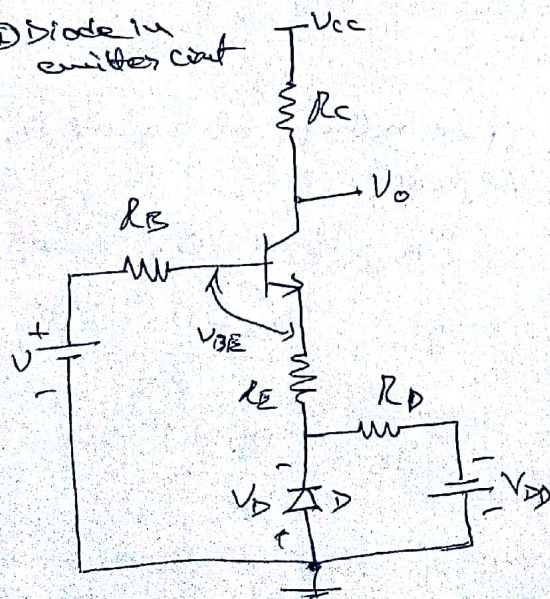


fig: Stabilization by means of voltage divider bias & diode

$$V_{BE} = V_T - \left[\frac{R_B + (1+\beta)R_E}{\beta} \right] I_C + \left[\frac{(R_E + R_B)(1+\beta)}{\beta} \right] I_{CO}$$

$$\therefore \left[\frac{R_B + (1+\beta)R_E}{\beta} \right] I_C = V_T - V_{BE} + \left[\frac{(R_E + R_B)(1+\beta)}{\beta} \right] I_{CO}$$

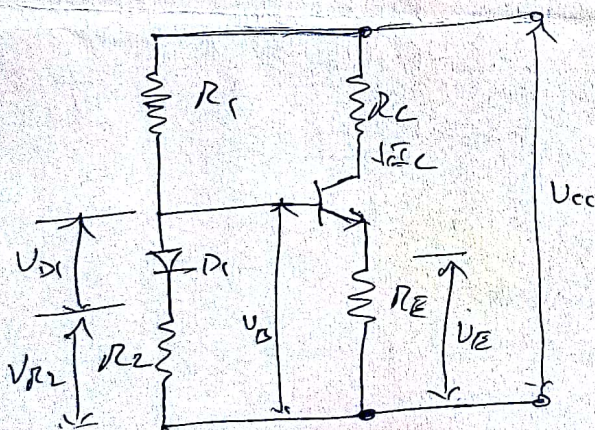
$$I_C = \frac{\beta[V_T - V_{BE}] + (R_E + R_B)(1+\beta)I_{CO}}{R_B + (1+\beta)R_E} \rightarrow (1)$$

If we write KVL to the base circuit of the BJT then eq (1) becomes

$$I_C = \frac{\beta[V - (V_{BE} - V_D)] + (R_E + R_B)(1+\beta)I_{CO}}{R_B + (1+\beta)R_E} \rightarrow (2)$$

Since V_D tracks V_{BE} w.r.t temp it is clear from eq (2) that I_C will be insensitive to variations in V_{BE} .

⑤ Diode in voltage divider circuit



$$I_E = \frac{V_B - V_{BE}}{R_E}$$

$$\text{also } I_E = \frac{V_E}{R_E}$$

$$I_{C \approx I_E}$$

$$I_C = \frac{V_B - V_{BE}}{R_E} \rightarrow (1)$$

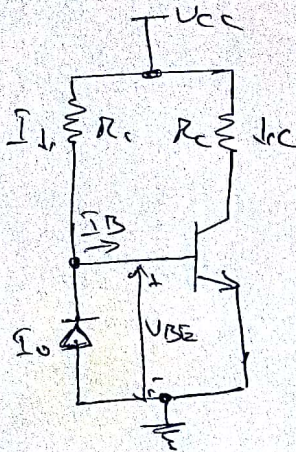
when V_{BE} changes with temp I_C also changes. To cancel the change in I_C , one diode is used in this circuit for compensation at shutdown.

The voltage of the base V_B is now,

$$V_B = V_{R2} + V_D$$

$$\therefore I_C = \frac{V_{R2} + V_D - V_{BE}}{R_E}$$

$$I_C \approx \frac{V_{R2}}{R_E}$$



$$I = \frac{V_{CC} - V_{BE}}{R_1}$$

$$I = I_B + I_O \quad \therefore I_B = I - I_O$$

For germanium transistor $V_{BE} = 0.2V$ which is very small & neglecting change in V_{BE} with temp we can write

$$I \approx \frac{V_{CC}}{R_1} \approx \text{const}$$

we know

$$I_C = \beta I_B + (1 + \beta) I_{CO}$$

Substitute value of I_B in above eq we get

$$I_C = \beta I - \beta I_O + (1 + \beta) I_{CO}$$

if $\beta \gg 1$ we get

$$I_C = \beta I - \beta I_O + \beta I_{CO}$$

now if $I_O = I_{CO}$ we get

$$I_C = \beta I$$

As I is const I_C remains fairly const. In other words we can say that changes by I_{CO} with temp are compensated by diode and thus collector current remains fairly const.

FET Biasing

Unlike BJTs Thermal runaway does not occur with FETs. However, the wide differences in maximum and minimum transfer characteristics make I_D levels unpredictable with simple fixed-gate bias voltage. To obtain reasonable limits on quiescent drain currents I_D & drain-source voltage V_{DS} , source resistor & potential divider bias techniques must be used. With few exceptions, MOSFET bias circuits are similar to those used for ~~BJT~~ BJTs. Various FET biasing circuits are

1. Fixed Bias
2. Self Bias
3. Potential Divider Bias
4. Current-Source Bias.

DC Load line and Bias point

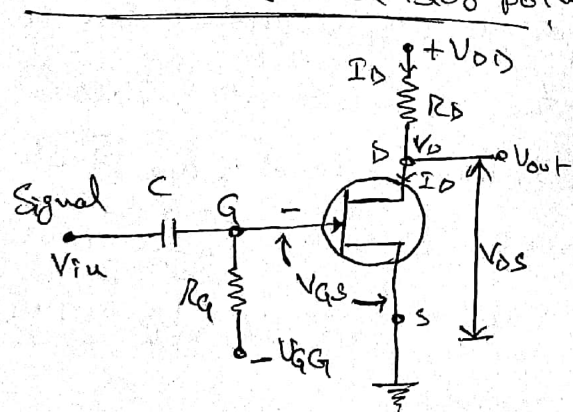


Fig (a) ~~Fixed~~ Fixed Bias Circuit for JFET

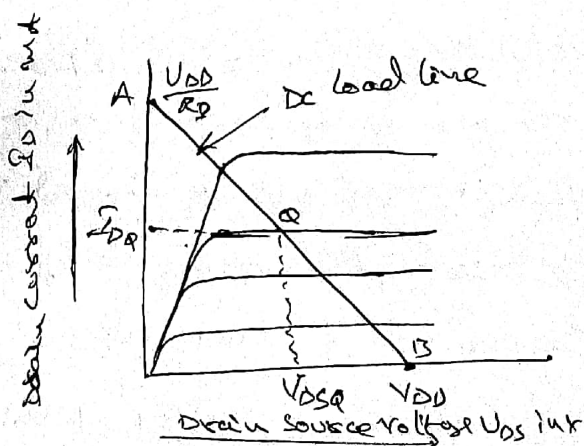


Fig (b) Characteristics of FET

The DC load line for a FET circuit is drawn upon the output characteristics of the device in exactly the same way as for a BJT circuit.

Consider the FET circuit & characteristics shown in fig (a) & (b) respectively. The drain source voltage is given as

$$V_{DS} = V_{DD} - I_D R_D \rightarrow (1)$$

where V_{DD} is the supply voltage
 $I_D R_D$ is the voltage drop across R_D .

(i) when $I_D = 0$, $V_{DS} = V_{DD}$ --- cutoff point B

(ii) when $V_{GS} = 0$; $I_D = \frac{V_{DD}}{R_D}$ --- saturation point A.

By joining these two points A & B, dc load line is obtained.

A dc bias point or quiescent point (Q-point) is selected on the FET dc load line. This point defines the dc conditions that exists in a circuit when no i/p signal is applied. The bias point is selected to give maximum possible variation in o/p (drain source) voltage when the drain current is varied by an i/p signal. In this case the +ve going & -ve going o/p voltage swings should be as closely equal as possible, where maximum o/p voltage swing is not required, the bias point may be at any convenient position on the load line. For the load line in fig ⑤ the bias conditions are $\frac{V_{DD}}{2}$ & $\frac{V_{DD}}{2R_D}$. For a FET amplifier, V_{GS} must remain in the pinch-off region of the characteristics. This means that it must not be allowed to go below the level of the pinch-off voltage V_p . Thus in the design of a FET bias circuit, the drain source voltage should always be a minimum of $(V_p + 1)$ volt.

$$\text{i.e. } V_{DS}(\text{min}) = V_p + 1 \text{ volts} \rightarrow \textcircled{2}$$

when an external bias voltage V_{GS} is included, the pinch-off voltage for that bias level on the drain characteristics is $V_p - V_{GS}$, where V_p is the pinch-off voltage at $V_{GS} = 0$. Consequently, the minimum drain-source voltage may be reduced to

$$V_{DS}(\text{min}) = V_p - V_{GS} + 1 \text{ volts} \rightarrow \textcircled{3}$$

For the operation of FET as a switch, the device will either be biased off or on into the channel ohmic region of the drain characteristics.

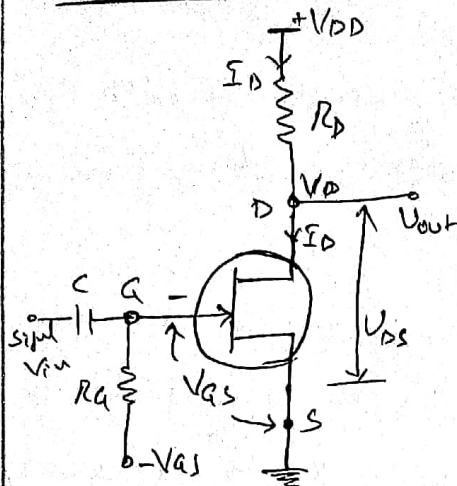


Fig. 1 Fixed bias circuit

Setting of gate source V_{GS} to give desired drain current ~~is limited~~ I_D . For a JFET drain is limited by the drain-source saturation current I_{DSS} . Since the FET has such a high i/p impedance that no gate current flows & the DC voltage of the gate set by a voltage divider or a fixed battery voltage is not affected or loaded by the FET. fixed DC bias is obtained using a battery V_{GG} . This battery ensures that the gate is always -ve w.r.t source & no current flows through resistor R_G & gate terminal i.e. $I_G \approx 0$. The battery provides a voltage V_{GS} to bias the n-channel JFET, but no steady current is drawn from the battery V_{GG} . Resistor R_G is included to allow any AC signal applied through capacitor 'C' to develop across R_G , while any AC signal will develop across R_D , the DC voltage drop across R_G is equal to $I_G R_G$ i.e. 0 volt.

The gate-source voltage V_{GS} is then

$$V_{GS} = -V_G - V_S = -V_{GG} - 0 = -V_{GG} \rightarrow (4)$$

The drain-source current I_D is then fixed by the gate source voltage as determined by eq. 1

$$\begin{aligned} I_D &= I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2 \\ &= I_{DSS} \left[1 - \frac{V_{GS}}{V_{GS(Off)}} \right]^2 \rightarrow (4.1) \end{aligned}$$

This current then causes a voltage drop across the drain resistor R_D & is given as

$$V_{RD} = I_D R_D$$

$$\text{d.c. voltage } V_{out} = V_{DD} - I_D R_D \rightarrow (5)$$

Since V_{GS} is fixed value of dc supply of the magnitude of gate-to-source voltage V_{GS} is also fixed, hence this circuit is named as fixed bias circuit. Since this bias circuit uses two batteries V_{DD} & V_{GG} , it is known as "two battery bias circuit".

A FET has a high i/p impedance. To make advantage of it, R_G should be as large as possible so that the i/p impedance of the circuit remains high. If R_G is extremely large a charge accumulated on the gate may take a long time to leak off. A reasonable upper limit is $1\text{ M}\Omega$. Normally R_G should not exceed this value.

Self-Bias

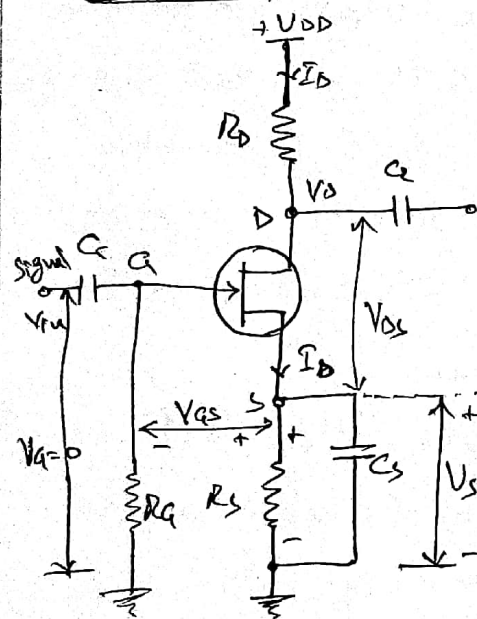


Fig (a): Self Bias circuit for n-channel FET

This is the most common method

for biasing a JFET. Self Bias for an n-channel JFET is shown in Fig (a). This circuit eliminates the requirement of two dc supplies i.e. only drain supply is ~~connected~~ used & no gate supply is connected. In this circuit, a resistor R_S , known as bias resistor, is connected in the source leg. The dc component of drain current I_D flows through R_S makes a voltage drop across resistor R_S . The voltage

drop across R_S reduces the gate-to-source reverse voltage required for FET operation. The capacitor C_S bypasses the ac component of the drain current I_D . The addition of Resistor R_G in the circuit does not disturb the dc bias, This is because gate current flowing

Through it is zero & the gate leakage current is almost zero. Thus, gate is essentially at dc ground. The resistor R_G is inserted in the circuit to avoid the short circuit of the ac input voltage. Further, if there is a leakage, the resistor R_G will provide to it an escape route other. w/v, the leakage current would build up static charge (voltage) at the gate which could change the bias. The resistor R_S , the feedback resistor, also helps in preventing any variation in JFET drain current.

Since no gate current flows through the reverse bias the gate current $I_G = 0$ and therefore

$$V_G = I_G R_G = 0V.$$

with a drain current I_D the voltage at the S is

$$V_S = I_D R_S \rightarrow (6)$$

The gate-to-source voltage is then

$$V_{GS} = V_G - V_S = 0 - I_D R_S = -I_D R_S \rightarrow (7)$$

So voltage drop across resistance R_S provides the biasing voltage V_{GS} & no external source is required for biasing & this is the reason that it is called "self bias".

The operating point (i.e. zero signal I_D & V_{GS}) can easily be determined from (4.2) &

$$V_{DS} = V_{DD} - I_D (R_D + R_S) \rightarrow (8)$$

Thus DC conditions of JFET amplifier are fully specified. Self biasing of a JFET stabilises its quiescent operating point against any change in its parameters like transconductance. Let the given JFET be replaced by another JFET having the double conductance then drain current will also try to be double but since any increase in voltage drop across R_S , therefore, gate-source voltage, V_{GS} becomes more -ve & thus increase in drain current is reduced.

A Slightly modified form of DC bias is provided by the circuit shown in fig (c). The resistors R_{G1} & R_{G2} form a potential divider across drain supply V_{DD} . The voltage V_2 across R_{G2} provides the necessary bias. The additional gate resistor R_{G1} from gate to supply voltage facilitates in larger adjustment of the DC bias point & permits use of larger value R_S .

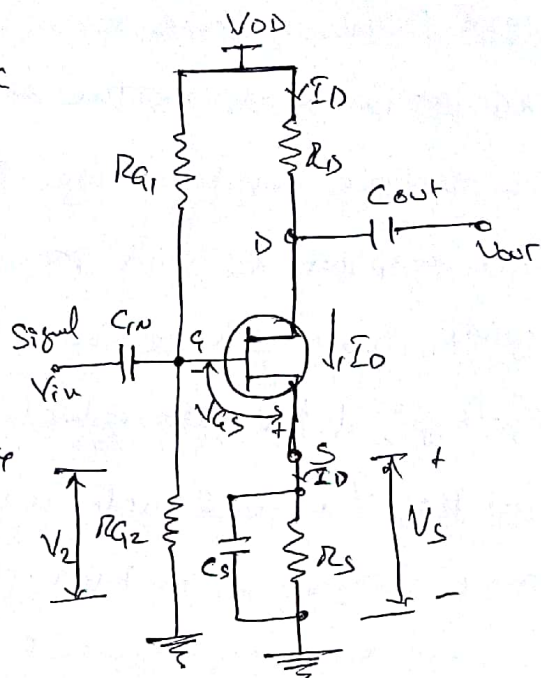


Fig (c): Potential Divider Bias circuit for n-channel JFET

The gate is reverse biased so that $I_G = 0$ at gate voltage

$$V_G = V_2 = \frac{V_{DD}}{R_{G1} + R_{G2}} \times R_{G2} \rightarrow (9)$$

$$\text{and } V_{GS} = V_G - V_S = V_G - I_D R_S \rightarrow (10)$$

The circuit is so designed that $I_D R_S$ is larger than V_G (or V_2) so that V_{GS} is -ve. This provides correct bias voltage.

The operating point can be determined as

$$I_D = \frac{V_G - V_{GS}}{R_S}$$

$$\text{and } V_{DS} = V_{DD} - I_D (R_D + R_S) \rightarrow (11)$$

Maximum gain is achieved by making resistance R_D as large as possible & for a given level of I_D it needs maximum voltage drop across resistor R_D . However, greatest bias stability is achieved by making R_S as large as possible.

As the gate voltage V_G is very large as compared to gate-to-source voltage V_{GS} , the drain current is approximately constant. In practice, the voltage divider bias is less effective with JFET than BJT.

It is because in BJT, $V_{BE} \approx 0.7V$ (Silicon) with only minor variations from one transistor to another transistor, But in a JFET, the V_{GS} can vary several volts from one JFET to another.

Current-Source Bias

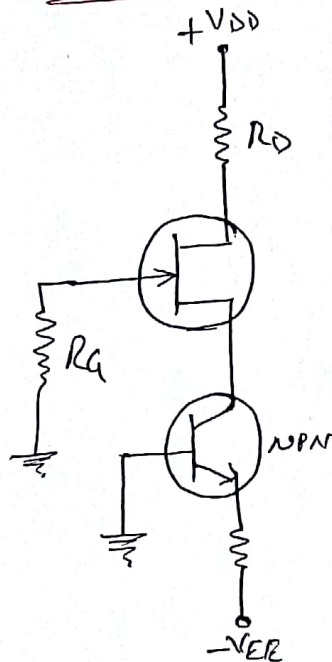


Fig (E): Current Source Bias.

When the drain supply voltage V_{DD} is not large, there may be not be enough gate voltage to swamp out the variations in V_{GS} . In such a case current-source bias (Fig E) may be used. In this arrangement, the BJT pumps a fixed current through the JFET. The drain current is given by

$$I_D = \frac{V_{EE} - V_{BE}}{R_E} \quad (12)$$

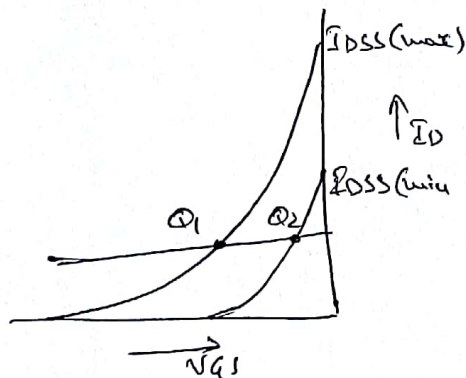


Fig (F):

Figure (F) illustrates how effective current-source bias is. Both Q points have the same value of drain current. Although V_{GS} is different for each Q point, V_{GS} no longer has any effect on the value of drain current.