QUESTION BANK (Academic Year 2018-19)
SWITCHING THEORY AND LOGIC DESIGN

II Year B-TECH

UNIT-1

1. Implement the following functions using NAND gates.

$$F_1 = A\ B + CD\ + (BC)^{|}$$
$$F_2 = WX^{|} + X^{|}Y(Z + W^{|})$$

2. Find the complement of the following Boolean functions and reduce them to minimum number of literals.

$$(BC^{|} + A^{|}D)(AB^{|} + CD^{|}$$
$$(B^{|}D + A^{|}BC^{|} + ACD + AB^{|}C)$$

3.a) Convert the given expression in standard SOP form f(A,B,C)=AC+BA+BC
b) Convert the given expression in standard POS form y=A. (A+B+C)

4.a) Given the 8bit data word 01011011, generate the 12 bit composite word for the hamming code that corrects and detects single errors.
b) Perform the following addition using excess-3 code. I) 386+756 ii) 1010 + 444

5. *a) i.)Represent +65* and -65 in sign magnitude, sign 1's complement and sign 2's Complement representation. ii.)Explain about Weighted and non-weighted codes

b) Using 10's complement, subtract i) 72532_{10}-3250_{10} ii) 3250_{10}-72532_{10}. What do you infer from the results?

6 a i) Perform $(24)_{10} - (56)_{10}$ in BCD using 9's complement

ii)) Convert $(97.75)_{10}$ to base 2.

b i) Convert $(2468)_{10}$ to ( ) $_{16}$

ii.) What is the advantage of 1's and 2's complement in computers. Represent +45 and -45 in sign-magnitude, sign-1's complement and sign-2's complement representation.

UNIT-2

1. Minimize the following function using K-map and also verify through tabulation method. F (A, B, C, D) = ∑(1,4,5,7,8,9,12,14)+d (0, 3, 6, 10).
2. Simplify the following Boolean expressions using K-map and implement it by using NOR gates. a) F(A,B,C,D)= $AB^{|}C^{|} + AC + A^{|}CD^{|}$
b)F(W,X,Y,Z)== $W^{|}X^{|}Y^{|}Z^{|} + WXY^{|}Z^{|} + W^{|}X^{|}YZ + WXYZ$

3 a) Reduce the following function using k-map technique F (A, B, C, D) =π(0,2,3,8,9,12,13,15)
b) Minimize the expression using k-map y= $A + B + C^{|}\,A + B + C\,A^{|} + B^{|} + C^{|}\,A^{|} + B + C\,(A + B + C)$
4. Simplify the following using tabulation method y(w,x,y,z)= $\sum m$(1,2,3,5,9,12,14,15)+ +d(4,8,11)
5 a.) What are the basic operations in Boolean algebra?

b.)What are the advantages of tabulation method over K-map?

UNIT-3

1. a) Design a excess-3 adder using 4-bit parallel binary adder and logic gates.
   b) What are the applications of full adders?
2. a) Design BCD to gray code converter and realize using logic gates.
   b) Design a 1:8 demultiplexer using two 1:4 demultiplexer.
3. a) Design and implement a two bit comparator using logic gates.
   b) Implement full adder using decoder and OR gates.
   .
4. a) Implement the following switching function using a Four input multiplexer
   $F(A, B, C, D) = \Sigma m\ (0, 1, 2, 4, 6, 9, 10, 13, 14)$
   b) A Combinational circuit is defined by the following three Boolean functions
   $F_1 = x'y'z' + xz$ $F_2 = xy'z' + x'y$ $F_3 = x'y'z + xy$
   Design the circuit with a decoder and external gates.

5. a) Define decoder. Construct 3x8 decoder using logic gates and truth table.
   b) Define an encoder. Design octal to binary encoder

6.
   a) Implement a full adder with two 4×1 multiplexers.
   b) Implement Half adder using 5 NAND gates

Unit-4

1. A) Derive the PLA programming table for the combinational circuit that squares a 3 bit Number.
   b) Implement the following Boolean functions using PAL.

$W(A, B, C, D) = \Sigma m(0,2,6,7,8,9,12,13)$

$X(A, B, C, D) = \Sigma m(0,2,6,7,8,9,12,13,14)$

$Y(A, B, C, D) = \Sigma m(2,3,8,9,10,12,13)$

$Z(A, B, C, D) = \Sigma m(1,3,4,6,9,12,14)$

2. a) Design a BCD to excess-3 code converter and implement using suitable PLA.
   b) Implement the following functions using a PROM

i) $F(w,x,y,z) = \sum(1,9,12,15)$

ii) $G(w,x,y,z) = \sum(0,1,2,3,4,5,7,8,10,11,12,13,14,15)$

3a) Implement the following Boolean functions using PLA.

$A(x,y,z) = \sum m(1,2,4,6)$

$B(x,y,z) = \sum m(0,1,6,7)$

$C(x,y,z) = \sum m(2,6)$

b) Design a combinational circuit using PROM that accepts 3-bit binary number and generates its equivalent excess-3 code.

4. a) Draw the logic diagram of a SR latch using NOR gates. Explain its Operation using excitation table.

b) Convert D flip-flop into T and JK flip-flops.

5 a) Implement 4 bit binary to gray code conversion logic functions in PLA.

b) Obtain programmable logic to implement the following functions in PLA.

$x(A, B, C, D) = \sum m(0, 2, 6, 7, 8, 9, 12, 13, 14)$

$y(A, B, C, D) = \sum m(0, 3, 7, 9, 11, 12, 14)$

6a) Design a BCD to excess-3 code converter using

i) ROM ii)PAL

b). Give the comparison between PROM, PLA and PAL.

c) Write short notes on PLA.

Unit-5

1. Convert the following
   a) JK flip-flop to T flip-flop
   b) RS flip-flop to D flip-flop
2. a) Draw the logic diagram of a JK flip- flop and using excitation table explain its operation.
   b) What do you mean by triggering? Explain the various triggering modes with examples
3. a) Draw the logic diagram of a SR latch using NOR gates. Explain its Operation using excitation table.
   b) Convert D flip-flop into T and JK flip-flops
   4 a) Construct a JK flip flop using a D flip flop, a 2x1 multiplexer and an inverter.
   b) Draw the schematic circuit of RS master slave flip flop. Give its truth table and justify the entries in the truth table.
   5. a) Distinguish between combinational and sequential logic circuits.
   b) Convert a D flip flop into
   i) SR flip flop ii) JK flip flop iii) T flip flop.
   6 a) Define a sequential system and explain how it differs from a combinational system..
   b) Draw the circuit of 4 bit Johnson counter using D flip flops and explain its operation with the help of bit pattern

Unit-6

1. a) Draw the diagram of Mealy type FSM for serial adder.
   b) Draw the circuit for Moore type FSM.
2. a) Convert the following Mealy machine into a corresponding Moore Machine.

8. PS	9. NS	a. Z
	10. X=0	11. X=1
12. A	13. C,0	14. B,0
15. B	16. A,1	17. D,0
18. C	19. B,1	20. A,1
21. D	22. D,1	23. C,0

b) Convert the following Moore machine into a corresponding Melay Machine

24. PS	. NEXT STATE		25. OUTPUT 26. Z
	27. X=0	28. X=1	
29. A	30. D	31. B	32. 0
33. B	34. B	35. C	36. 1
37. C	38. C	39. D	40. 0
41. D	42. D	43. B	44. 0

3. Find the equivalence partition and a corresponding reduced machine in a standard form for a Given machine.

PS	NS	Z
	X=0	X=1
A	B,0	E,0
B	E,0	D,0
C	D,1	A,0
D	C,1	E,0
E	B,0	D,0
F	C,1	C,1
G	C,1	D,1
H	C,0	A,1

4 a) distinguish between moore and melay machines?
(b) Write capabilities and limitations of finite –state machine?
5(a) draws and explain moore circuit?
(b)draw and explain melay circuit?