VLSI DESIGN Question Bank

Academic Year :2018-2019
Department :ECE
Year/Semester :III YEAR– II SEMESTER
Subject : VLSI DESIGN

UNIT-1

1a)Derive the expression for Ids versus Vds relationship? [5]

b) An nMOS transistor is operating in active region with the following parameters:

VGS=3.9V,Vtn=1V,W/L=100,μnCox=90μA/V2. Find ID and RDS.

2a) Explain different steps involved in the IC fabrication? [5]

b) Draw the circuit for NMOS inverter and explain its operation and characteristics[5]

3 a) Explain the MOS transistor operation with the help of neat sketches in the

Enhancement mode.Depletion mode[5]

b) Explain how the BiCMOS inverter performance can be improved. [5]

4 a) Explain the steps of CMOS fabrication with suitable sketch. and explain its operation and characteristics [5]
b) What are the advantages of BICMOS process over CMOS ? [5]

5 a) Derive the expression for the threshold voltage of MOSFET. [5]
b) Explain the figure of merit of a MOS transistor[5]

6 a) Explain latch up problems in CMOS circuits? [5]
b) Explain the term output conductance, using necessary equations. [5]

UNIT-2

1 a) Explain 2μm CMOS design rules for wires. [5]
b) Design a stick diagram for CMOS logic Y= (A+B+C)/ [3]
c) Define stick diagram and layout diagram? [2]

2 a) Explain 2μm Double Metal, Double Poly. CMOS / BiCMOS Rules. [5]
b) Design stick diagram for NMOS logic Y= ((A+B).C)/ [5]

3 a) What is the need for design rules? Explain different types of design rules. [5]
b) Draw the stick diagram layout for y= (A.B) +E+ (C.D) [5]

4 a) What is a stick diagram and explain different symbols used for components in stick diagram. [5]
b) Design a layout diagram for pMOS logic Y= (AB+CD) [5]

5. a) Explain the color code used for drawing stick diagram for NMOS and PMOS designs. [5]
b) What are the different types of contact cuts made during the fabrication of an IC? Which one is commonly used and why? [3]
c) Draw the stick diagram for CMOS inverter[2]

6 Design a stick diagram for two input CMOS NAND and NOR gates. [10]

UNIT-3

1. a) Explain briefly about sheet resistance? Derive the Expression for RS[5]
b) Calculate the ON resistance from VDD to GND for the nMOS and CMOS inverter circuits. [5]

2. a) Define standard unit capacitance? Explain. [5]
b) Explain the problem of driving large capacitive loads? How such loads can be driven? [5]

3 Discuss the limits of scaling. Why scaling is necessary for VLSI circuits? [10]

4.(a) Define scaling factor? Explain different types of device parameters? [5]
(b) Draw and explain the structure of scaled MOS transistor[5]

5 a) Explain different types of Wiring capacitance for MOS transistors. [5]
b) Realization of gates using NMOS PMOS and CMOS technologies[5]

6(a) What is inverter delay? How delay is calculated for multiple stages. [5]
b)Write about the limits due to subthreshold currents [5]

UNIT -4

1.a) Explain the stuck.-at fault model with example. [5]
b)) Explain the terms. (a) controllability (b) observability (c) fault coverage

2.a) Explain the principles of Built in self Test. [5]

b)Explain how serial –scan testing is implemented. [5]

3 a)Explain the different kinds of physical faults that can occur on a cmos chip and relate them to typical circuit failures. [5]
b)Explain the Ad hoc testing principle? [5]

4 a) Explain how an electrostatic discharge event could cause on a cmos chip. [5]
b) Explain the power distribution subsystem of a chip? [5]

5 Explain the input/output subsystem of L(di/dt) noise.
6 Explain the clock mechanisms of generation and distribution[10]

UNIT -5

1a) Explain the basic architecture of FPGA. [5]
b) Explain the FPGA design process. [5]

2 a) How to design FPGA-Based PCBs? Explain. [5]
b) Write about FPGA families of different vendors[5]

3(a) What parameters to be consider while identifying the FPGA [5]
(b)What is the need of a FPGA? And write its applications[5]

4(a) Explain the FPGA implementation of Half adder [5]
(b) Explain the FPGA implementation of Full adder [5]

5 (a)Explain the term logic synthesis[5]
(b) Explain the design flow of low level synthesis to high level synthesis[5]

UNIT -6

1 (a) why low power is essential in vlsi design for deep sub micro design[5]
(b)what are the sources of power dissipation[5]

2(a) Explain the switching power dissipation glitching power dissipation [5]
(b) Explain the short circuit power dissipation[5]
3 Explain the static power dissipation [10]

4(a) why leakage power is an issue? [5]
(b) How to control the power dissipation in DSM[5]

5(a) Explain the supply voltage scaling in power dissipation[5]

(b) Explain the dynamic voltage scaling in power dissipation[5]

6(a) How to reduce the switching capacitance[5]
(b) Explain the terms parallelismpipelining [5]