

Integrated Circuits

- * Transistor was invented by William Schottky
- * Integrated circuit was invented by Jack Kilby. In 2000, he got Nobel prize.

Statement:-

IC circuit reflects capability of semiconductor industrial to fabricate complex electronic circuit.

Statement:- Large number of components are fabricated on single silicon chip.

Advantages of IC:-

1. Space is reduced (or) size is reduced.
2. cost is Less.
3. Delay is reduced between components.
4. Speed is more & improved performance.
5. Reliability is more.
6. power dissipation is Less.

Op - Amp:- reduce noise

* The operational amplifier is most versatile active element among linear IC's:

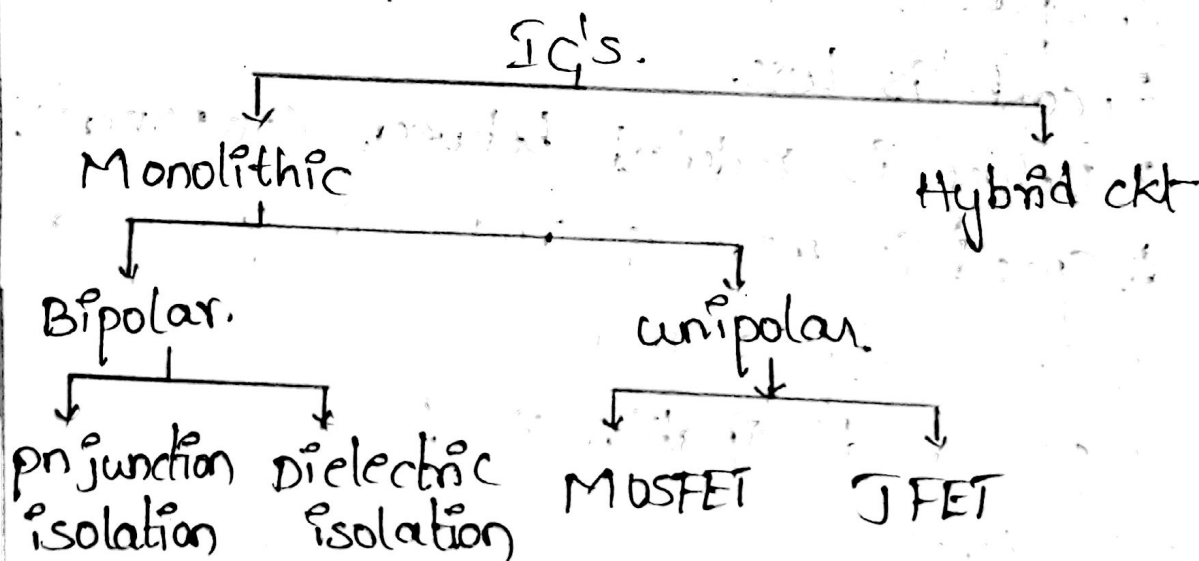
* It is a device which performs various operations such as addition, subtraction, multiplication, division, integration, differentiation.

Popular Linear IC's are

- 1, 741 Op-Amp
- 2, 555 timer
- 3, 565 PLL

Classification of IC's:

- 1, Digital IC's: It operate on two voltage levels i.e., Logic 0, Logic 1.
- 2, Linear IC's: It perform Linear functions like Amplification, mixing, modulation, Oscillation etc.



IC generation:

Small Scale integration - SSI

3-30 gates (or) 100 transistor/chip.

Applications:

Logic gates and flipflops.

Medium Scale Integration - MSI

30 to 300 gates (or) 100 to 1000 transistor/chip

Applications:-

Counters, Multiplexers, Adders.

Large Scale Integration - LSI

300- 3000 gates / chip (or) 1k to 20k transistor.

Applications:-

8 bit Microprocessor, RAM, ROM

Very Large Scale Integration - VLSI

3000 gates / chip or 20k to 100k transistor/chip

Applications:-

16 bit / 32 bit Microprocessor.

Ultra Large Scale Integration - ULSI

10^6 to 10^7 transistor / chip.

Application: Special process.

Gate Scale Integration - GSI

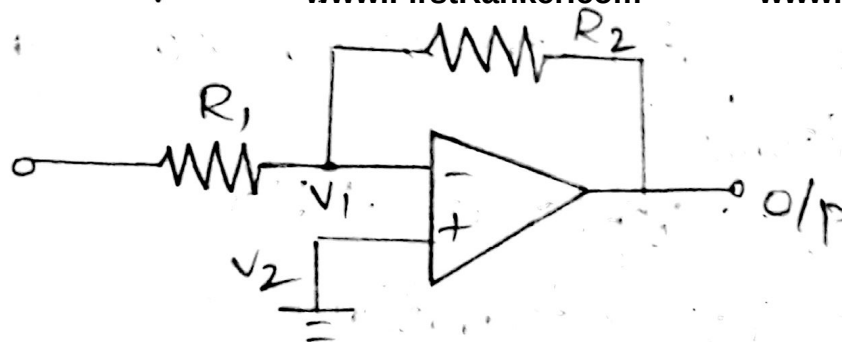
10^7 transistor / chip.

Operational Amplifier:-

Inverting o/p  o/p terminal

non inverting i/p

Inverting terminal produces o/p as 180° phase shift. Non inverting terminal produces o/p as in phase.



$$V_0 = V_d A_{OL}$$

$$V_d = V_1 - V_2; \quad A_{OL} = \text{Open Loop gain}$$

$$V_d = \frac{V_0}{A_{OL}}$$

$$V_0 = 5V$$

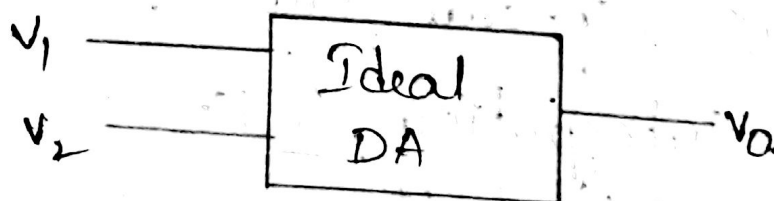
$$A_{OL} = 10^6$$

$$V_1 - V_2 = \frac{V_0}{\infty} = 0$$

$$V_d = \frac{5}{10^6} = 5 \mu V$$

$$V_1 = V_2$$

If non-inverting terminal is grounded, inverting terminal is also acts as ground potential through there is no physical connection between inverting terminal & ground. This principle is called virtual ground concept.



$$V_0 \propto V_1 - V_2$$

$$V_0 = A_d V_d$$

$$A_d = \frac{V_0}{V_d}$$

$$A_d = 20 \log \frac{V_0}{V_d} \text{ dB}$$

$$V_C = \frac{V_1 + V_2}{2}$$

$$V_O = A_C V_C$$

$$V_O = A_D V_D + A_C V_C$$

$$V_O = A_D V_D$$

Common mode rejection ratio (CMRR) :-

The ability of differential amplifier to reject Common mode signal is called Common mode rejection ratio. It is expressed by a ratio of A_D & A_C . In ideal sense CMRR is ∞ because $A_D = \infty$ & $A_C = 0$ but in practical sense it is very high.

$$C = \left| \frac{A_D}{A_C} \right|$$

$$C(\text{dB}) = 20 \log \left| \frac{A_D}{A_C} \right|$$

$$V_O = A_D V_D + A_C V_C$$

$$= A_D V_D \left[1 + \frac{A_C V_C}{A_D V_D} \right]$$

$$= A_D V_D \left[1 + \frac{1}{A_D/A_C} \frac{V_C}{V_D} \right]$$

$$= A_D V_D \left[1 + \frac{1}{C} \frac{V_C}{V_D} \right]$$

Features of differential Amplifier:-

1. High differential gain (A_D)

2. Low (A_C)

3. High CMRR

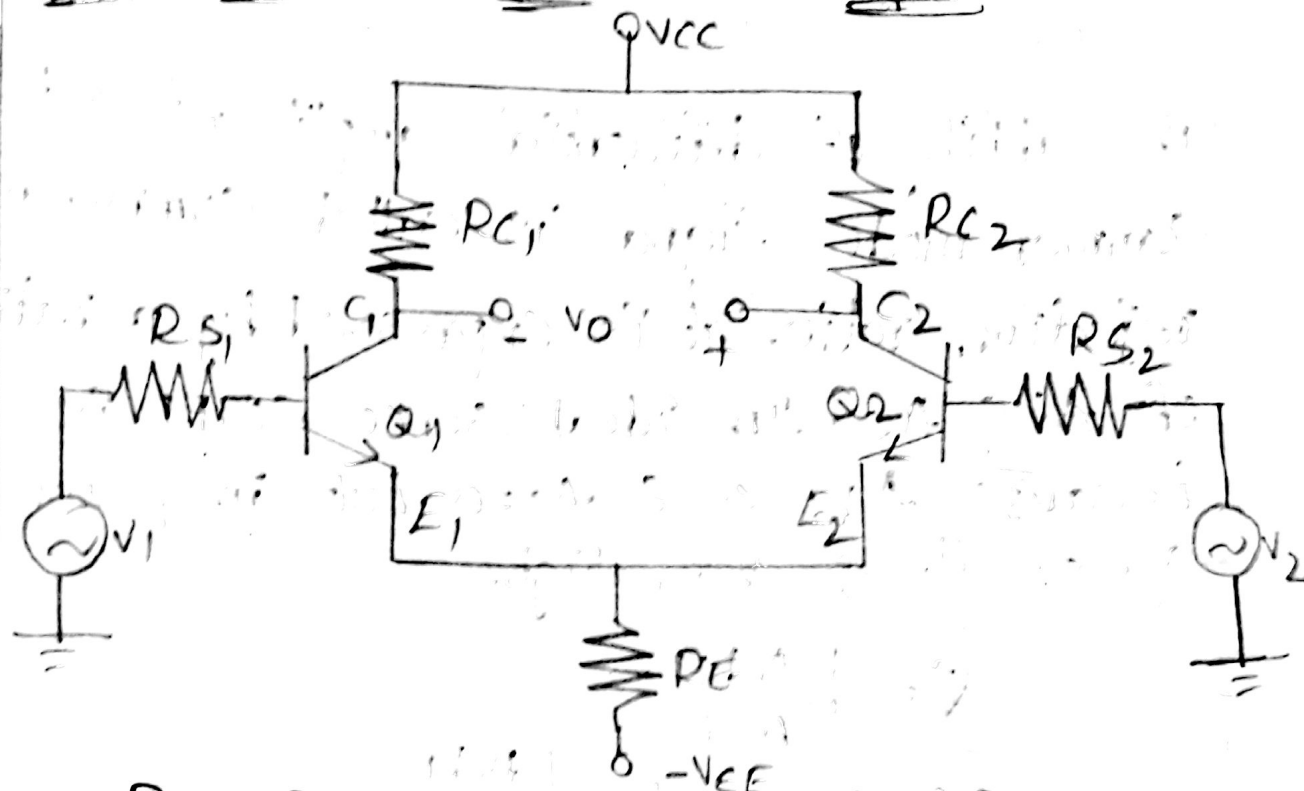
6. High i/p impedance.

7. Large bandwidth

8. o/p impedance is low.

9. Low offset voltages & currents

Transistorised Differential amplifier



$$RC = RC_1 = RC_2$$

RE = Emitter resistance

$$RS = RS_1 = RS_2$$

V_1 & V_2 i/p voltage

V_O = o/p voltage

$$V_C = V_{EE}$$

$$Q_1 = Q_2$$

If R_2 is grounded

then $V_2 = 0$

$$V_O = A(V_1 - V_2)$$

$V_O = AV_1$ = Non-inverting terminal

In the transistorised differential amplifier, transistors are identical output is taken between two collectors. Since V_{CC} is common, DC potential of collectors are equal. Hence the o/p is measured across collectors. This o/p is called balanced o/p. If o/p is taken b/w C_1 & ground, C_2 & ground it is called unbalanced o/p.

We have $V_o = A(V_1 - V_2)$

where A is gain of amplifier.

If B_2 is grounded $V_2 = 0$.

$$\therefore V_o = AV_1$$

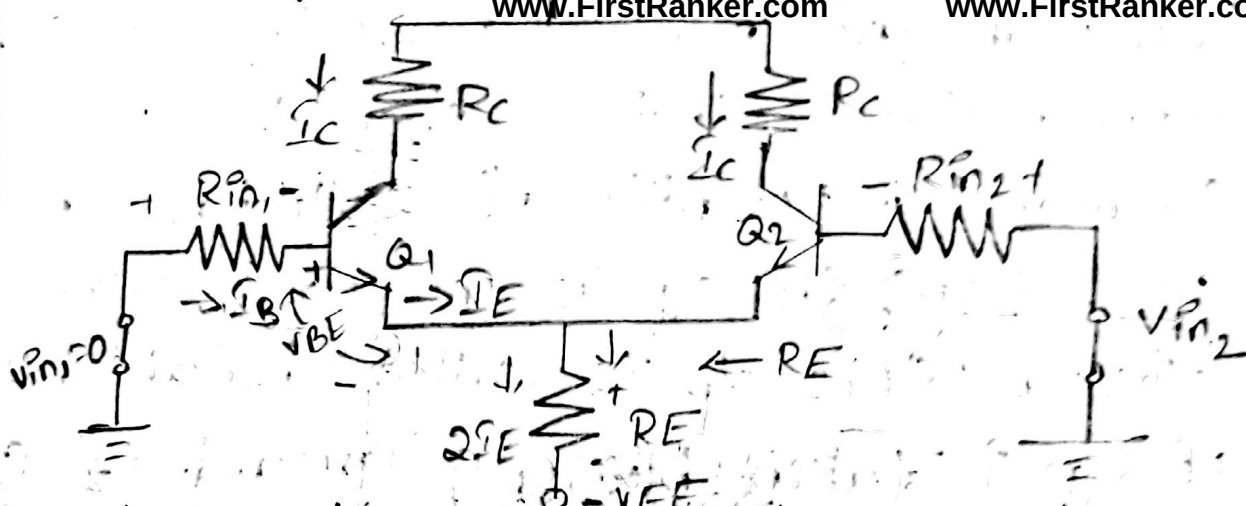
Since V_o & V_1 are in phase,

The ~~pin~~ base B_1 at which i/p voltage is applied is called non-inverting terminal.

If B_1 is grounded $V_1 = 0$ then $V_o = -AV_2$

which implies V_o & V_2 are 180° out of phase.

Hence B_2 at which i/p voltage is applied is called inverting terminal.



Applying KVL to B-E Loop.

$$-R_m I_B - V_{BE} - R_E (2I_E) + V_{EE} = 0$$

$$I_E = \frac{V_{EE} - V_{BE}}{2R_E + \frac{R_m}{\beta_{DC}}}$$

$$I_B = \frac{I_E}{\beta_{DC}}$$

$$\approx \frac{V_{EE} - V_{BE}}{2R_E} \quad \left[\because \frac{R_m}{\beta_{DC}} \ll 2R_E \right]$$

Since V_{BE} is constant, I_E is independent of V_{EE} & $2R_E$

The voltage of emitter of Q_1

$$V_E = (-I_B R_m - V_{BE}) \approx -V_{BE}$$

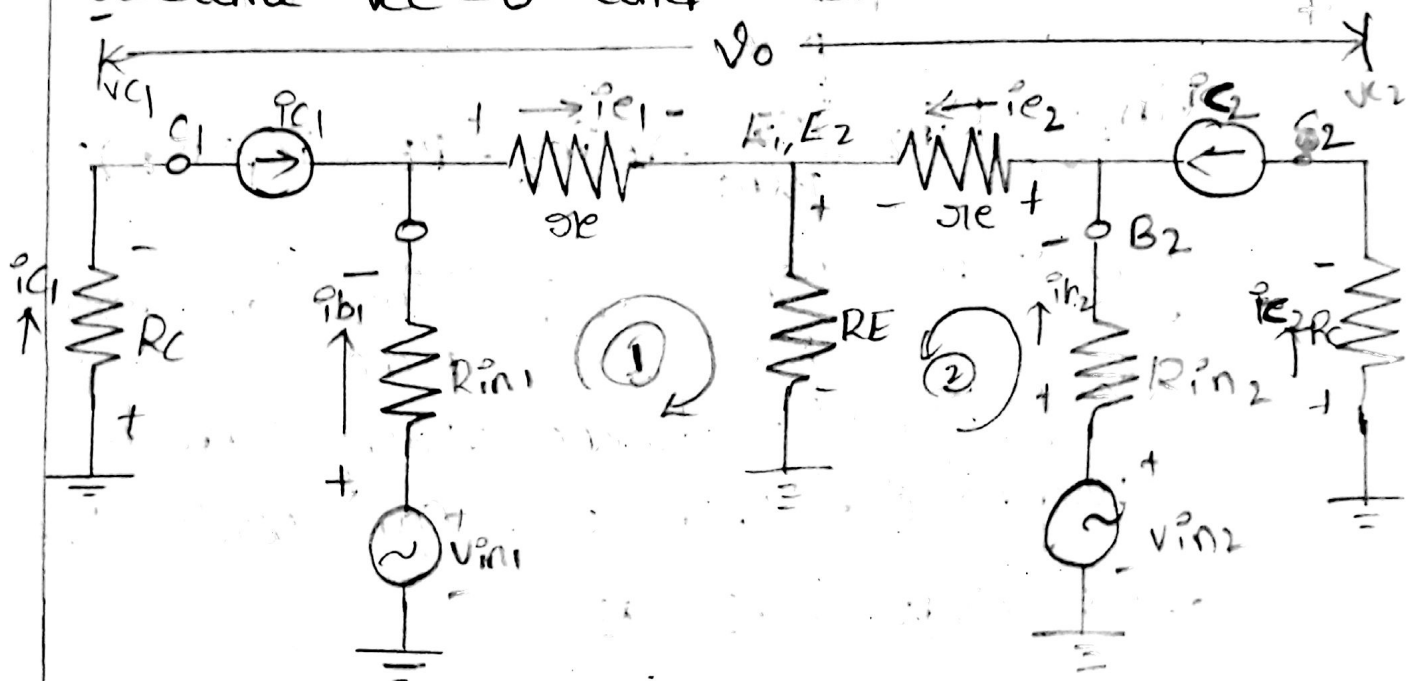
$\therefore I_B$ is very small

$$V_C = V_{CC} - I_C R_C$$

$$V_{CE} = V_C - V_E = V_{CC} - I_C R_C - (-V_{BE})$$

$$= V_{CC} + V_{BE} - I_C R_C \quad \text{--- (2)}$$

In AC Analysis we calculate the differential gain and differential input resistance. we use the transistor T equivalent models in place of the transistors and assume $V_{CC} = 0$ and $V_{EE} = 0$.



AC Equivalent circuit.

Before we proceed we assume that

$$I_{E1} = I_{E2}$$

$$\Rightarrow r_{e1} = r_{e2} = r_e = \frac{26 \text{ mV}}{I_E}$$

which is called AC resistance
writing Kirchhoff voltage law for the
loops ① & ②.

loop ①

$$V_{in1} - R_{in1} i_{b1} - i_{e1} r_e - R_E (i_{e1} + i_{e2}) = 0$$

$$V_{in2} - i_{b2} R_{in2} - r_e i_{e2} - R_E (i_{e1} + i_{e2}) = 0$$

putting $i_{b1} = \frac{i_{e1}}{\beta_{AC}}$ and $i_{b2} = \frac{i_{e2}}{\beta_{AC}}$

$$V_{in1} - R_{in1} \frac{i_{e1}}{\beta_{AC}} - i_{e1} r_e - R_E (i_{e1} + i_{e2}) = 0$$

$$V_{in2} - R_{in2} \frac{i_{e2}}{\beta_{AC}} - i_{e2} r_e - R_E (i_{e1} + i_{e2}) = 0$$

generally $\frac{R_{in1}}{\beta_{AC}}$ and $\frac{R_{in2}}{\beta_{AC}}$ are very very small. Hence they can be neglected. Then we can write the above expressions as.

$$(r_e + R_E) i_{e1} + R_E i_{e2} = V_{in1} \quad \text{--- (A)}$$

$$R_E i_{e1} + (r_e + R_E) i_{e2} = V_{in2} \quad \text{--- (B)}$$

$$\begin{vmatrix} r_e + R_E & R_E \\ R_E & r_e + R_E \end{vmatrix} \begin{vmatrix} i_{e1} \\ i_{e2} \end{vmatrix} = \begin{vmatrix} V_{in1} \\ V_{in2} \end{vmatrix}$$

i_{e1} & i_{e2}

Solving A & B for i_{e1} & i_{e2} using Cramer's rule at

$$i_{e1} = \frac{v_{in2} \begin{vmatrix} r_e + R_E & R_E \\ R_E & r_e + R_E \end{vmatrix}}{\begin{vmatrix} r_e + R_E & R_E \\ R_E & r_e + R_E \end{vmatrix}}$$

$$= \frac{(r_e + R_E) v_{in1} - R_E v_{in2}}{(r_e + R_E)^2 - R_E^2} \quad \text{--- (C)}$$

$$i_{e2} = \frac{\begin{vmatrix} r_e + R_E & v_{in1} \\ R_E & v_{in2} \end{vmatrix}}{\begin{vmatrix} r_e + R_E & R_E \\ R_E & r_e + R_E \end{vmatrix}}$$

$$= \frac{(r_e + R_E) v_{in2} - R_E v_{in1}}{(r_e + R_E)^2 - R_E^2} \quad \text{--- (D)}$$

By Dckt-2-

$$V_o = V_{C2} - V_{C1}$$

$$= -R_C i_{C2} - (-R_C i_{C1})$$

$$= R_C (i_{C1} - i_{C2})$$

$$= R_C (i_{e1} - i_{e2})$$

In Transistor
Emitter current
is almost equal
to collector
current

$$V_o = R_C \left[\frac{(r_e + R_E) v_{in1} - R_E v_{in2}}{(r_e + R_E)^2 - R_E^2} \right]$$

$$- \frac{(r_e + R_E) v_{in2} - R_E v_{in1}}{(r_e + R_E)^2 - R_E^2}$$

$$V_o = R_c \left[\frac{(r_e + R_E)(V_{in1} - V_{in2}) + R_E(V_{in1} - V_{in2})}{(r_e + R_E) + R_E} \right]$$

$$= R_c \left[\frac{(r_e + 2R_E)(V_{in1} - V_{in2})}{r_e + 2R_E + R_E + R_E} \right]$$

$$= R_c \left[\frac{(r_e + 2R_E)(V_{in1} - V_{in2})}{r_e(r_e + 2R_E)} \right]$$

$$= \frac{R_c}{r_e} V_d$$

$$V_o = \frac{R_c}{r_e} V_d, \quad A_d = \frac{V_o}{V_i} = \frac{R_c}{r_e}$$

Voltage gain is independent on R_E

Differential Input Resistance

It is defined as Equivalent resistance that to be measured at either input terminal with other terminal grounded. Thus

$$R_{i1} = \left. \frac{V_{in1}}{i_{b1}} \right|_{V_{in2}=0}, \quad R_{i2} = \left. \frac{V_{in2}}{i_{b2}} \right|_{V_{in1}=0}$$

$$R_{i1} = \left. \frac{V_{in1}}{i_{b1}} \right|_{V_{in2}=0}$$

$$\begin{aligned}
 &= \frac{V_{in1}}{r_{e1}/\beta a c} \quad V_{in2} = 0. \\
 &= \frac{\beta a c V_{in1}}{(r_e + R_E) V_{in1} - R_E (0)} \quad \text{from (c).} \\
 &= \frac{\beta a c (r_e^v + 2 r_e R_E)}{(r_e + R_E)} \\
 &= \frac{\beta a c (r_e) (r_e + 2 R_E)}{r_e + R_E}
 \end{aligned}$$

If $R_E \gg r_e$ Thus r_e can be neglected

$$= \frac{\beta a c r_e (2 R_E)}{R_E}$$

$$R_{i1} = 2 (\beta a c r_e)$$

$$R_{i2} = 2 (\beta a c r_e)$$

output resistance: output resistance is a resistance measured between collector and ground.

$$R_{o1} = R_{o2} = R_C$$

Important points:

* Current gain of differential Amplifier is undefined. Hence current will not be

is also a small signal amplifier. Hence it is used as a voltage amplifier not as current amplifier (or) power amplifier.

*

Differential gain

$$A_d = \frac{R_C}{r_e}$$

AC Analysis is being done by using 'r' parameters. It can be done by 'h' parameters also.

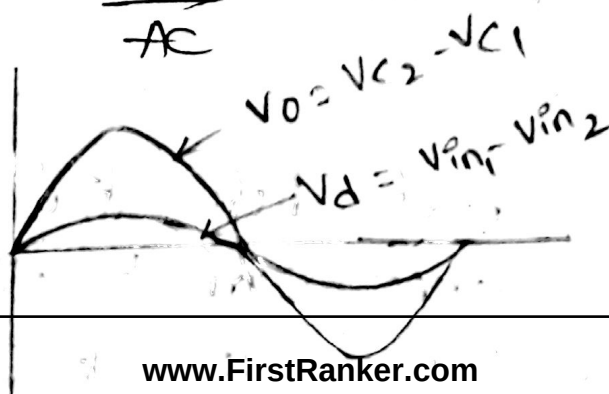
$$1) A_d = \frac{h_{fe} R_C}{R_s + h_{ie}}$$

$$2) R_i = 2(R_s + h_{ie})$$

$$3) R_o = R_C$$

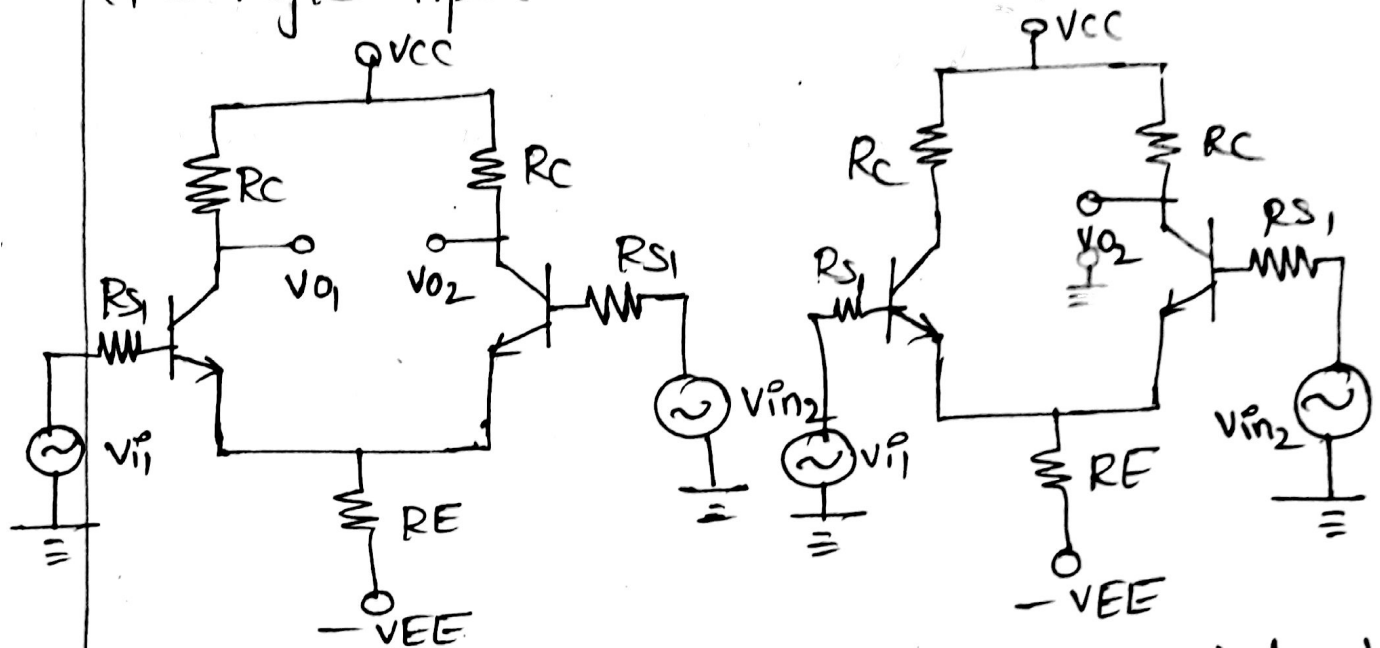
$$4) A_c = \frac{h_{fe} R_C}{2R_E(1 + h_{fe}) + R_s + h_{ie}}$$

$$5) \rho = \frac{A_d}{A_c}$$

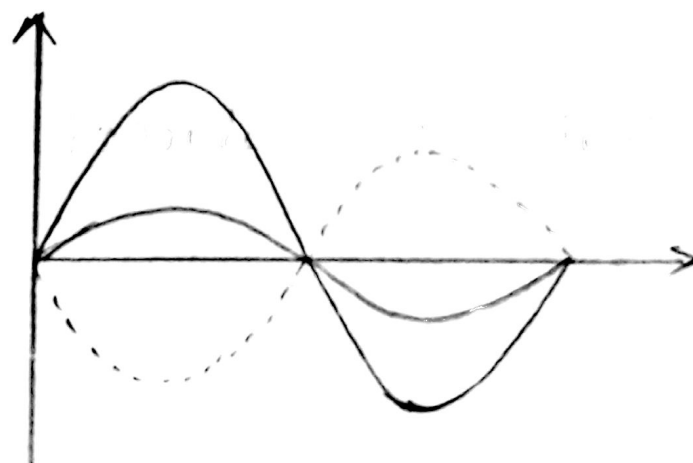


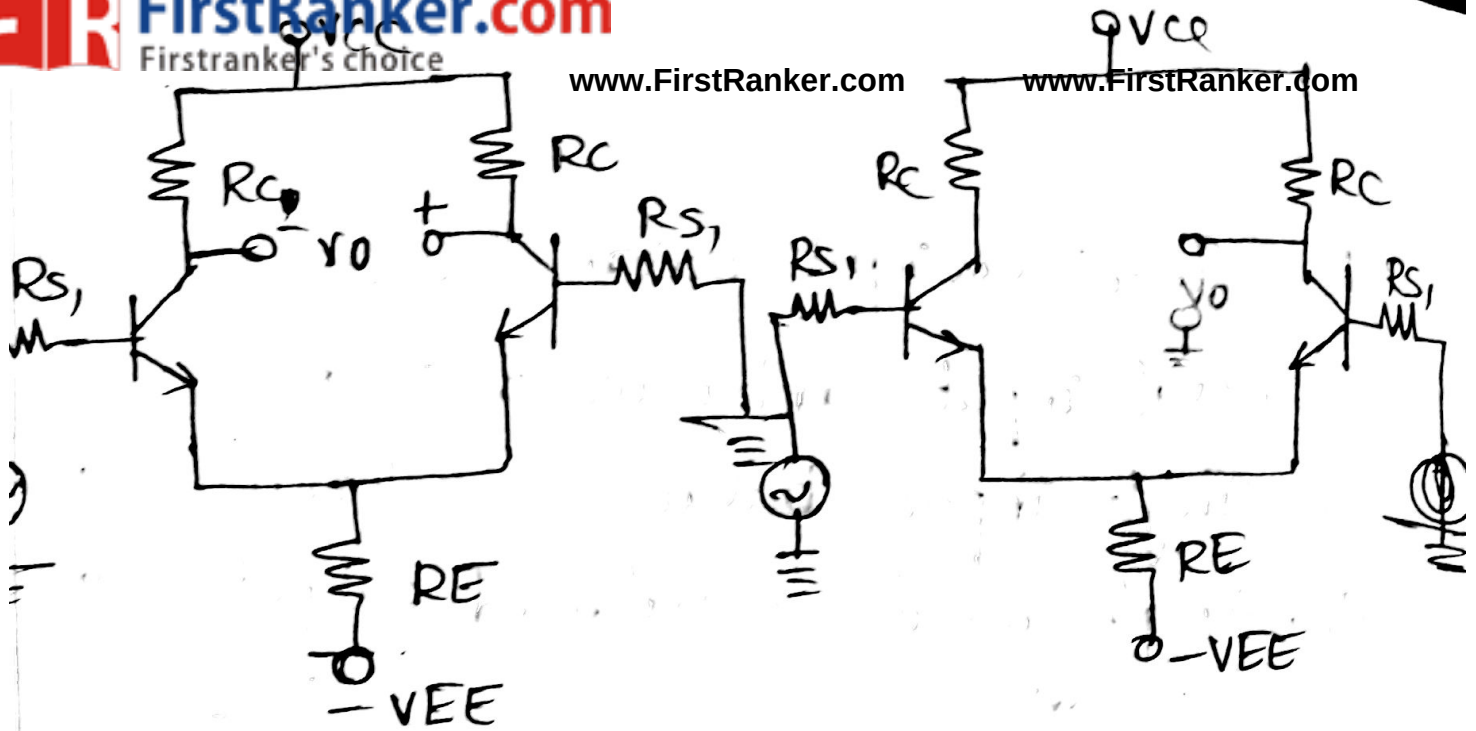
Different Configurations of Differential Amplifier—

1. Differential input balanced output Diff Amplifier
2. Dual input unbalanced output "
3. Single input balanced output "
4. Single input unbalanced output "



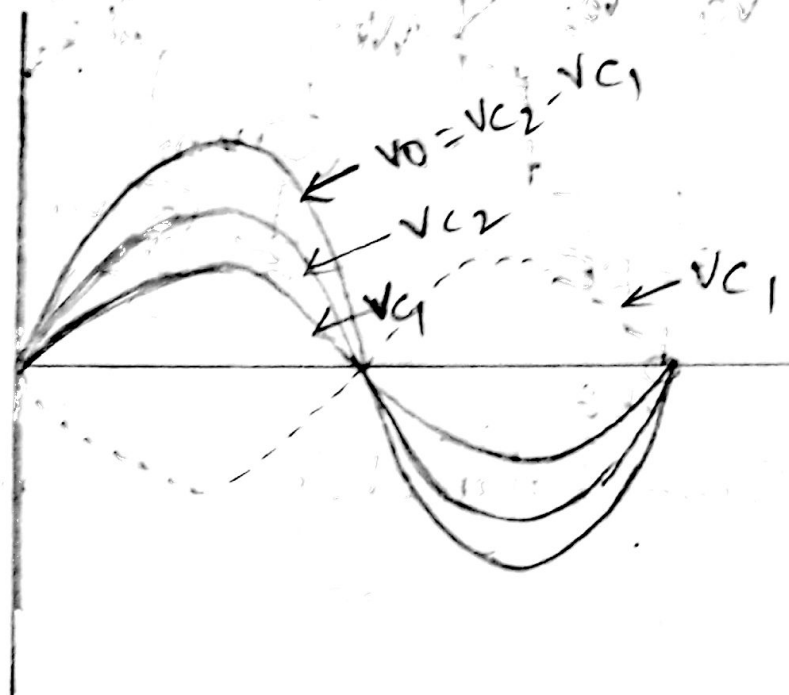
Dual Input balanced o/p. Dual Input unbalanced o/p



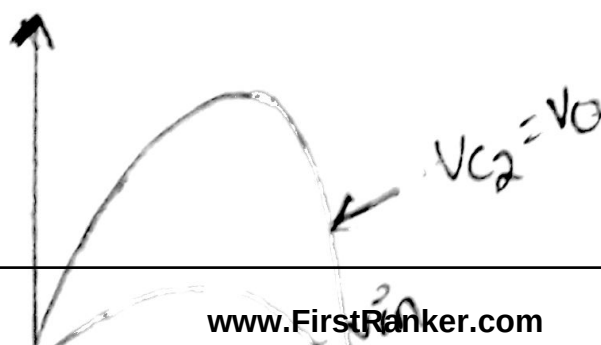


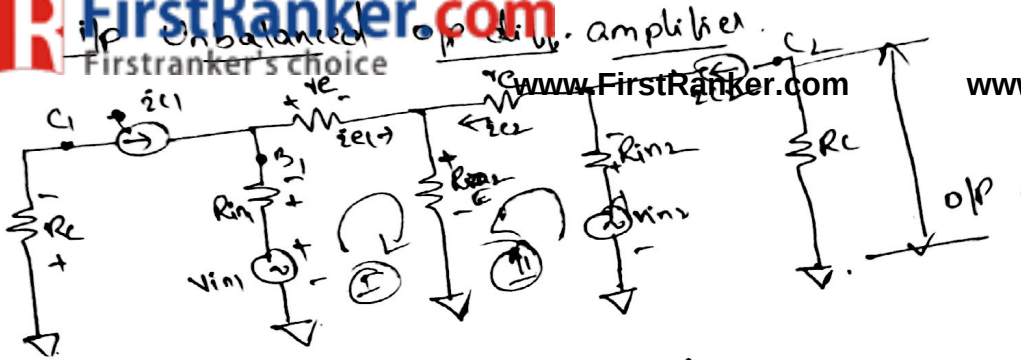
Single i/p balanced o/p

Single i/p unbalanced o/p



Single i/p balanced o/p.





// i_{E1} & i_{E2} same as Dual IP/A.

$$i_{E1} = \frac{V_{in1}(R_E + r_e) - V_{in2}(R_E)}{(r_e + R_E)^2 - R_E^2}$$

$$i_{E2} = \frac{(r_e + R_E)V_{in2} - V_{in1}(R_E)}{(r_e + R_E)^2 - R_E^2}$$

o/p Voltage $V_o = V_{C2} = -i_{C2}R_C$

$$\Rightarrow V_o = -R_C i_{E2}$$

$$= -R_C \left[\frac{V_{in2}(r_e + R_E) - V_{in1}(R_E)}{(r_e + R_E)^2 - R_E^2} \right]$$

$$= R_C \left[\frac{V_{in1}(R_E) - (r_e + R_E)V_{in2}}{(r_e + 2R_E)r_e} \right]$$

$$= R_C \left[\frac{V_{in1}(R_E) - R_E(V_{in2})}{2R_E \cdot r_e} \right]$$

$$r_e + R_E \approx R_E$$

$$= R_C \left[\frac{R_E(V_{in1} - V_{in2})}{2r_e R_E} \right]$$

$$= \frac{R_C}{2r_e} (V_{in1} - V_{in2})$$

$$\frac{V_o}{V_{id}} = \frac{R_C}{2r_e}$$

Cascade differential Amplifier:-

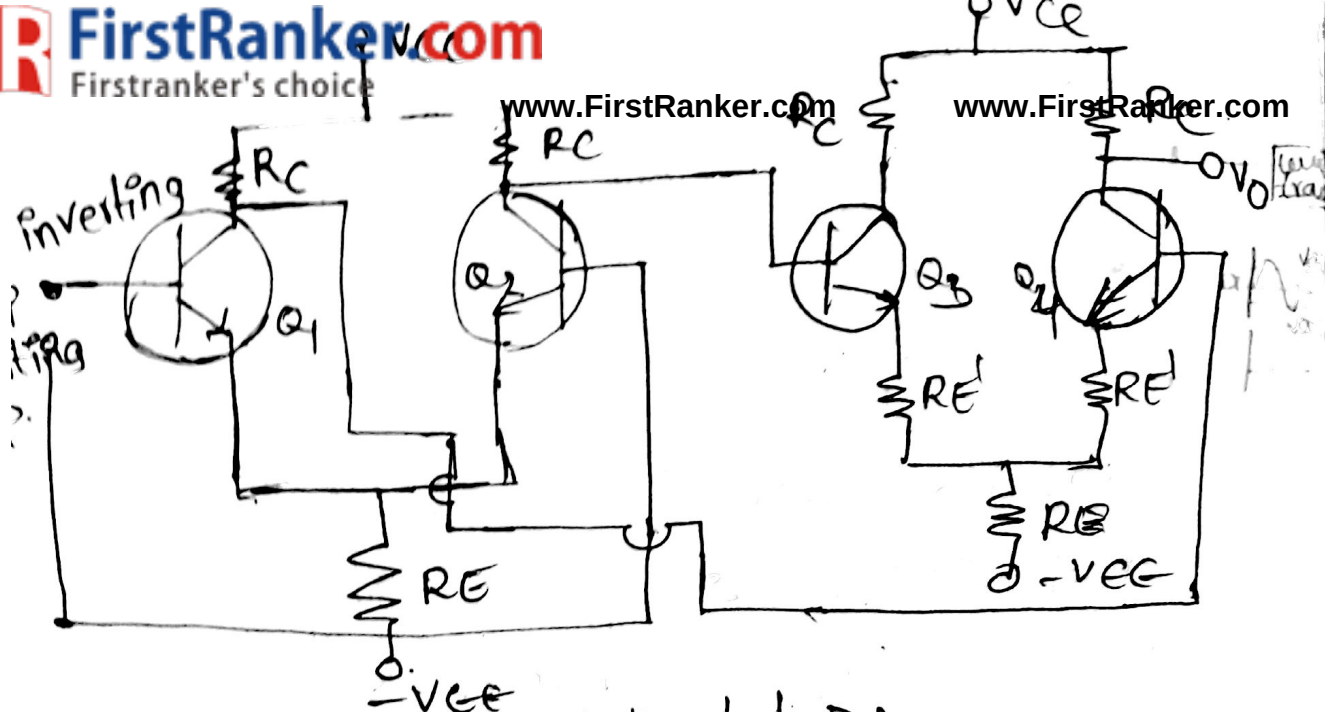
* Cascading is done to increase the output.

* The cascading network first stage is dual flp balanced olp differential amplifier and second stage is single ended ckt. i.e. Dual flp unbalanced olp DA.

* Cascaded differential amplifiers are directly coupled. Therefore coupling capacitors can not be included because due to delays introduced by the capacitor distorts the olp severely and use of differential amplifier becomes meaningless. DC coupled is also called Direct coupling.

* In many cases the transistors and resistors are perfectly matched there is no mismatch.

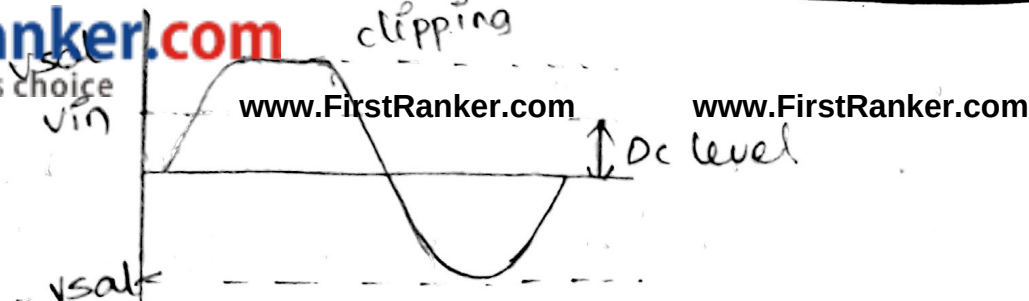
EIAWBS



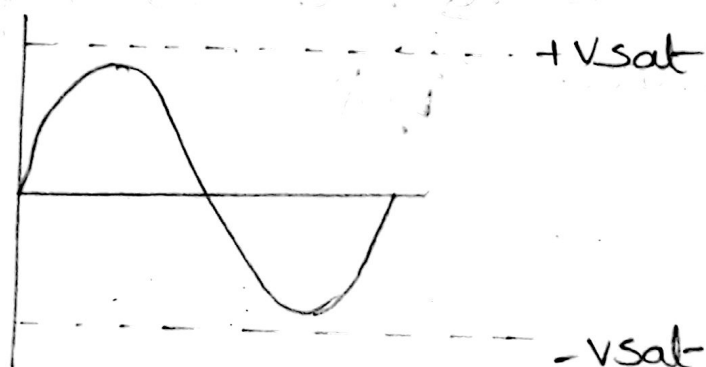
cascaded DA
The Second differential amplifier swamping resistors are added to increase the input Resistance. The first differential amplifier is Dual ip balanced o/p D.A. The Second Diff amplifier is Dual ip unbalanced o/p P.A. The Q_1 o/p is directly connected to Q_4 and Q_2 o/p is directly connected to Q_3 .

Level translator

with cascaded DA dc level of emitters are rise which shifts operating point and emitts the o/p swings and distort the o/p.



without Level translator.



with level translator.

Especially, emitter voltage of 2nd stage introduces lot of dc voltage due to direct coupling. the, DC Level is brought down to zero. Then distortion can be greatly reduced.

The voltage at o/p terminal of 2nd stage is, well above zero voltage. DC voltage is undesirable as limits peak to peak voltage and contributes and distortion.

The final stage included to shift the o/p DC level at the 2nd stage down to zero. Such a stage

The cascaded DA configuration contains level translator in the final stage with an emitter follower configuration. Emitter follower is used due to high input Resistance ✓

If we use emitter follower) i/p impedance very high
it acts as Buffer

Emitter follower

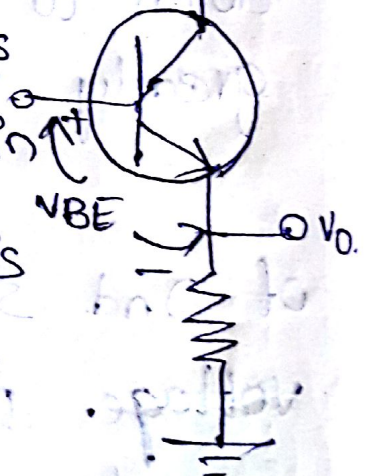
gain = 1

Different ckt's of Level translators:-

1) Emitter follower:- Emitter follower

is a simplest Level translator. It provides High i/p resistance, and

$V_O = V_{in} - V_{BE}$. Since V_{BE} is 0.7V, the dc level shift V_{in} is 0.7V downwards. This is not sufficient. Hence we go for alternatives.



$$V_O = V_{in} - V_{BE}$$

2) Resistor divider network:-

In this circuit $V_O = IR_2$
 $I = \frac{V_{in} - V_{BE} - I(R_1 + R_2)}{R_1 + R_2}$ and

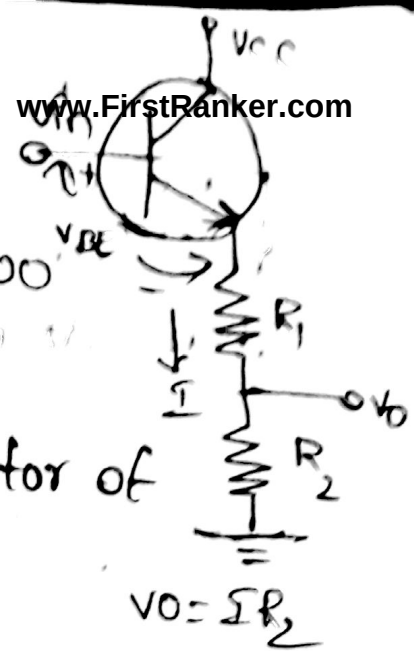
$$V_O = \frac{V_{in} - V_{BE}}{R_1 + R_2} \times R_2$$

By properly choosing R_1 &

R_2 we can bring dc value downward. but there are two disadvantages in the ckt

1. V_o is reduced by a factor of

$$\frac{R_2}{R_1 + R_2}$$



$$V_o = I R_2$$

3. The o/p Impedance is high.

Therefore we go for alternative

3) constant current source level translator;

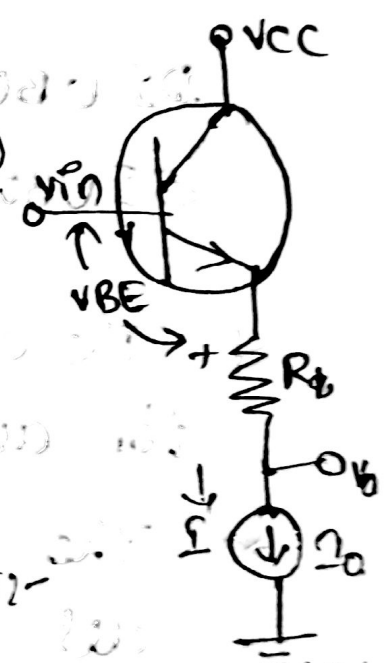
$$\begin{aligned} \text{In this ckt } V_o &= V_{in} - V_{BE} - I_o R_1 \\ &= V_{in} - (V_{BE} + I_o R_1) \end{aligned}$$

The shift is $V_{BE} + I_o R_1$

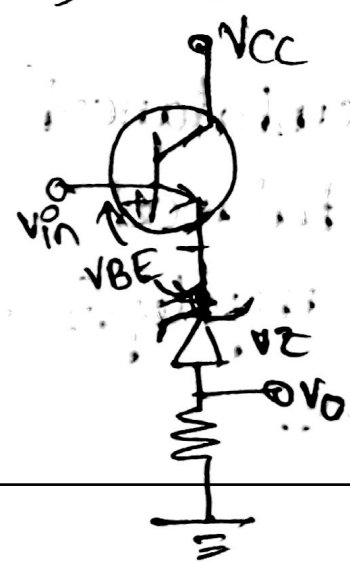
down ward. where I_o is

the constant current

Source



4) Zener diode level translator:-



In this ckt use zener diode for keeping voltage constant
 V_o is given by $V_o = V_{in} - (V_{BE} + V_z)$

Therefore the shift is $V_{BE} + V_z$
downward. The no. of

Configuration	A_d	R_{in}	R_o
DI BODA	R_C / r_e	$2 R_{AC} r_e$	R_C
SI BODA	R_C / r_e	$2 R_{AC} r_e$	R_C
DI UBODA	$R_C / 2 r_e$	$2 R_{AC} r_e$	R_C
SI UBODA	$R_C / 2 r_e$	$2 R_{AC} r_e$	R_C

* The o/p resistors ~~are~~ is R_C and same for all configurations.

* The Differential i/p is same for all configurations.

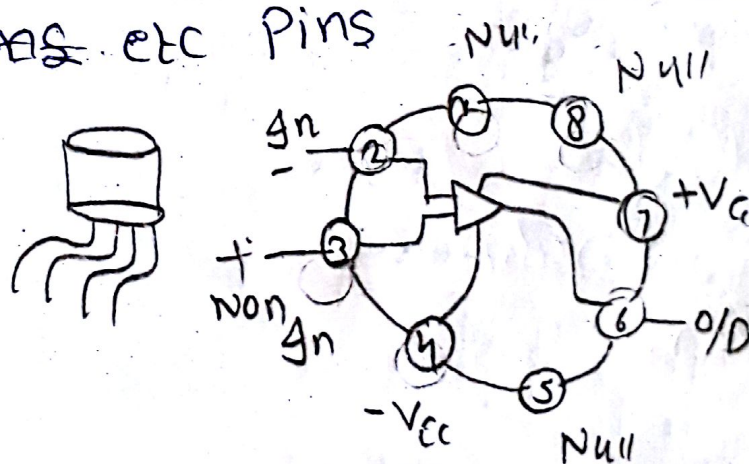
* The Differential gain of unbalanced configurations is half of balanced configuration and DC analysis is same for all configurations.

for protecting the IC's the semiconductor IC's is packaged with plastic or ceramic material. IC's are available with three different types of packages.

- 1) metal can package
- 2) DIP (Dual Inline package)
- 3) Flat package

* metal can package:

In this the IC's are available with 3, 5, 8, 10, 12 pins etc. Pins

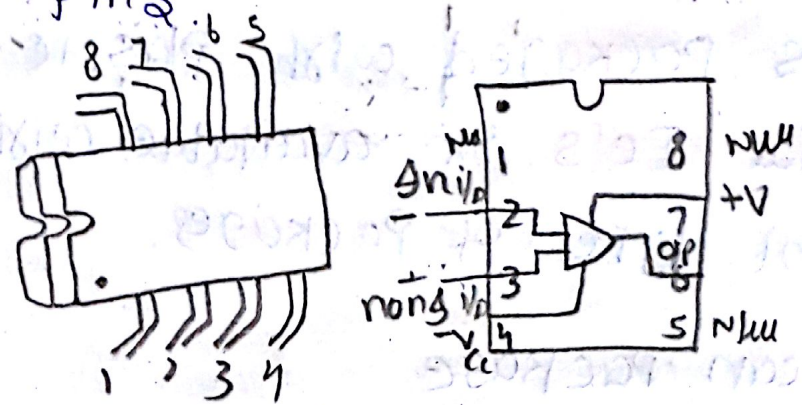


* DIP (Dual Inline package):

In this the IC available with plastic (or) ceramic gates with two sided pins it is available with 3, 5, 8, 10, 14, 16, 20 for analog 40 pins for digital.

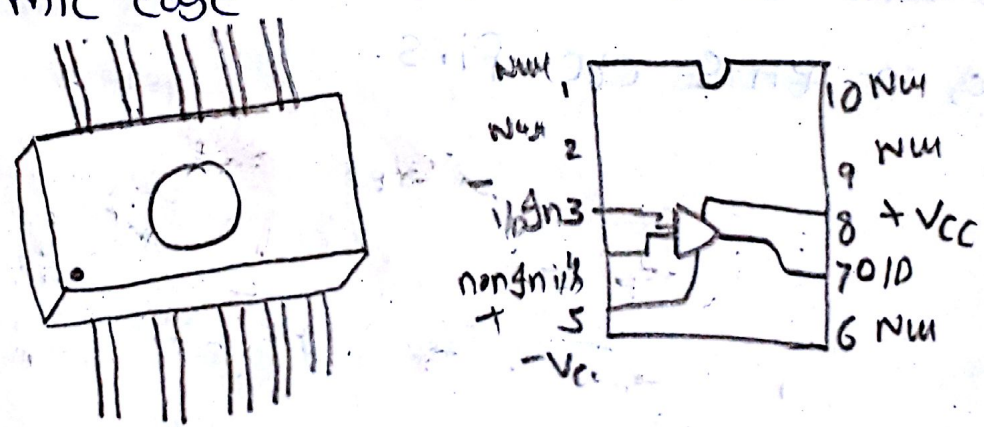
The 8 pin dual inline IC is also called as minimum dip plastic package.

It is the most using package because of easily mounted on the circuit board without holding the pins.



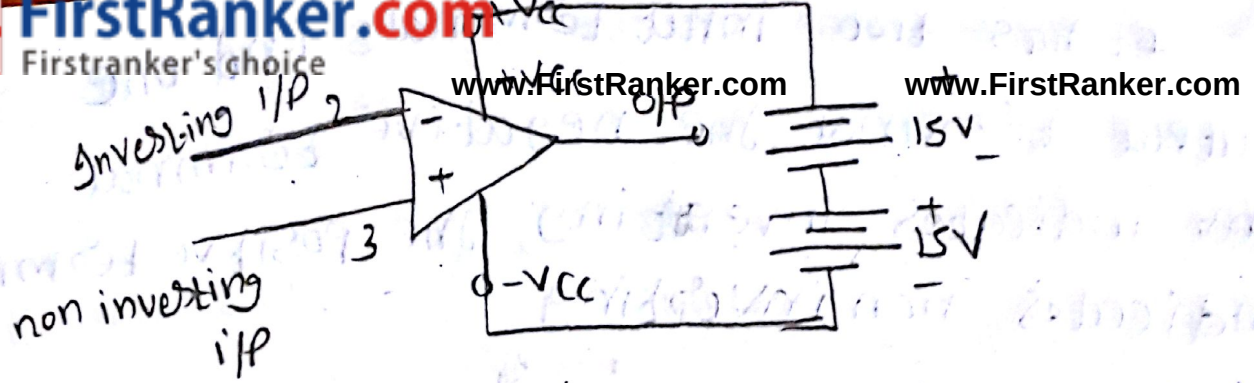
* Flat Package:

These available with pin no 8, 12, 14, 16 in this type the chip is enclosed in a rectangular ceramic case.



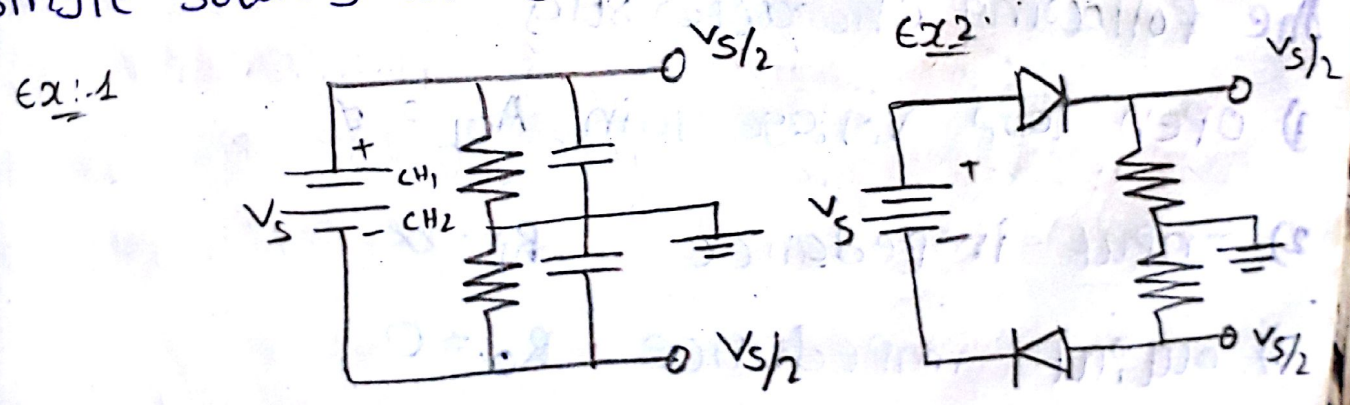
* Power supply connections:

The v^+ and v^- terminals are connected to two dc voltage sources. The v^+ pin is connected to the positive terminal of 1 source and the v^- pin is connected to the negative terminal of other source as shown in below.

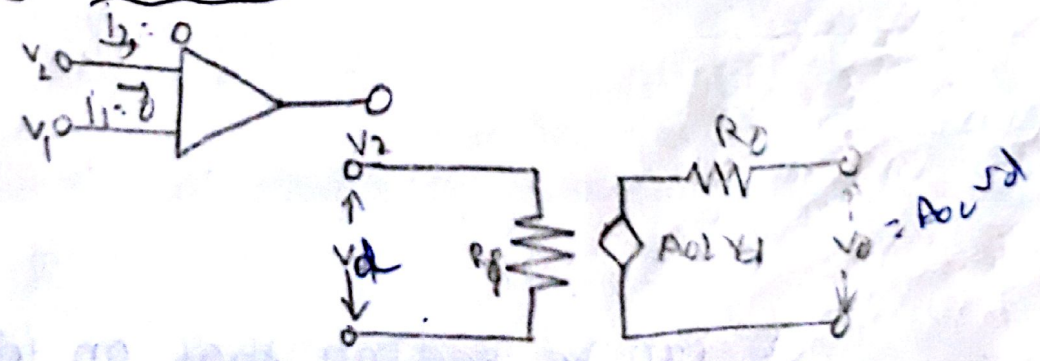


where the two sources are $15V$ batteries. These are typical values but in general the power supply voltages may range from about $\pm 5V$ to $\pm 20V$ range. The common terminal of the V^+ and V^- sources is connected to the grounded.

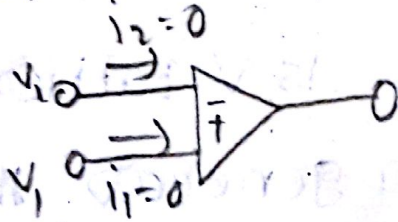
Instead of using two sources we use single source along with external components.



* Ideal OP - Amplifier :-



It has two input terminals and one output terminal. The negative terminal indicates inverting, the positive terminal indicates non-inverting.

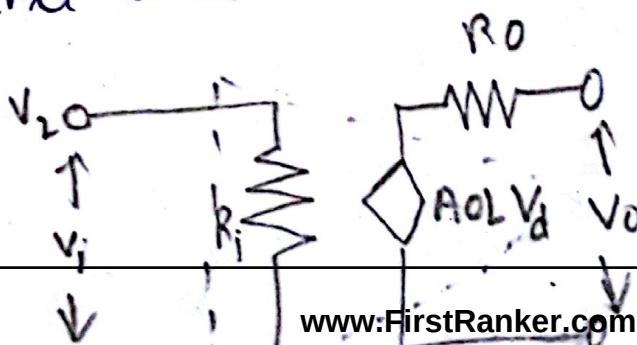


If $V_1 = 0$ the output V_0 is 180° out of phase with input signal V_2 .

When $V_2 = 0$ output V_0 will be in phase with the input signal applied at V_1 .

This op-amp is set to be ideal if it has the following characteristics.

- 1) open loop voltage gain $A_{OL} = \infty$
- 2) input impedance $R_i = \infty$
- 3) output impedance $R_o = 0$
- 4) Band width $= \infty$



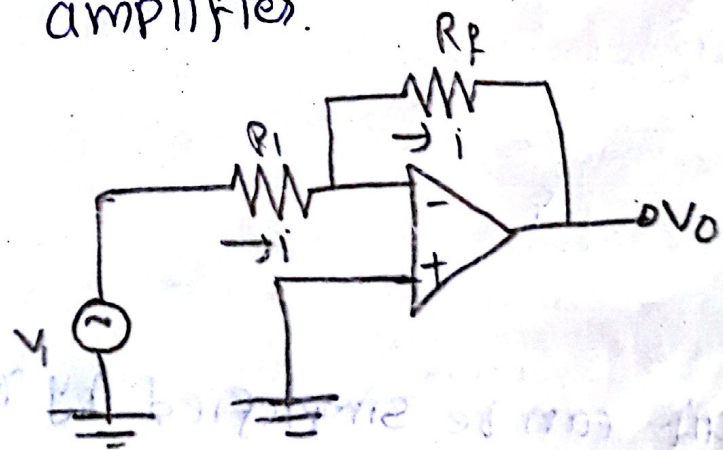
because of infinite input impedance.
 since gain is ∞ infinite the voltage between inverting & non inverting terminal that is differential voltage $V_d = V_1 - V_2$ is essentially zero.

The output voltage V_o is independent of the current drawn from the output as $R_o = 0$

* Inverting op-amp :-

As the name such as the output of such an amplifier is inverted as compared to the input signal.

An amplifier which provides a phase shift of 180° input and output is called inverting amplifier.



Assume an ideal op-amp that current i through R_1 is $i = \frac{V_i}{R_1}$

op-amp draws no current all the current flowing through R_1 must flow

through R_f , the out-put voltage

$$V_o = -i R_f$$

$$V_o = -\frac{V_i R_f}{R_i}$$

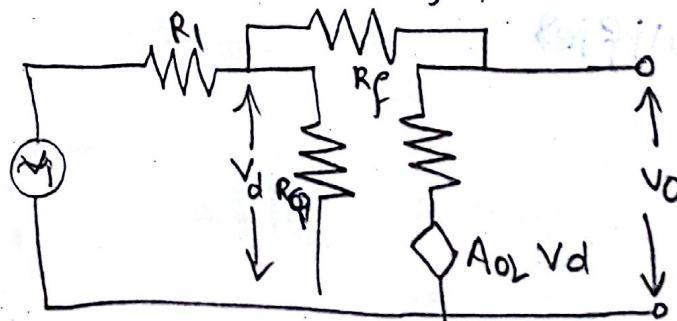
$$A_{CL} = \frac{V_o}{V_i} = -\frac{R_f}{R_i}$$

$\frac{R_f}{R_i}$ is the gain of the amplifier

while negative sign indicates that the polarity of o/p is opposite to that of input.

* Practical op-amp:-

The equivalent ckt of practical inverting amplifier is shown in fig (a).



The circuit can be simplified by replacing the signal source V_i , R_1 and R_f by thevenin equivalent by shown in fig (b)

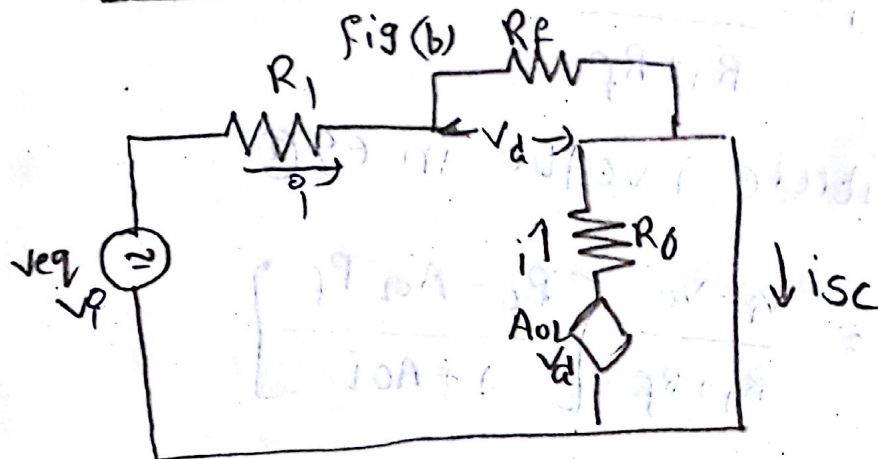
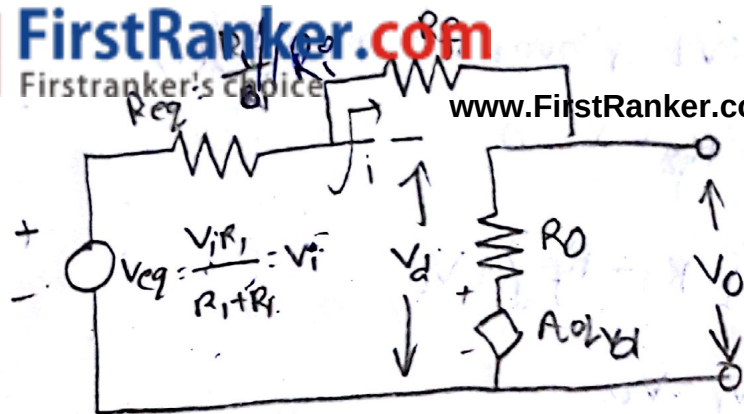


Fig (c)

The input impedance R_i of an op-amp is usually much greater than R_1 . so we may assume $v_{eq} = v_i$ and $R_{eq} = R_1$. From the o/p loop of figure (b)

$$V_o = iR_0 + A_{ol} V_d \quad \text{--- (1)}$$

from fig (c)

$$V_d + iR_f + V_o = 0$$

$$V_d = -iR_f - V_o$$

substitute V_d value in eq (1)

$$\begin{aligned} V_o &= iR_0 + A_{ol}(-iR_f - V_o) \\ &= iR_0 - A_{ol}iR_f - A_{ol}V_o \end{aligned}$$

$$V_o(1 + A_{ol}) = i[R_0 - A_{ol}R_f]$$

$$-V_i + iR_i + iR_f + V_o = 0$$

$$V_i = i[R_i + R_f] + V_o$$

$$i = \frac{V_i - V_o}{R_i + R_f}$$

substitute i value in eq ②

$$V_o = \frac{V_i - V_o}{R_i + R_f} \left[\frac{R_o - A_{OL} R_f}{1 + A_{OL}} \right]$$

$$= \frac{(V_i - V_o)(1 + A_{OL})(R_i + R_f)(R_o - A_{OL} R_f)}{(R_i + R_f) \times (1 + A_{OL})}$$

$$= \frac{V_i + V_i A_{OL} - V_o - V_o A_{OL}}{R_i + R_i A_{OL} + R_f + R_f A_{OL}}$$

$$= \frac{V_i R_o - V_i A_{OL} R_f - V_o R_o + V_o A_{OL} R_f}{R_i + R_i A_{OL} + R_f + R_f A_{OL}}$$

$$= \frac{V_i (R_o - A_{OL} R_f) + V_o (A_{OL} R_f - R_o)}{R_i + R_i A_{OL} + R_f + R_f A_{OL}}$$

$$V_o (R_i + R_i A_{OL} + R_f + R_f A_{OL}) = V_i (R_o - A_{OL} R_f) + V_o (A_{OL} R_f - R_o)$$

$$V_o R_i + V_o R_i A_{OL} + V_o R_f + V_o R_f A_{OL} = V_i (R_o - A_{OL} R_f) + V_o (A_{OL} R_f - R_o)$$

$$V_o (R_i + R_f) + V_o A_{OL} (R_i + R_f) = V_i (R_o - A_{OL} R_f) + V_o (A_{OL} R_f - R_o)$$

$$V_o R_i [1 + A_{OL}] + V_o R_f = V_i (R_o - A_{OL} R_f) - V_o R_o$$

$$V_o R_i [1 + A_{OL}] + V_o (R_f + R_o) = V_i (R_o - R_f A_{OL})$$

$$V_o [R_i [1 + A_{OL}] + (R_f + R_o)] = V_i [R_o - R_f A_{OL}]$$

$$\frac{V_o}{V_i} = \frac{R_o - R_f A_{OL}}{R_i(1 + A_{OL}) + R_f + R_o}$$

$$A_{OL} \gg 1$$

$$R_i A_{OL} \gg R_i + R_f$$

neglected R_o .

$$\frac{V_o}{V_i} = \frac{R_o - R_f A_{OL}}{R_i + R_i A_{OL} + R_f + R_o}$$

$$\frac{V_o}{V_i} = \frac{R_o - R_f A_{OL}}{R_i A_{OL}} = -\frac{R_f}{R_i}$$

* characteristics of op-amp:

1) DC characteristics:

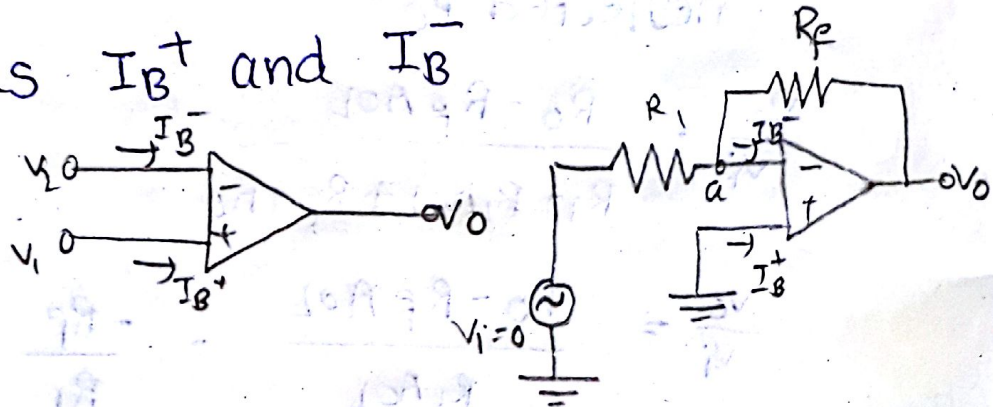
2) AC characteristics.

* DC characteristics:

The non ideal dc characteristics are

- 1) I/P bias current.
- 2) I/P offset current.
- 3) I/P offset voltage.
- 4) Thermal drift.

Ideally there is no input drawn from source to the op-amp but in practical the base currents are entering into inverting and non inverting terminals are shown as I_B^+ and I_B^-



The average of currents entering into inverting and non inverting terminals of an op-amp is called input bias current.

$$I_B = \frac{I_B^+ + I_B^-}{2}$$

If $v_i = 0$, $v_o = 0$ so apply KVL at output

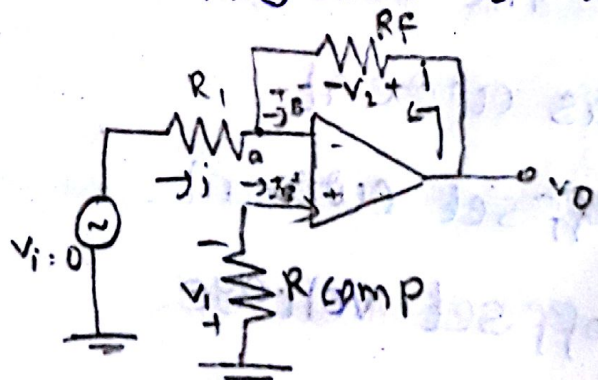
loop

$$-v_o + v_2 - v_1 = 0$$

$$v_o = v_2 - v_1$$

$$\Rightarrow v_1 - v_2 = 0$$

$$\Rightarrow v_1 = v_2$$



$$v_2 = I_B R_f$$

voltage at non inverting terminal

$V_i = 0$ we get

$$I_1 = \frac{V_1}{R_1}, \quad I_2 = \frac{V_2}{R_F}$$

$$I_B^- = I_1 + I_2$$

$$= \frac{V_1}{R_1} + \frac{V_2}{R_F}$$

$$[V_1 = V_2]$$

$$= V_1 \left[\frac{1}{R_1} + \frac{1}{R_F} \right]$$

$$= V_1 \left[\frac{R_1 + R_F}{R_1 R_F} \right]$$

$$I_B^+ = \frac{V_1}{R_{comp}}$$

$$\text{Assume } I_B^+ = I_B^-$$

$$\frac{V_1}{R_{comp}} = V_1 \left[\frac{R_1 + R_F}{R_1 R_F} \right]$$

$$\frac{1}{R_{comp}} = \frac{R_1 + R_F}{R_1 R_F}$$

$$R_{comp} = \frac{R_1 R_F}{R_1 + R_F}$$

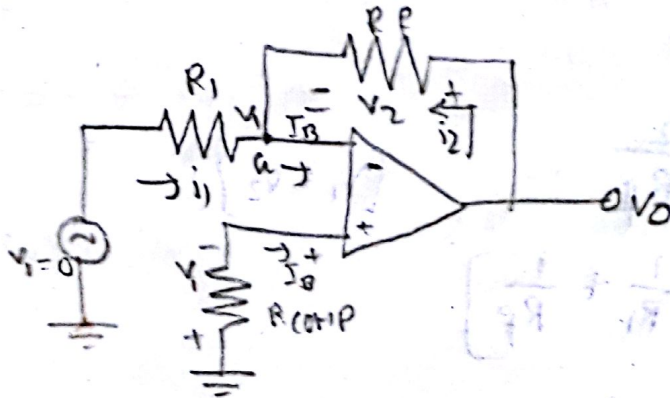
$$R_{comp} = R_1 || R_F$$

Input offset current:

Bias current compensation will work

input transistors can not be identical they will always $\vee$ some small difference between I_B^+ and I_B^- and it can written as

$$I_{os} = |I_B^+ - I_B^-|$$



$$I_B = I_1 + I_2$$

$$I_2 = I_B^- - I_1 \quad \text{--- ①}$$

$$I_1 = \frac{V_1}{R_1} \quad \text{--- ②}$$

$$V_1 = I_B^+ R_{comp} \quad \text{--- ③}$$

substitute v_1 value in eq ②

$$I_1 = \frac{I_B^+ R_{comp}}{R_1}$$

substitute I_1 value in eq ①

$$I_2 = I_B^- - \frac{I_B^+ R_{comp}}{R_1}$$

$$\begin{aligned} V_o &= V_2 - V_1 \\ &= I_B^- R_{comp} - I_B^+ R_{comp} \\ &= R_{comp} (I_B^- - I_B^+) \end{aligned}$$

$$V_o = R_F \left[I_B^- - \frac{I_B^+ R_{comp}}{R_1} \right] - I_B^+ R_{comp}$$

$$R_{comp} = R_1 // R_F$$

$$V_o = R_F \left[I_B^- - \frac{I_B^+ \frac{R_1 R_F}{R_1 + R_F}}{R_1} \right] - I_B^+ \left[\frac{R_1 R_F}{R_1 + R_F} \right]$$

$$= R_F \left[I_B^- - I_B^+ \frac{R_1 R_F}{R_1 + R_F} - I_B^+ \left[\frac{R_1}{R_1 + R_F} \right] \right]$$

$$= R_F \left[I_B^- - I_B^+ \left[\frac{R_F}{R_1 + R_F} + \frac{R_1}{R_1 + R_F} \right] \right]$$

$$= R_F \left[I_B^- - I_B^+ \left[\frac{R_F + R_1}{R_1 + R_F} \right] \right]$$

$$= R_F [I_B^- - I_B^+]$$

$$\frac{R_F R_1}{(R_1 + R_F)}$$

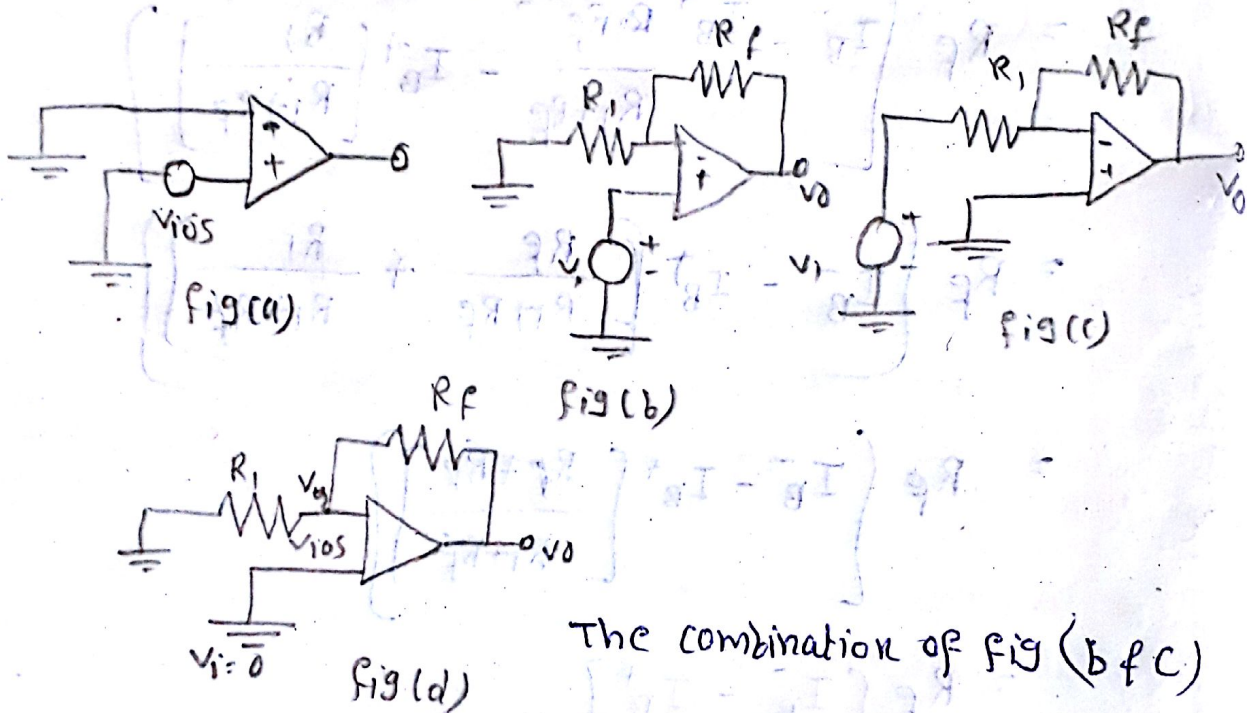
$$V_o = R_F |I_{os}|$$

* Input offset voltage:-

In spite using above compensating technique, is ^{found} the output voltage may still ^{not} be zero with zero input voltage. This is due to unavoidable imbalances inside the op-amp and one may have to

applying a small voltage at the input terminal to make output voltage zero. This voltage is called offset voltage.

— This is the voltage required to be applied at the input for making output voltage to "Zero" volts



The combination of fig (b & c)

V_i is set to zero. The circuits of fig b & c which is same as fig (d). The voltage V_2 at the non-inverting terminal is given by

$$V_2 = \frac{R_1}{R_1 + R_f} \cdot V_o$$

$$V_o = \frac{R_1 + R_f}{R_1} V_2$$

$$V_o = (V_i - V_2) \quad V_i = 0$$

$$V_0 = 10 - V_2$$

$$V_0 = \left| \frac{R_1 + R_2}{R_1} \right| V_2$$

* Thermal drift:

Bias current, off set current and off set voltage changes with temperature. A circuit may not remain with at 25°C when the temperature rises from 25°C to 35°C . This is called thermal drift. The units of Thermal drift are $\text{nano amp} / ^\circ\text{C}$.

* AC characteristics

* Frequency compensation:

In order to find large band width and less closed loop gain we are using some compensation techniques they are

- 1) External frequency compensation.
- 2) Internal frequency compensation.

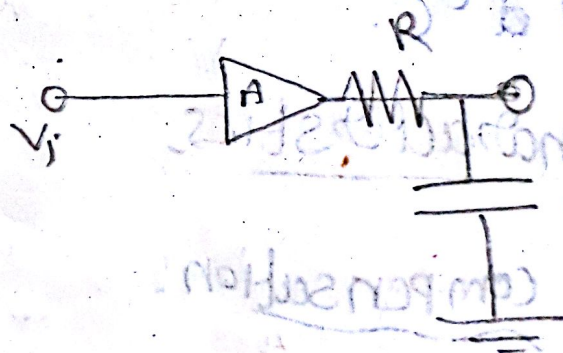
* External frequency compensation:

1) Dominant Pole compensation

2) Pole zero compensation

* Dominant Pole compensation:-

Introduce a dominant pole by adding RC network in series with OP-amp (or) by connecting capacitor C from a suitable high resistance point to ground. The compensated transfer function A' becomes



$$A' = A \cdot \frac{V_o}{V_i}$$

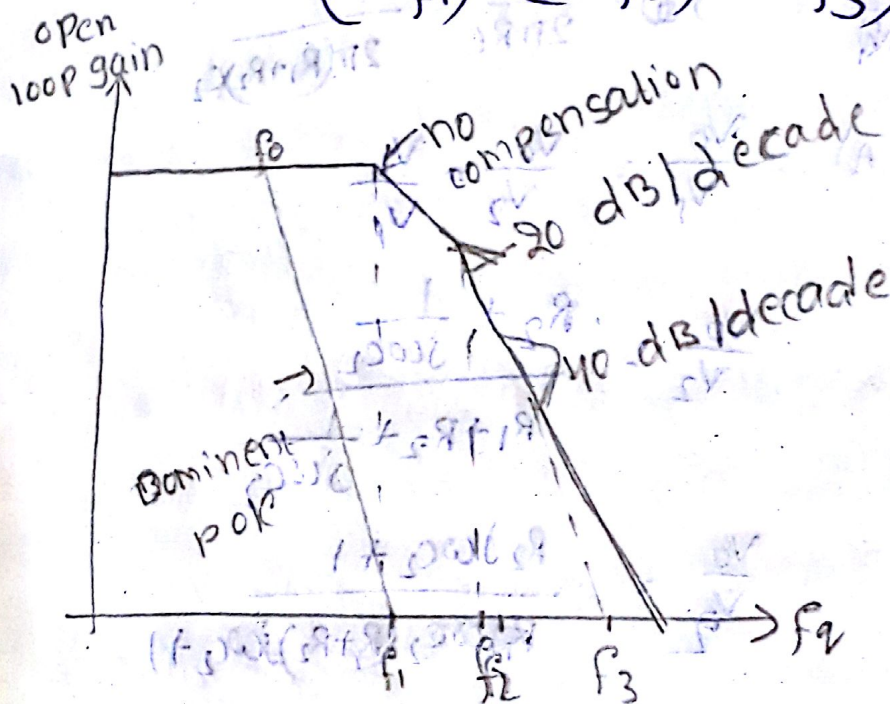
$$\frac{V_o}{V_i} = \frac{1}{R + \frac{1}{j\omega C}}$$

$$\frac{V_o}{V_i} = \frac{1}{j\omega RC + 1}$$

$$\frac{V_o}{V_i} = \frac{1}{j2\pi f RC + 1} \quad (\omega = 2\pi f)$$

consider an open loop with three break frequencies

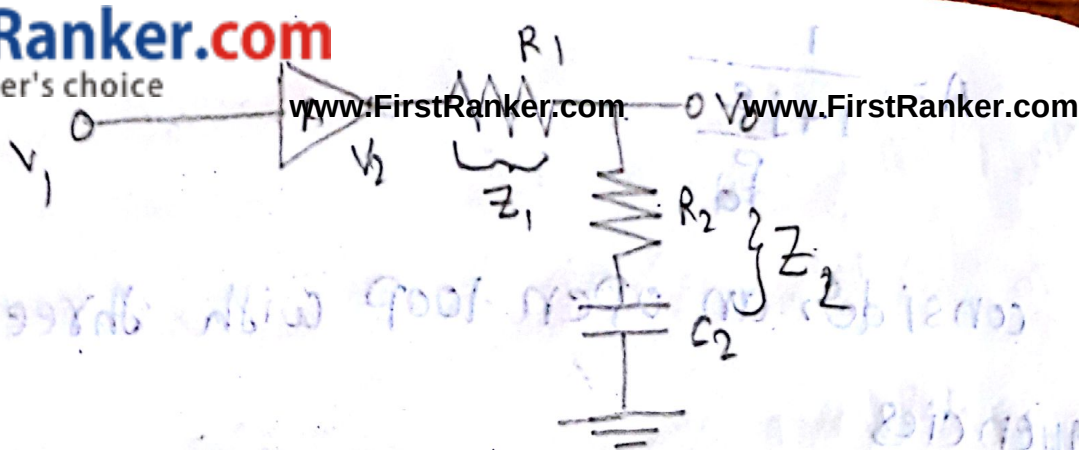
$$A_1 = \frac{A_{OL}}{\left(1 + j\frac{f}{f_1}\right) \left(1 + j\frac{f}{f_2}\right) \left(1 + \frac{f}{f_3}\right)}$$



The frequency can be found graphically by having A_1 pass through 0 dB at the frequency f_1 with a slope -20 dB/decade

* Pole Zero Compensation

Here the uncompensated transfer function A is altered by adding both pole and zero. The zero should be at high frequency than pole the transfer function of the compensating network alone is



$$V_0 = \frac{Z_2}{Z_1 + Z_2} V_1$$

$$f_0 = \frac{1}{2\pi RC} = \frac{1}{2\pi(R_1 + R_2)C_2}$$

$$A' = \frac{V_0}{V_1} = \frac{V_0}{V_2} \cdot \frac{V_2}{V_1}$$

$$\frac{V_0}{V_2} = \frac{R_2 + \frac{1}{j\omega C_2}}{R_1 + R_2 + \frac{1}{j\omega C_2}}$$

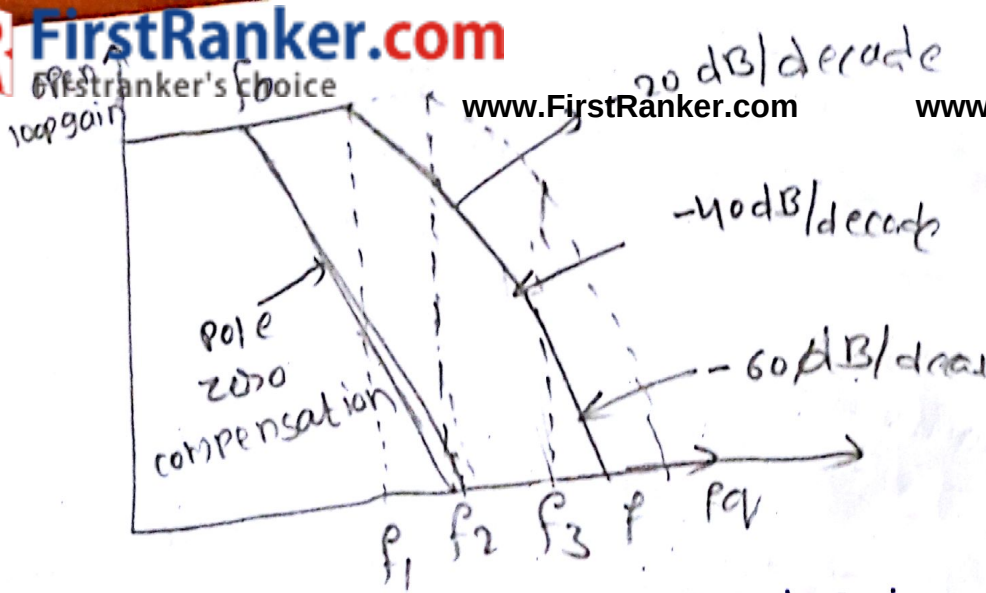
$$\frac{V_0}{V_2} = \frac{R_2 j\omega C_2 + 1}{R_2(R_1 + R_2)j\omega C_2 + 1}$$

$$\frac{V_0}{V_2} = \frac{1 + j2\pi f R_2 C_2}{(R_1 + R_2)j2\pi f C_2 + 1}$$

$$\frac{V_2}{V_1} = A = \frac{1 + jf/f_0}{1 + jf/f_0}$$

$$\frac{V_0}{V_1} = \frac{V_0}{V_2} \times \frac{V_2}{V_1}$$

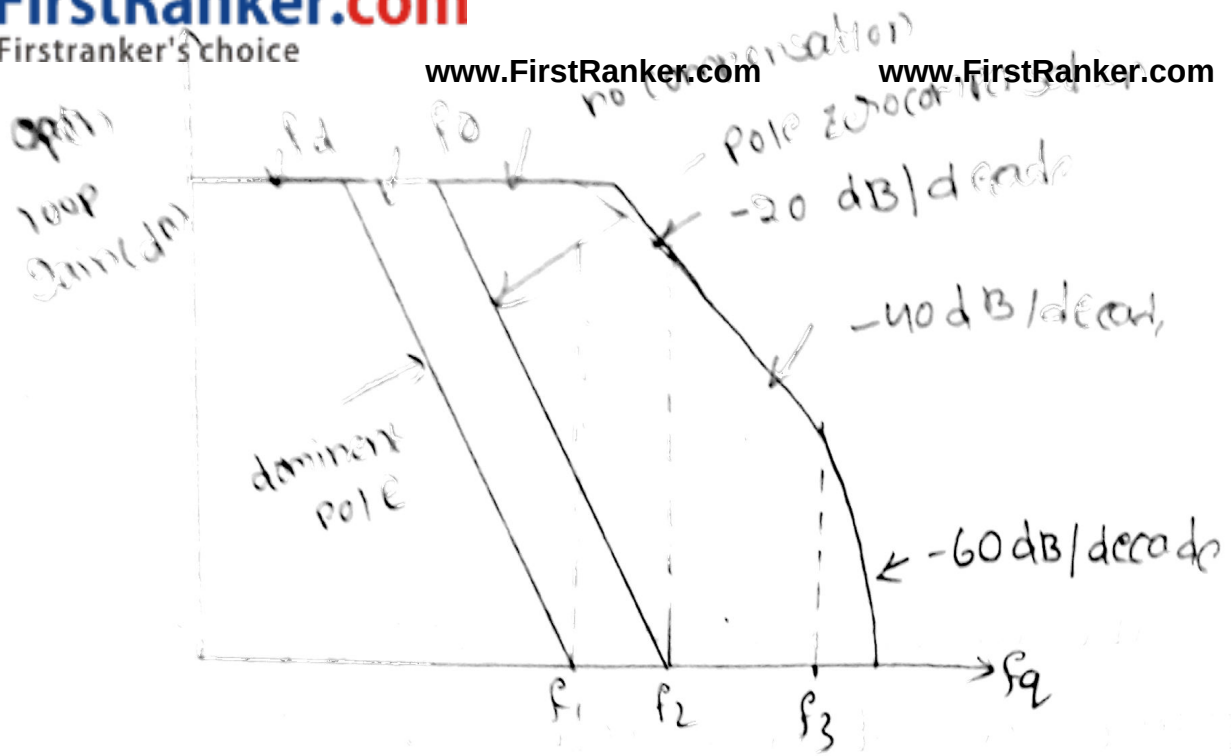
$$= A \cdot \frac{1 + j(f/f_0)}{1 + j(f/f_0)}$$



The compensating n/w is design to produce zero at first corner frequency f_1 of uncompensated Transfer function A . These zero will cancel the effect of pole at f_1 , the pole of the compensating n/w f_0 is selected. The frequency can be found graphically. A passes through 0 dB at frequency f_2 with a slope of -20 dB for decayed.

consider an open loop with 3 break frequencies

$$\frac{V_o}{V_i} = A \cdot \frac{1 + j(f/f_d)}{[1 + j(f/f_1)] [1 + j(f/f_2)] [1 + j(f/f_3)]}$$



- * A comparison of dominant pole and pole zero compensation is shown in above figure. The dominant pole is selected so that the compensated transfer function goes through 0 dB at first corner frequency f_1 . In pole zero compensation the zero is ^{at} ~~at~~ ^{chosen} ~~introduction~~ at f_1 and pole is selected so that the modified transfer function goes through 0 dB at the ~~freq~~ f_2 .

* Internal frequency compensation:

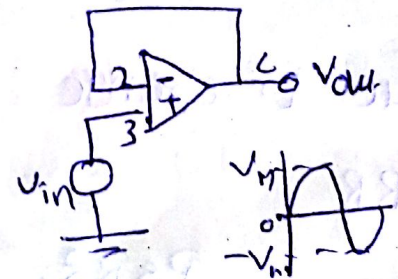
These are used in instrumentation ckt op-amps are used to amplify low input signal. It does not require high frequency response in that we are using internal

For high amplitude signals
measuring slew rate. If i/p signal having
magnitude the ideal response measured with
rise time

Rise time is defined as time taken
to rise from 10% to 90% of its maximum value.

slew rate is defined as maximum rate
of change of output voltage with time. It is
specified in volt / μ sec.

$$\text{slew rate} = \frac{dV_o}{dt}$$



voltage follower

consider a voltage follower
ckt shown in figure the input is large amplitude,
high frequency sine wave

$$V_o = V_m \sin \omega t$$

The rate of change of o/p is given by

$$\frac{dV_o}{dt} = V_m \omega \cos \omega t$$

The maximum rate of change of o/p occurs
when $\cos \omega t = 1$

$$\text{slew rate} = \frac{dV_o}{dt} = \omega V_m$$

$$S.R. = \frac{V_m 2\pi f}{10^6} \text{ V/MS}$$

$$f_{max} = \frac{S.R \times 10^6}{V_m 2\pi}$$

For example 1V/μsec slew rate means that
o/p rises or falls by 1V in 1 micro sec.

*PSRR (Power supply Rejection Ratio):

The change in op-amp input voltage
due to change in supply these called ΔV_i in
PSRR.

$$PSRR = \frac{\Delta V_i}{\Delta V_{cc}}$$

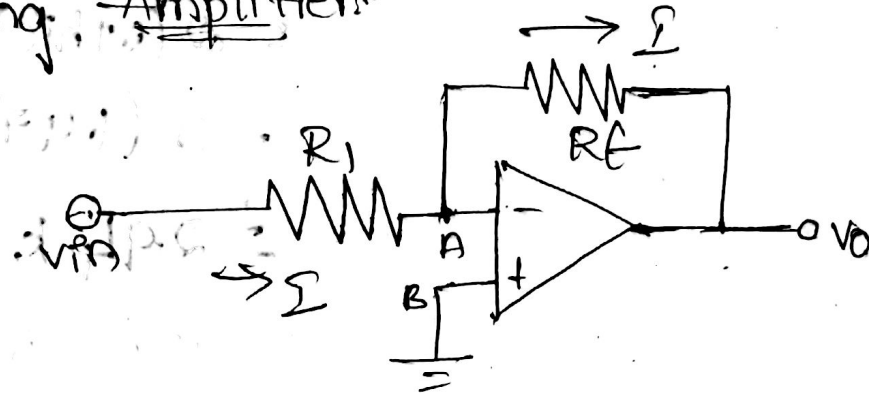
*CMRR (Common mode Rejection Ratio):

It is defined as the ratio of differential
voltage gain to common mode voltage gain

$$CMRR = \frac{A_d}{A_{cm}}$$

3. Linear and Non Linear Applications of op-amps,

Inverting Amplifier:-



Analysis

$$\frac{V_{in} - V_A}{R_1} = \frac{V_A - V_o}{R_f} = I$$

but $V_A = 0$.

$$V_o = -I R_f$$

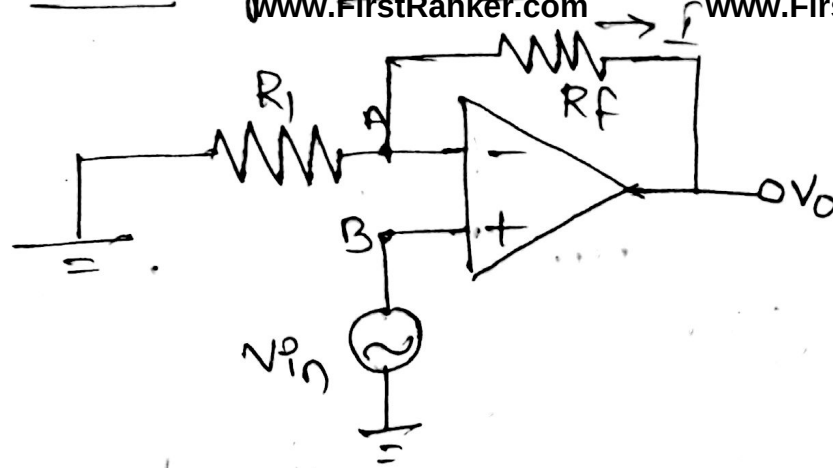
$$\frac{V_{in}}{R_1} = -\frac{V_o}{R_f}$$

$$-\frac{V_{in}}{R_1} = \frac{V_o}{R_f}$$

$$V_o = -\frac{R_f}{R_1} V_{in}$$

* If $R_1 = R_f$ Then $V_o = -V_{in}$. So it is called phase inverter ckt.

* If $R_f = n R_1$ Then $V_o = -n V_{in}$. It is called square changer.



$V_A = V_B = V_{in}$ (Due to the concepts of virtual ground)

$$\frac{0 - V_A}{R_1} = \frac{V_A - V_O}{R_f}$$

But $V_A = V_{in}$

$$-\frac{V_{in}}{R_1} = \frac{V_{in} - V_O}{R_f}$$

$$\frac{V_O}{R_f} = \frac{V_{in}}{R_f} + \frac{V_{in}}{R_1}$$

$$V_O = V_{in} + \frac{R_f}{R_1} V_{in}$$

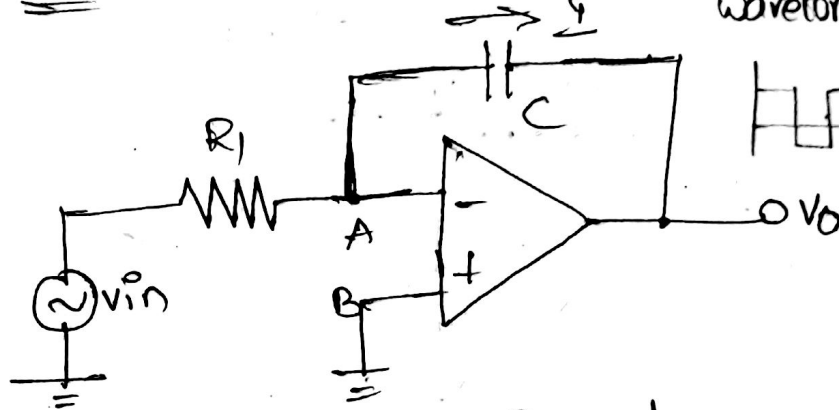
$$= V_{in} \left(1 + \frac{R_f}{R_1} \right)$$

$$\frac{V_O}{V_{in}} = \left(1 + \frac{R_f}{R_1} \right)$$

$\therefore$ the closed loop gain is always greater than one.

* There is no phase inversion (because all are +ve values)

Integrator:-



$V_A = V_B = 0$ $\therefore$ virtual ground.

$$I = \frac{V_{in} - V_A}{R_i} = C_F \frac{dV_C}{dt} = C_F \frac{d}{dt} [V_A - V_O]$$

$$\frac{V_{in} - V_A}{R_i} = C_F \frac{d}{dt} (V_A - V_O)$$

$$\frac{V_{in}}{R_i} = C_F \frac{d}{dt} (-V_O)$$

$$C_F \frac{d}{dt} V_O = -\frac{V_{in}}{R_i}$$

$$V_O = -\frac{1}{R_i C_F} \int_0^t V_{in} dt$$

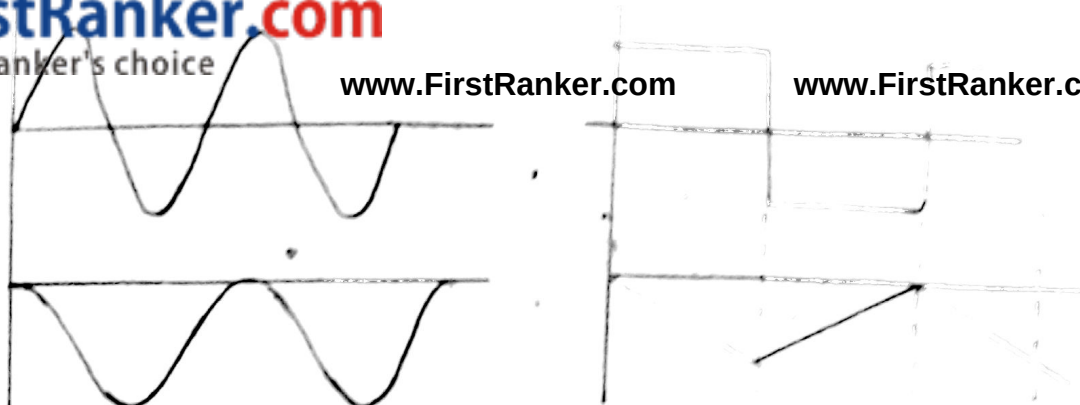
$$V_O \propto \frac{1}{R_i C_F} \text{ (time constant)}$$

$$V_O \propto \int V_{in}$$

* V_O is integral of V_{in}

* R_F is replaced by R_i

* V_O is negative integral of V_{in}

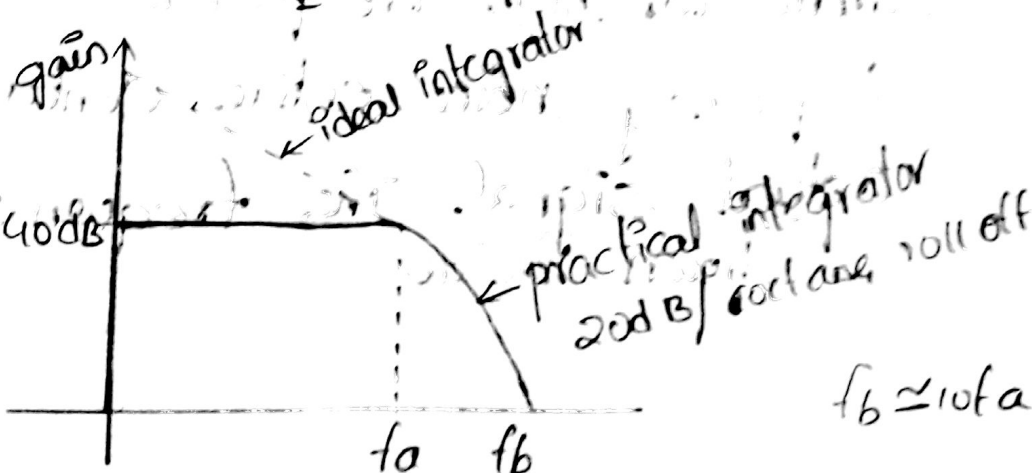
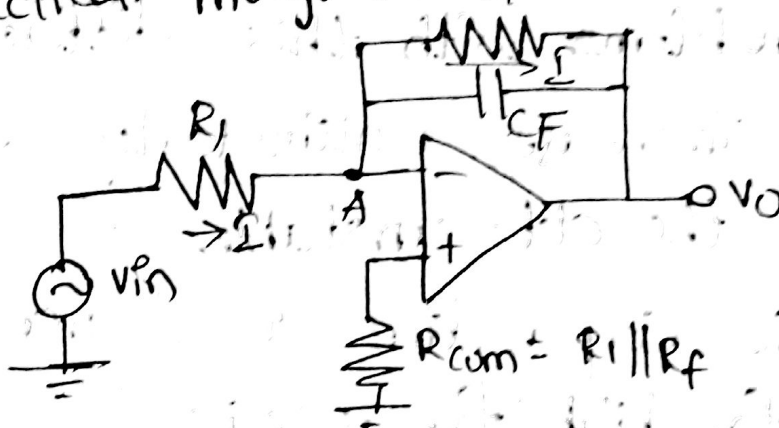


Why practical Integrator?

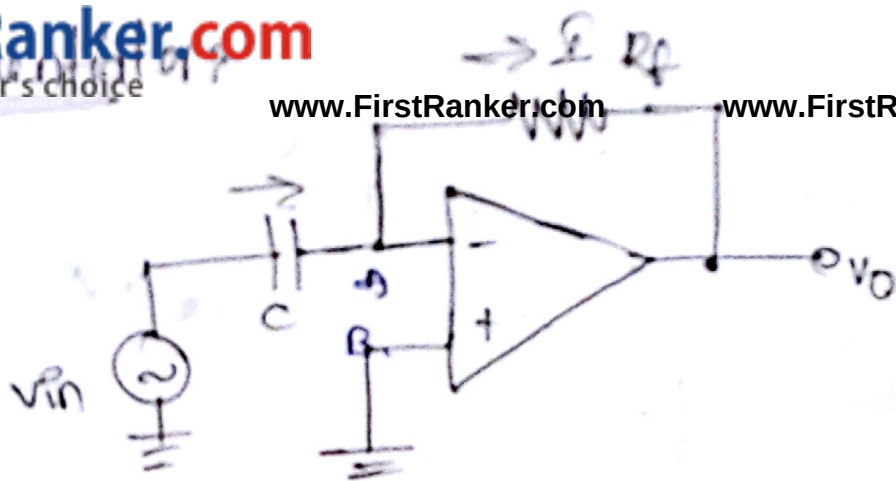
a) when $V_{in} = 0$; $\frac{1}{2\pi fC} = X_C$

when $f \rightarrow 0 \Rightarrow X_C \rightarrow \infty$

As capacitor is acting as emmitter ckt the integrator acts as open loop amplifier & produces errors in the o/p voltage To avoid practical integrator R_F is introduced



$$f_a = \frac{1}{2\pi R_i C_F} \quad f_b = \frac{1}{2\pi R_F C_F}$$



$$V_A = V_B = 0.$$

$$C \frac{d}{dt} (v_{in} - V_A) = \frac{V_A - V_O}{R_f}$$

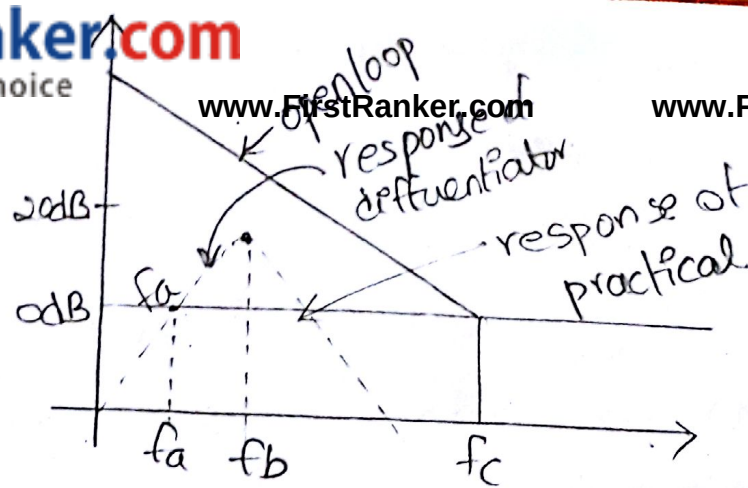
$$C \cdot \frac{d}{dt} v_{in} = -\frac{V_O}{R_f} \quad (\because V_A = 0)$$

$$V_O = -R_f \cdot C \cdot \frac{d}{dt} v_{in}$$

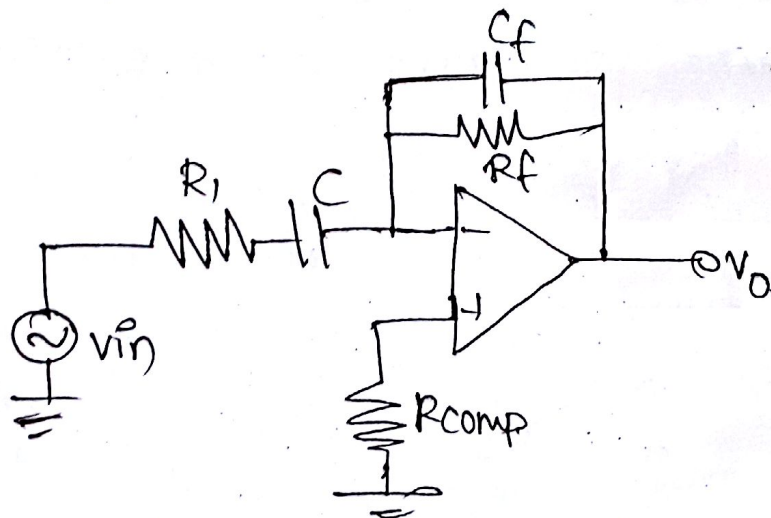
The problems with this differentiator are

1, gain increases unlimitedly which means the ckt unstable

2, As the Capacitive reactance is small for high frequencies the high frequency noise enters contaminates actual signal. The frequency response is shown below.



practical Differentiator:



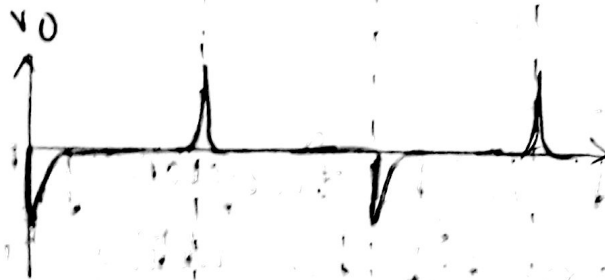
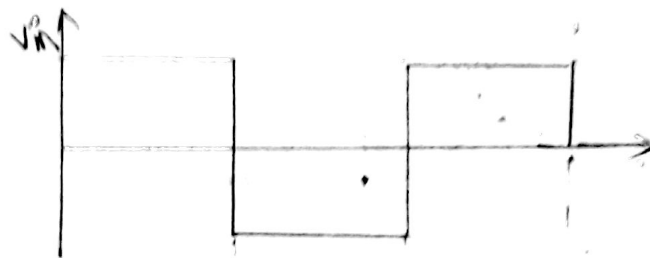
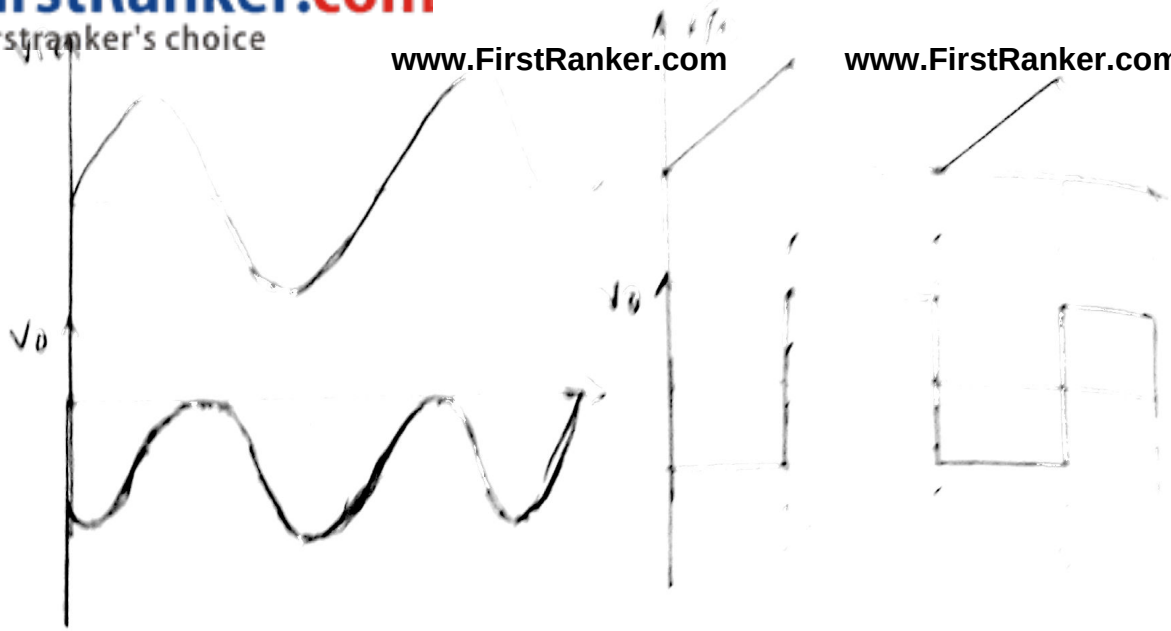
The stability and high frequency noise problems are corrected by adding R_i & C_f .

f_A = frequency at which gain is 0dB

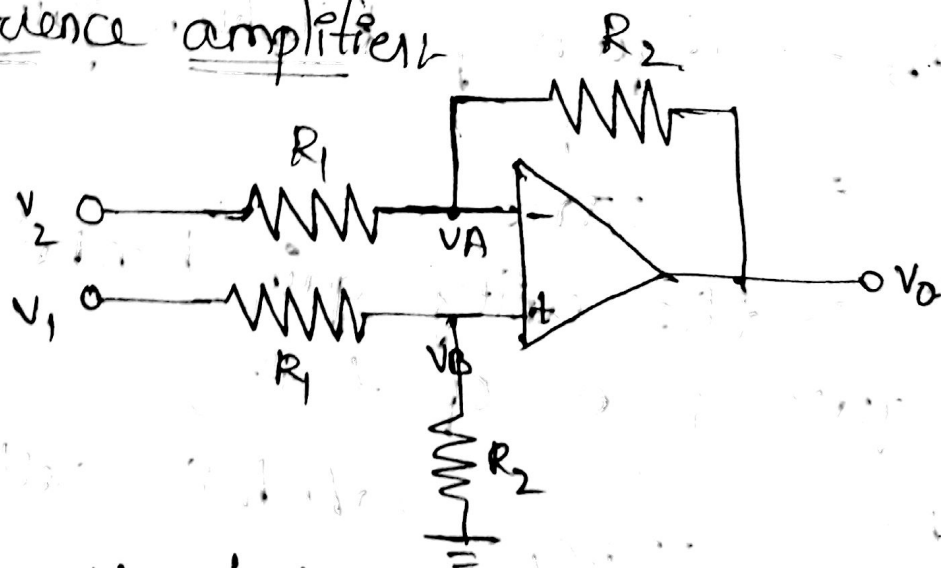
$$= \frac{1}{2\pi R_i C_f}$$

f_c is the unity gain bandwidth frequency of op-Amp.

$f_b = \frac{1}{2\pi R_i C_i}$ which is called gain-crossover frequency. The signal is properly differentiated $T \gg R_i R_f C_f$



Difference amplifier



A ckt which amplifies the difference of two ip signals is called Difference amplifier or Subtractor.

are V_A & V_B writing the nodal eqns. for node.

$$V_A = V_B = V_3$$

writing Nodal Equation at node-A.

$$\frac{V_3 - V_2}{R_1} + \frac{V_3 - V_0}{R_2} = 0 \rightarrow A$$

writing Nodal Eq'n at node B.

$$\frac{V_3 - V_1}{R_1} + \frac{V_3}{R_2} = 0 \rightarrow B$$

from Eq'n A

$$\frac{V_3}{R_1} - \frac{V_2}{R_1} + \frac{V_3}{R_2} - \frac{V_0}{R_2} = 0$$

$$V_3 \left[\frac{1}{R_1} + \frac{1}{R_2} \right] - \frac{V_2}{R_1} = \frac{V_0}{R_2} \quad \text{--- (C)}$$

from Eq'n B

$$\frac{V_3}{R_1} - \frac{V_1}{R_1} + \frac{V_3}{R_2} = 0$$

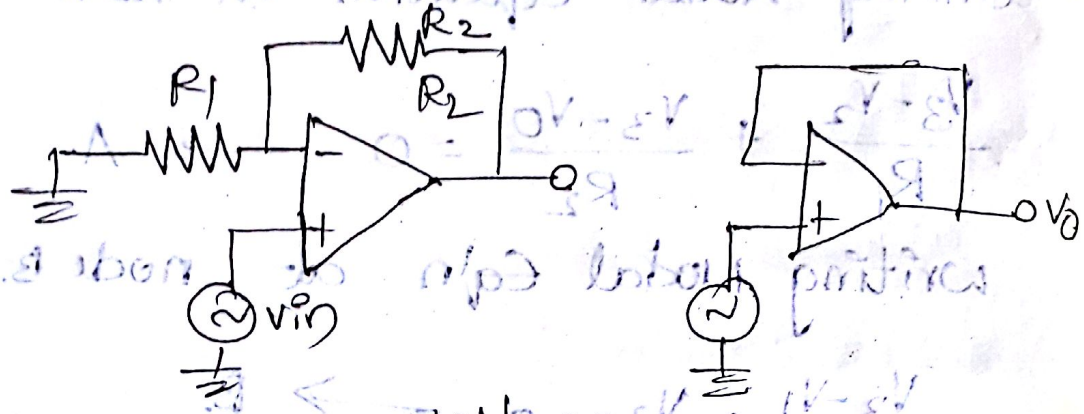
$$V_3 \left[\frac{1}{R_1} + \frac{1}{R_2} \right] - \frac{V_1}{R_1} = 0 \quad \text{--- (D)}$$

subtracting (D) from C

$$\frac{V_1}{R_1} - \frac{V_2}{R_1} = \frac{V_0}{R_2}$$

$$\therefore V_0 = \frac{R_2}{R_1} [V_1 - V_2]$$

It is very useful in detecting very small differences in signals. Since the gain is $\frac{R_2}{R_1}$ if $R_2 = 100R_1$ then a small difference $[V_1 - V_2]$ is amplified 100 times.

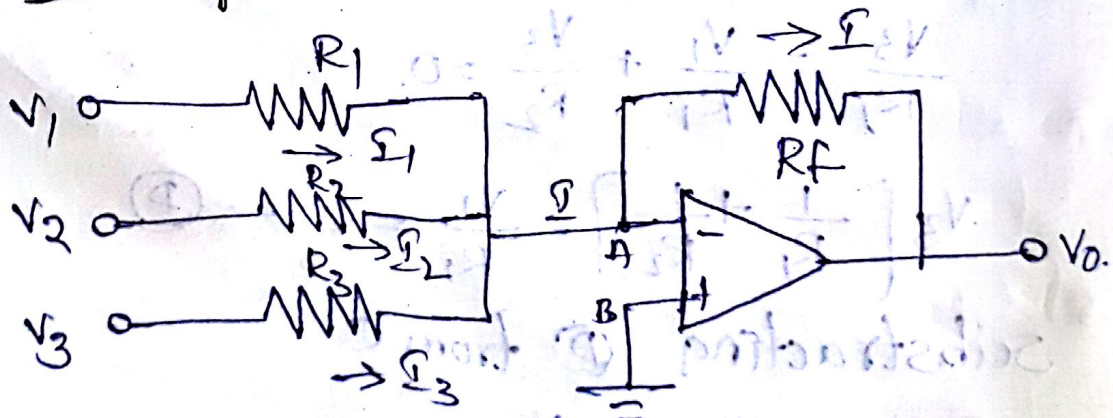


voltage follower

$$\frac{V_o}{V_i} = 1 + \frac{R_f}{R_1} \Rightarrow \frac{V_o}{V_i} \approx 1$$

$$R_1 = \infty, R_2 = 0 \Rightarrow V_o = V_i$$

Inverting Summer Amplifier



$V_A = V_B = 0$ based on virtual ground

$$I = I_1 + I_2 + I_3$$

$$= \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \quad (\because V_A = 0)$$

$$I = \frac{V_A - V_O}{R_f} = -\frac{V_O}{R_f} \quad (\because V_A = 0)$$

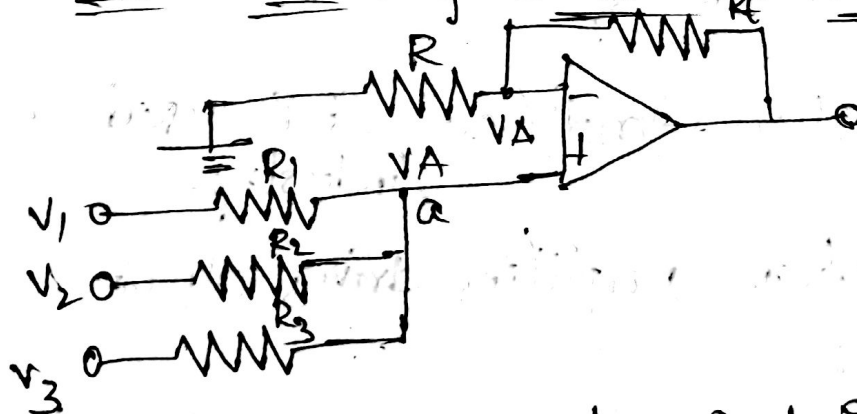
$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = \frac{V_O}{R_f}$$

$$V_O = R_f \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right)$$

If $R_f = R_1 = R_2 = R_3 = R$ Then

$$V_O = [V_1 + V_2 + V_3]$$

Non-Inverting Summer amplifier



Let voltage at -ve terminal is V_A then voltage at +ve terminal is V_A . The nodal equation at A^+ is written as

$$\frac{V_1 - V_A}{R_1} + \frac{V_2 - V_A}{R_2} + \frac{V_3 - V_A}{R_3} = 0$$

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = V_A \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \right)$$

$$V_A = \frac{V_1/R_1 + V_2/R_2 + V_3/R_3}{1/R_1 + 1/R_2 + 1/R_3}$$

$$V_0 = \left(1 + \frac{R_F}{R}\right) V_A$$

$$= \left(1 + \frac{R_F}{R}\right) \left[\frac{V_1/R_1 + V_2/R_2 + V_3/R_3}{1/R_1 + 1/R_2 + 1/R_3} \right]$$

Let $R_1 = R_2 = R_3 = R = \frac{R_F}{2}$ then

$$V_0 = \left(1 + \frac{R_F}{R_F/2}\right) \left[\frac{V_1/R + V_2/R + V_3/R}{1/R + 1/R + 1/R} \right]$$

$$= \frac{3(V_1 + V_2 + V_3)}{1/R}$$

$$\boxed{V_0 = V_1 + V_2 + V_3}$$

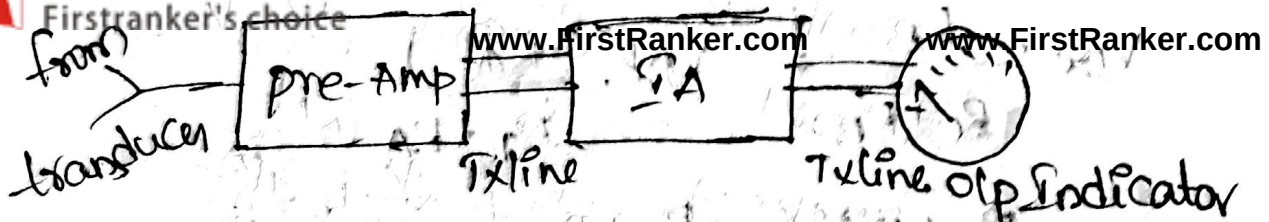
Instrumentation Amplifier: It is used in Industry.

* Instrumentation amplifier drives output of transducers

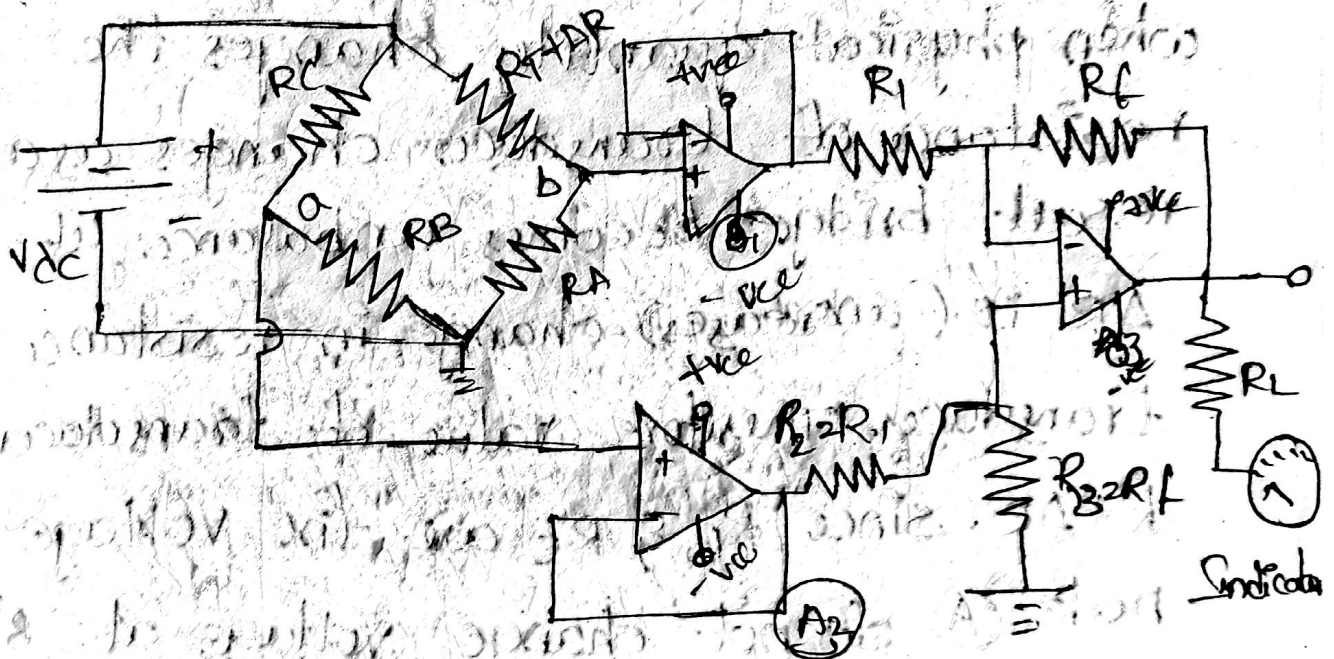
* Transducer converts one form of energy into another form

Ex Thermistor, photo conductive cell, strain gauge etc.,

* In Industry where direct measurement of physical quantity is not possible there



The instrumentation amplifier forms intermediate stage the indicator is suitable to calculate the measure physical quantity. The IA uses transducer bridge as shown below.



A_1 & A_2 are voltage followers which avoid the loading effect & A_3 is a normal amplifier. R_A , R_B , R_C and R_T are ratio arms of wheatstone bridge.

R_T = Resistance of transducer

R_f = Resistance of feedback path

when bridge is balanced

$$V_{out} = V_b$$

$$V_{DC} \frac{R_B}{R_C + R_B} = V_{DC} \frac{R_A}{R_T + R_A}$$

$$\frac{R_C + R_B}{R_B} = \frac{R_T + R_A}{R_A}$$

$$\frac{R_C}{R_B} + 1 = \frac{R_T}{R_A} + 1$$

$$\boxed{\frac{R_C}{R_B} = \frac{R_T}{R_A}}$$

when physical quantity changes the resistance of transducer changes as a result bridge becomes unbalance. Let ΔR is (increases) change in resistance of transducer. Therefore value of transducer is $R + \Delta R$. Since R_B & R_C are fix voltage at node A do not change voltage at B' changes.

$$V_a = V_{DC} \frac{R_B}{R_B + R_C}$$

$$V_b = V_{DC} \left[\frac{R_A}{R_A + R_T + \Delta R} \right]$$

$$V_{ab} = V_a - V_b$$

$$= V_{DC} \left[\frac{R_B}{R_B + R_C} - \frac{R_A}{R_A + R_T + \Delta R} \right]$$

$$\text{Let } R_A = R_B = R_C = R_D = R$$

$$V_{ab} = \left[\frac{R}{2R} - \frac{R}{2R + \Delta R} \right] V_{dc}$$

$$= \left[\frac{R(2R + \Delta R) - R \cdot 2R}{2R(2R + \Delta R)} \right] V_{dc}$$

$$= V_{dc} \left[\frac{2R + (\Delta R)R - 2R}{2R(2R + \Delta R)} \right] = \frac{R \cdot \Delta R \cdot V_{dc}}{2R(2R + \Delta R)}$$

$$= \frac{\Delta R V_{dc}}{2(2R + \Delta R)}$$

$$= V_{dc} \frac{\Delta R}{4R} \quad (\because R \gg \Delta R)$$

V_{ab} is applied to instrumentation amplifier which is combination of amplifiers A_1 & A_2 & A_3 .

A_1, A_2 are voltage followers and their main function is to eliminate loading effect of the bridge network. The gain of amplifier $A_3 = -\frac{R_f}{R_i}$

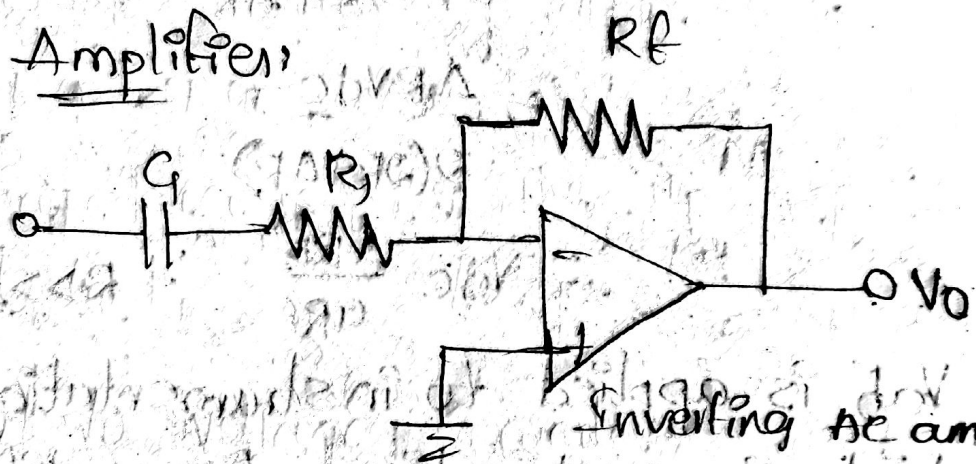
$$\text{Therefore } V_o = V_{ab} \cdot \frac{-R_f}{R_i}$$

$$= \left(-\frac{R_f}{R_i} \right) V_{dc} \cdot \frac{\Delta R}{4R}$$

$V_o \propto \Delta R$ if all other are constants.

Thus the o/p voltage is proportional to change in resistance of transducer & these change is a measure of physical quantity. The o/p drives the Integrating meter we can be calculated directly in terms of units of physical quantity being measured.

AC Amplifier

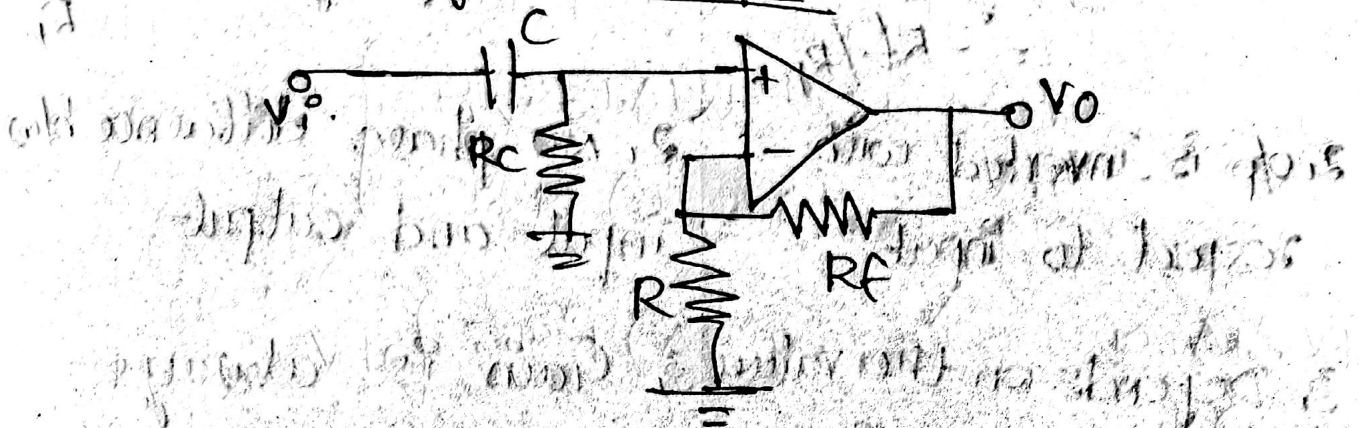


Inverting and non-inverting amplifiers respond to both AC & DC signals if one wants to consider only AC response then DC is locked by input capacitor.

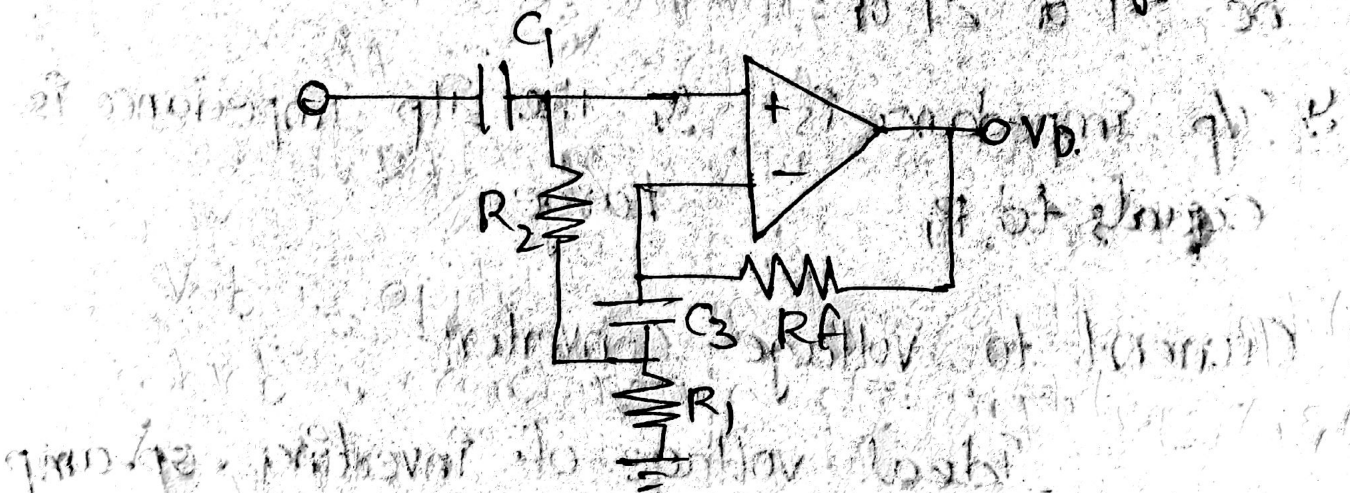
Inverting AC amplifier, If capacitor blocks dc component of input together with R_1 which sets low (or) 3dB frequency of amplifier and V_o is given by

$$V_o = -I \cdot R_f = \frac{-V_i}{R_1} \cdot R_f = -\frac{R_f}{R_1} V_i$$

NON-Inverting Ac amplifier



High ϕ impedance non-inverting amplifier



Here R_2 is added to provide V_c return path however, it reduces input resistance of amplifier and input resistance is equal to R_2 only. This effect can be reduced by adding capacitor C_3 . C_3 is large enough to act as short-circuit to AC signals and circuit will have difference.

Inverting Amplifier

1. voltage gain = $-R_f/R_i$

2. op is Inverted with respect to input

3. Depends on the value of R_i & R_f gain can be >1 or <1 or $=1$

4. I/p Impedance is equals to R_i

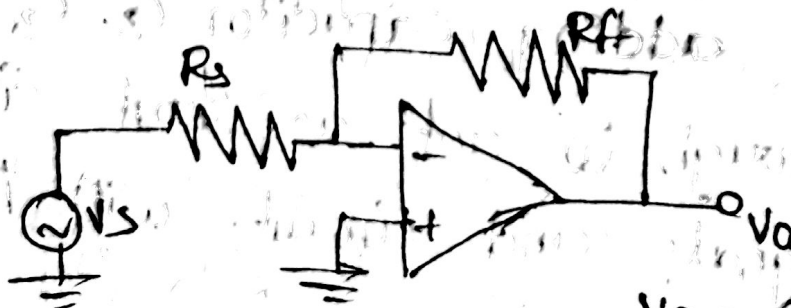
Current to voltage Converter

Ideal voltage of inverting op-amp

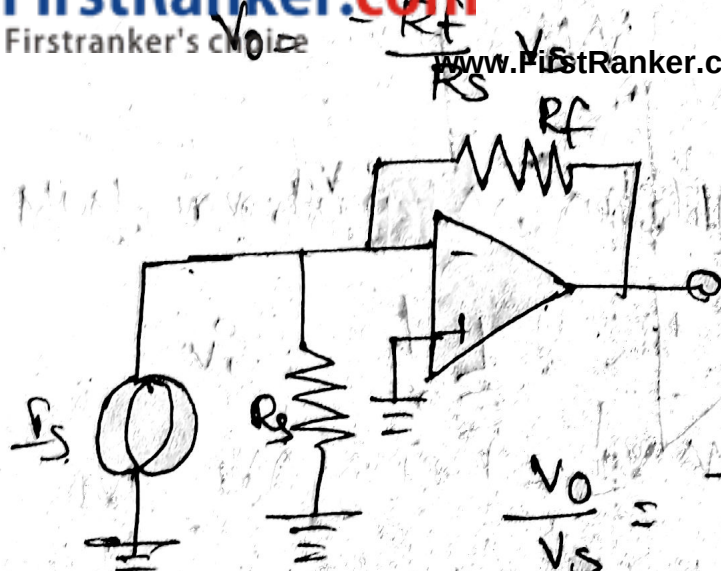
is $\frac{V_o}{V_s} = -\frac{R_f}{R_s}$

where R_s = Source Resistance

Let us assumed that I_s & R_s are replaced by I_s & R_s as shown where $V_s = I_s \cdot R_s$



$V_o = -\frac{R_f}{R_i} \cdot V_{in}$



$$\frac{V_o}{V_s} = -\frac{R_f}{R_s}$$

$$\Rightarrow \frac{V_o}{I_s R_s} = -\frac{R_f}{R_s}$$

$$\therefore V_o = -I_s \cdot R_f$$

Thus output voltage is proportional to the input current. In other words the ckt is

Converting ip current into voltage. In ideal conditions $R_s = \infty$. But in practice R_s is very high. The ckt is also called Trans

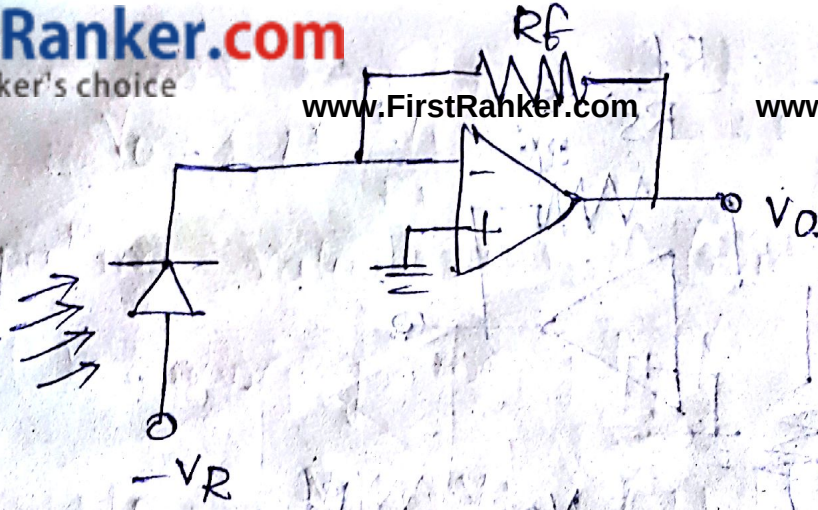
resistance amplifier. Current to voltage

Principle is used in ckt's like photo conducting and photo voltaic detectors.

photo detectors are Transducers that produce electric current in response to

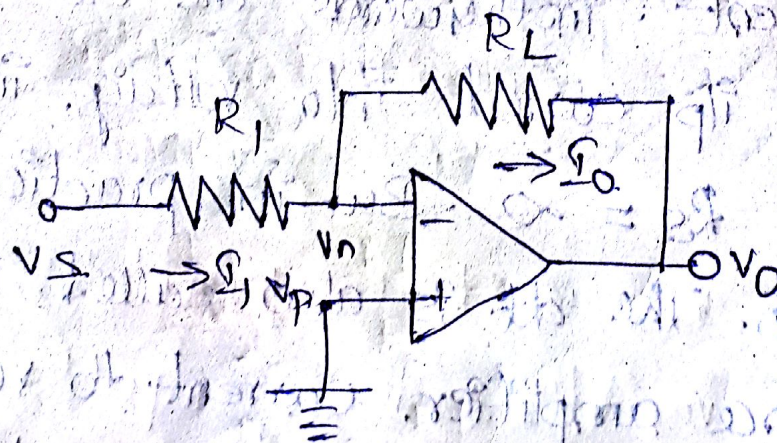
incident light. a transresistance

amplifier converts this current to a voltage.



Voltage to Current Converter

floating load means the load is connected in the feedback grounded load means one of the terminal node is grounded.



$$I_1 = \frac{V_S - V_N}{R_1} = \frac{V_S}{R_1} \quad (\because V_N = V_P = 0)$$

$$I_1 = \frac{V_S}{R_1} = \left(\frac{1}{R_1} \right) V_S$$

$$I_0 = \frac{1}{R_1} V_S$$

The ckt is also called Trans

Conductance amplifier

is required to drive the reflected coil in television.

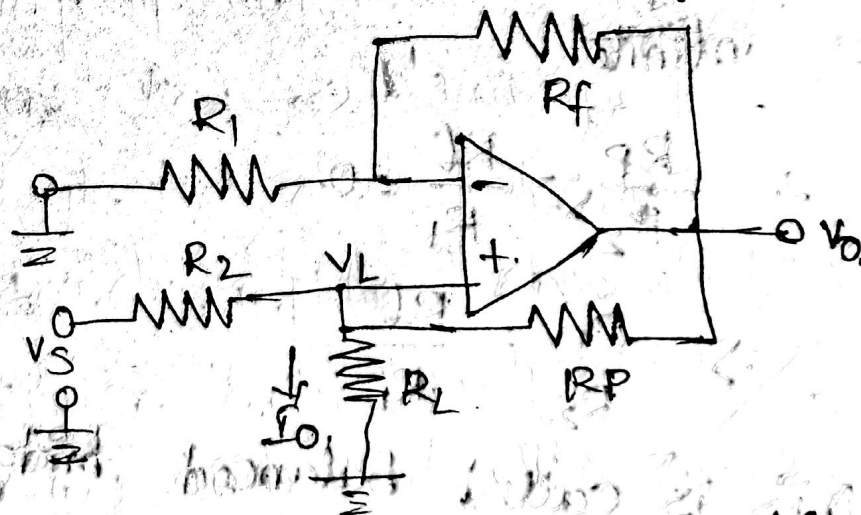
the load may be the reflection coil or transducer V_L is limited such that

$$-V_{sat} < V_L < V_{sat}$$

Voltage to current converter (Grounded load)

It is desired to ground one of load terminals it is no longer possible to place load in feedback.

The following V to Σ Converter Grounded Load is shown in fig. it employs positive and negative feedback.



Applying KCL at non inverting Load

$$\frac{V_S - V_L}{R_2} + \frac{V_O - V_L}{R_1} = 0 \quad \text{--- (A)}$$

Assuming i_p current to op-amp is negligible.

$$V_0 = \left(1 + \frac{R_F}{R_1}\right) V_L \quad \text{--- (B)}$$

putting value of V_0 from B in A, &
rearranging we get

$$I_0 = \frac{V_S}{R_2} - \frac{V_L}{R_2} - \frac{\left(1 + \frac{R_F}{R_1}\right) V_L}{R_F} = \frac{V_L}{R_1} \frac{R_1 + R_F}{R_1 R_2}$$

$$I_0 = \frac{V_S}{R_2} - V_L \left(\frac{1}{R_2} + \frac{R_1}{R_1 R_2} + \frac{R_F}{R_1 R_2} + \frac{1}{R_F} \right)$$

$$I_0 = \frac{V_S}{R_2} - \frac{V_L}{R_0} \quad \text{where } R_0 = \frac{R_F}{\frac{R_F}{R_2} - \frac{R_F}{R_1}}$$

for ideal current source behavior I_0 must be independent of V_L . i.e., R_0 must be infinite.

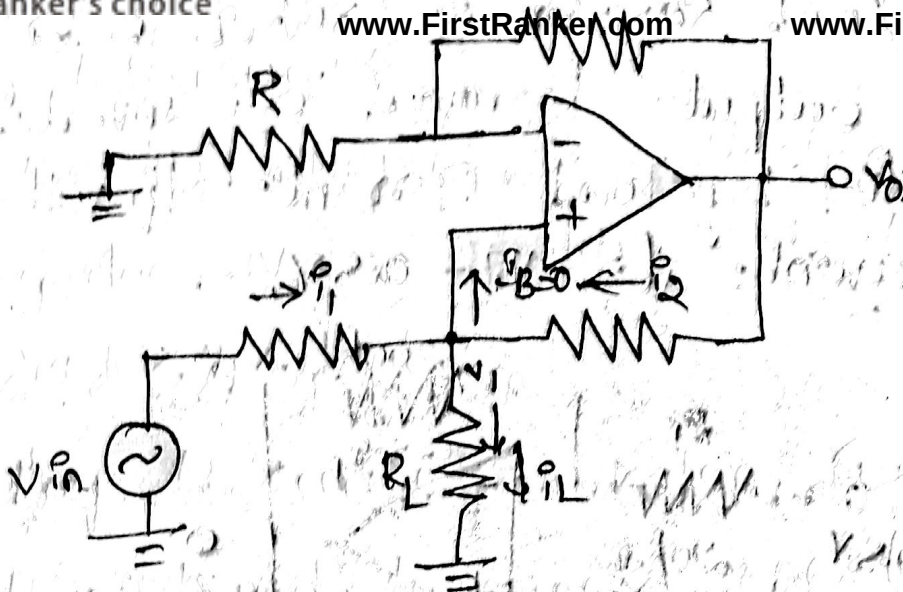
$$\therefore \frac{R_F}{R_2} - \frac{R_F}{R_1} = 0$$

$$\Rightarrow \frac{R_F}{R_2} = \frac{R_F}{R_1}$$

This is called balanced bridge condition.

$$\therefore I_0 = \frac{V_S}{R_2} = \left(\frac{1}{R_2}\right) V_S$$

So the o/p current is independent of Load voltage V_L .



writing KCL at Node 'a'

$$I_1 + I_2 = I_L \quad (\because I_B \text{ is negligible})$$

$$\frac{V_{in} - V_1}{R} + \frac{V_O - V_1}{R} = I_L$$

$$\frac{V_{in}}{R} - \frac{V_1}{R} + \frac{V_O}{R} - \frac{V_1}{R} = I_L$$

$$V_{in} + V_O - 2V_1 = I_L R \quad \text{--- (A)}$$

$$2V_1 = V_{in} + V_O - I_L R \quad \text{--- (B)}$$

Since op-amp in non-inverting mode

$$1 + \frac{R}{R} = 2$$

$$\frac{V_O}{V_1} = 2 \Rightarrow V_O = 2V_1$$

putting $2V_1 = V_O$ in (B)

$$2V_1 = V_{in} + 2V_1 - I_L R$$

$$I_L R = V_{in}$$

$$I_L = \left(\frac{1}{R}\right) V_{in}$$

2. Design an amplifier to have a gain of +8 using single op-amp.

sol:

$$\text{gain} = \frac{V_o}{V_{in}} = \left(1 + \frac{R_f}{R_i} \right)$$

$$8 = \left(1 + \frac{20}{3} \right)$$

$$= 1 + 7$$

Comparators: It is basically open loop configuration and op-amp produces the o/p as $+V_{sat}$ or $-V_{sat}$

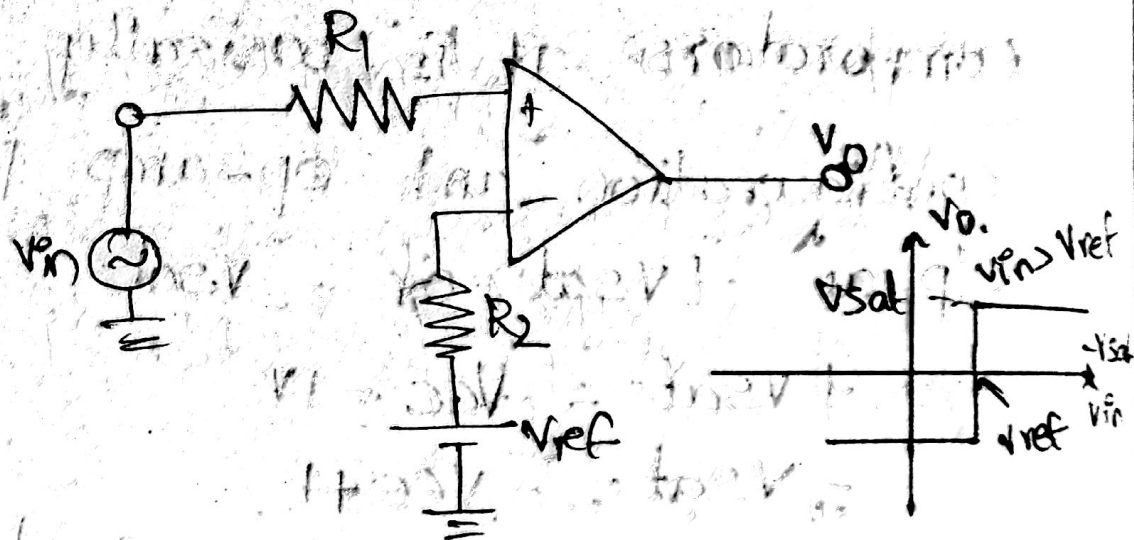
$$+V_{sat} = V_{cc} - 1V$$

$$-V_{sat} = -V_{ee} + 1V$$

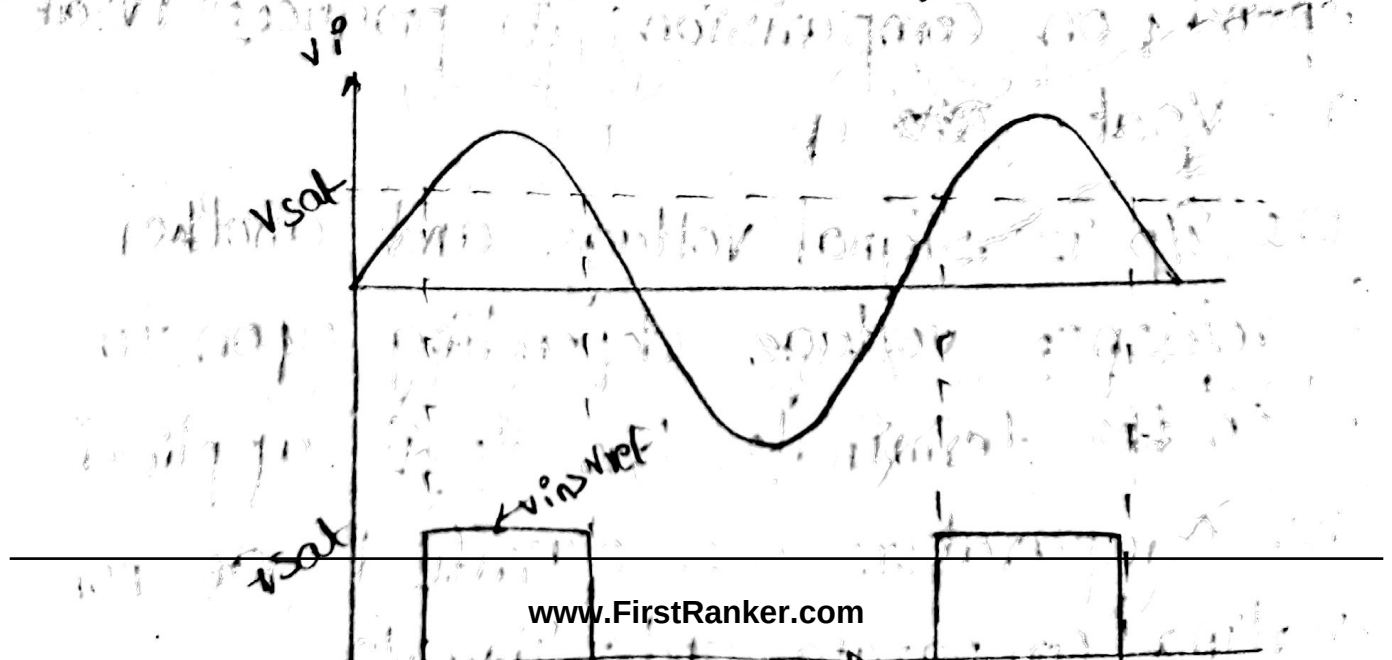
Op-amp compares two inputs and depend on comparison it produces $+V_{sat}$ or $-V_{sat}$.

* One i/p is signal voltage and another is reference voltage depending upon to which the terminals the i/p is applied the comparators are classified as non inverting comparator and Inverting comparator. The $V_o = \pm V_{sat}$ because open loop gain of op-amp is very high

- Even for small signals. Very important thing is no feedback to the op-amp.
- * The point at which the transfer characteristic is straight line is tripper
 - * The Trip point moves to V_{ref} when $V_{in} > \text{trip point}$ o/p is high. while $V_{in} < \text{trip point}$ o/p is low for non inverting Comperator

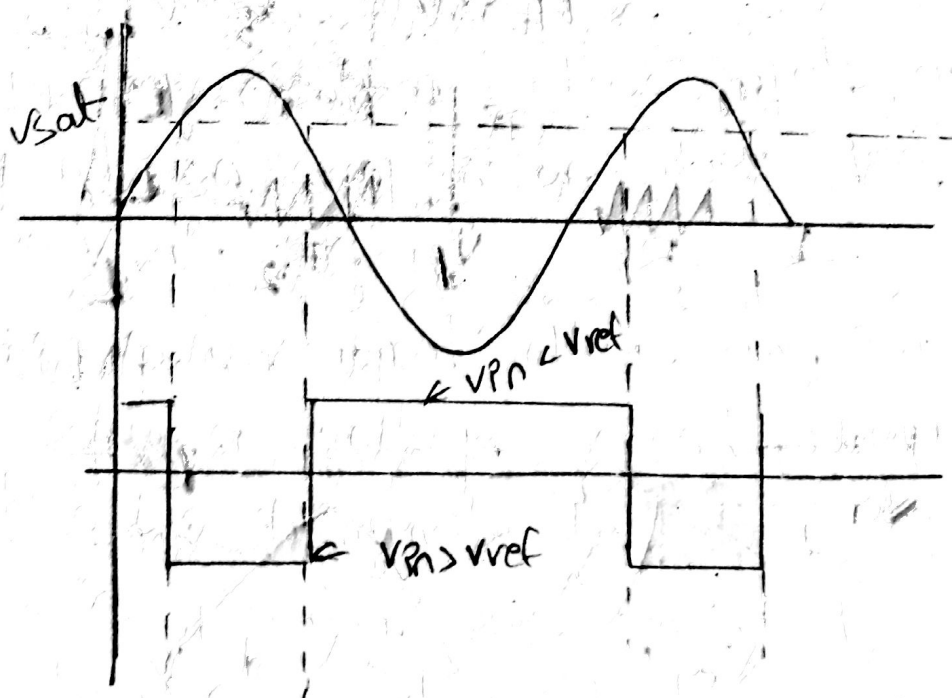
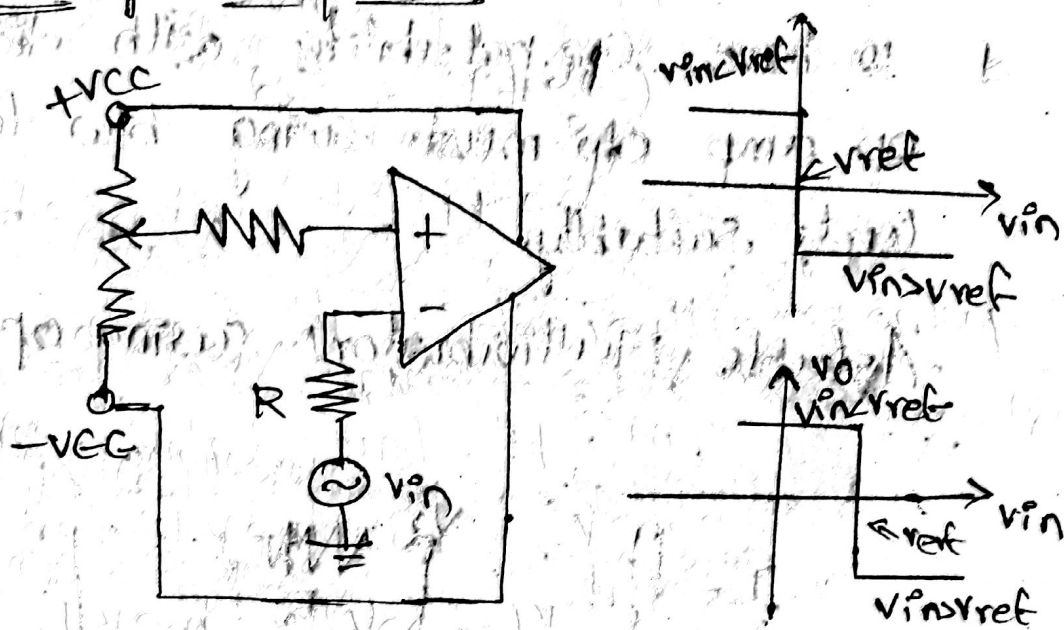


Non-Inverting Comperator.



V_{ref} is applied to inverting terminal
signal is given to non-inverting terminal
based on the transfer characteristics if
 $V_{in} > V_{ref}$ o/p is V_{sat} if $V_{in} < V_{ref}$ o/p
is $-V_{sat}$.

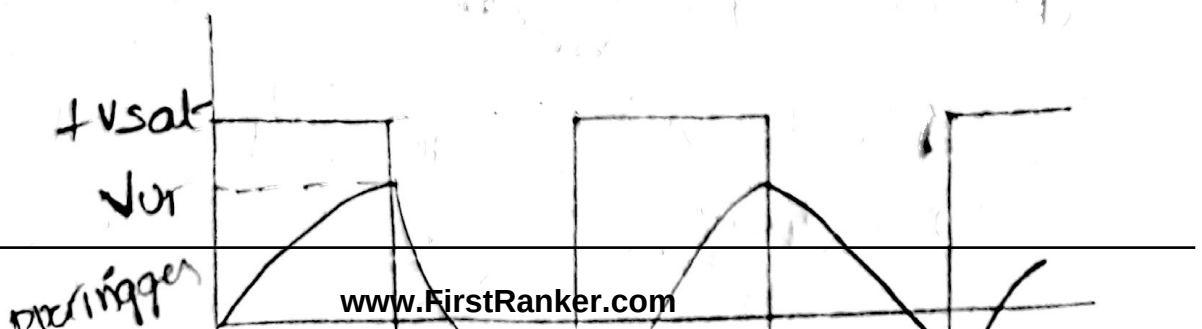
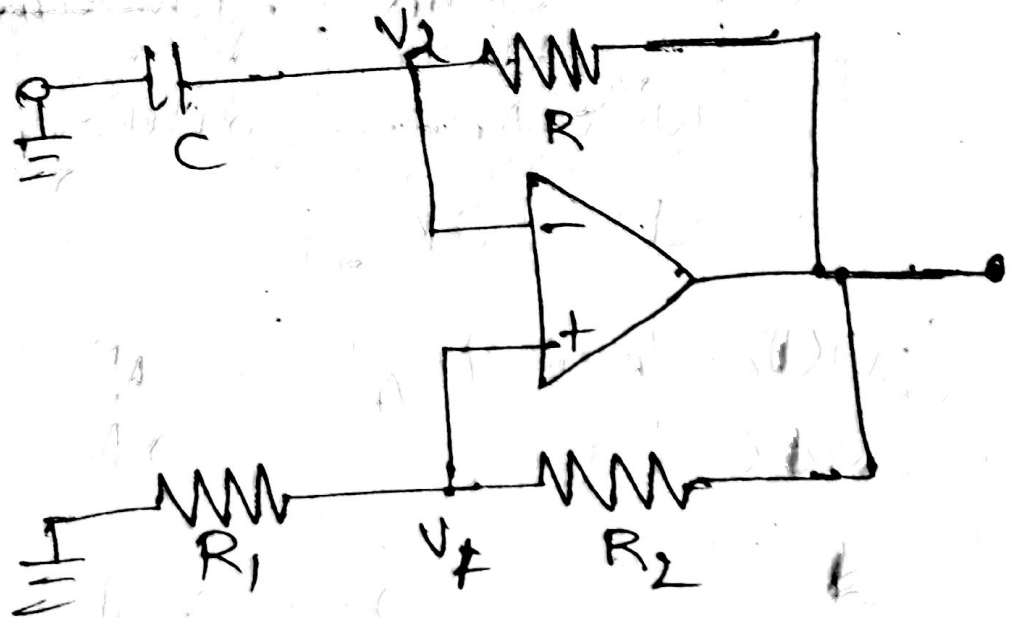
Inverting Comparator



What are the limitations of op-amp Comparator.

- * To have better accuracy. op-amp must have high CMRR, high gain, negligible i_p & negligible offset.
- * The response time should be minimum. to respond to instantaneous changes of i/p .
- * To have compatibility with digital devices op-amp o/p must swing b/w two logic levels suitably.

Astable Multivibrator:- (using op-amp)



The Astable multivibrator has two Quasistable states it is also called free running multivibrator or free running oscillator. In this ckt, Op switches between $+V_{sat}$ or $-V_{sat}$. Assume Capacitor has more charge initially then $V_2 = 0$. But V_1 is not equal to zero due to output offset voltage. V_1 may be positive or negative depends on op-amp. If V_1 will be positive then Op switches to $+V_{sat}$. Now, Capacitor charges through R then V_2 is. When $V_2 > V_1$ then V_0 switches to $-V_{sat}$. Now, Capacitor discharges fully and charges in opposite direction.

When V_2 is slightly more negative than V_1 , the op-amp switches to $+V_{sat}$ again & this completes one cycle.

Frequency of oscillation

$$V_c(t) = V_{max} + (V_{initial} - V_{max}) e^{-t/\tau}$$

$V_c(t)$ = Instantaneous voltage of capacitor.

$V_{initial}$ = Initial voltage

V_{max} = voltage towards which capacitor is charging.

$$V_{UT} = V_{sat} + (V_{LT} - V_{sat}) e^{-T_1/RC}$$

$$V_{sat} - V_{UT} = -(V_{UT} - V_{sat}) e^{-T_1/RC}$$

$$V_{sat} - V_{UT} = (V_{sat} - V_{LT}) e^{-T_1/RC}$$

$$\frac{V_{sat} - V_{UT}}{V_{sat} - V_{LT}} = e^{-T_1/RC}$$

$$\frac{-T_1}{RC} = \ln \left[\frac{V_{sat} - V_{UT}}{V_{sat} - V_{LT}} \right]$$

$$T_1 = -RC \ln \left[\frac{V_{sat} - V_{UT}}{V_{sat} - V_{LT}} \right]$$

[we apply
→ No log of
the term
reversed]

$$T = 2RC \ln \left[\frac{V_{sat} - V_{LT}}{V_{sat} - V_{UT}} \right]$$

But $V_{UT} = \frac{R_1}{R_1 + R_2} \cdot V_{sat}$

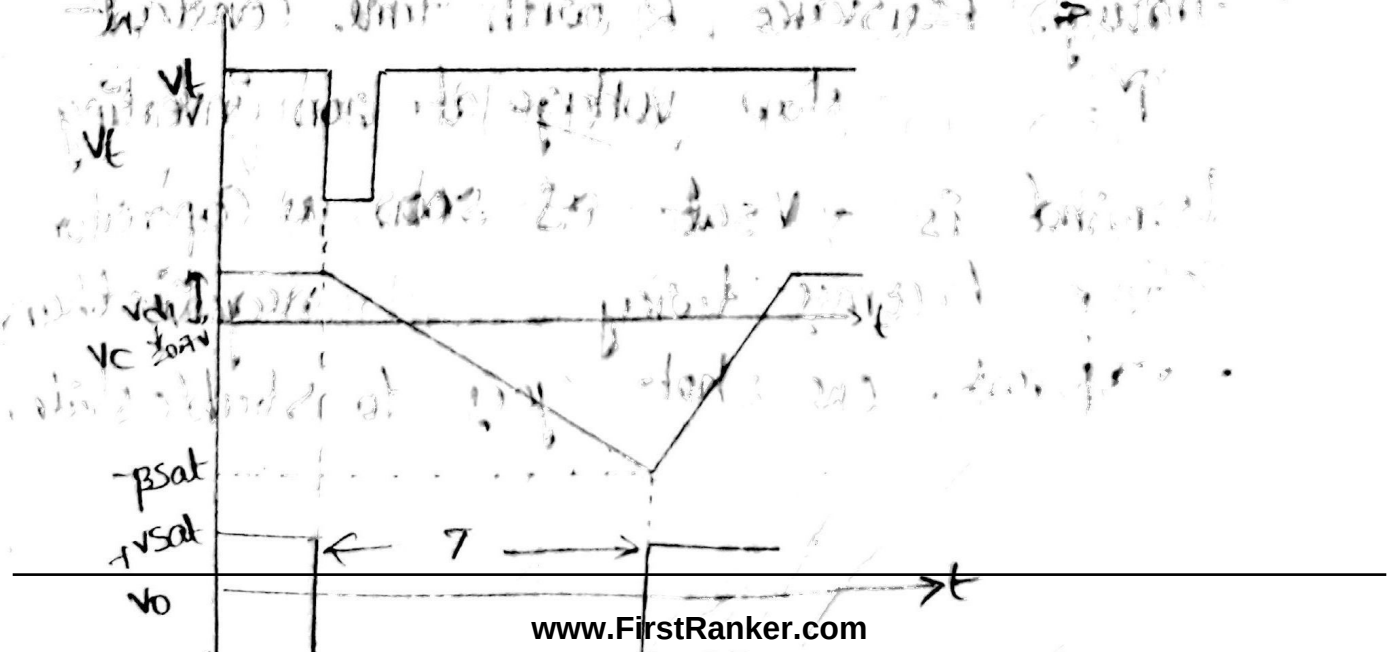
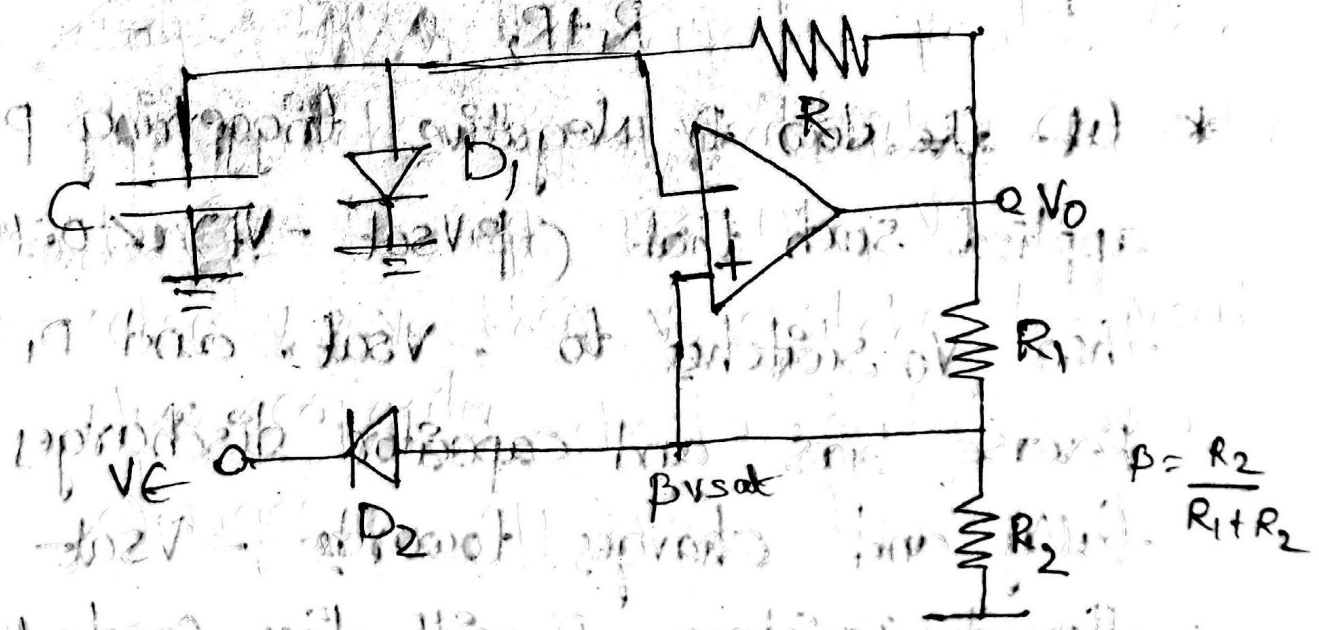
$$V_{LT} = \frac{R_1}{R_1 + R_2} (-V_{sat})$$

$$T = 2RC \ln \left[\frac{V_{sat} - \frac{R_1}{R_1+R_2} (V_{sat})}{V_{sat} - \frac{R_1}{R_1+R_2} (V_{sat})} \right]$$

$$= 2RC \ln \left[\frac{V_{sat} \left(1 + \frac{R_1}{R_1+R_2} \right)}{V_{sat} \left(1 - \frac{R_1}{R_1+R_2} \right)} \right]$$

$$T = 2RC \ln \left[\frac{2R_1 + R_2}{R_2} \right]$$

Monostable Multivibrator



* Monostable Multivibrator is also called

one shot (or) Monoshot. It has one stable state and one Quasi stable state.

* The Diode D_1 clamps the capacitor voltage ~~to~~ to $0.7V$. Let us assume the circuit is in stable state. Therefore $V_o = +V_{sat}$.

* Now voltage at non inverting terminal is $+ \beta V_{sat}$ - $\beta = \frac{R_2}{R_1 + R_2}$

* Let ~~the~~ Now a Negative triggering pulse applied such that $(\beta V_{sat} - V_t) < 0.7V$ then V_o switches to $-V_{sat}$ and D_1 is Reverse bias and capacitor discharges fully and charges towards $-V_{sat}$ through Resistance R with time constant $\tau = RC$. Now voltage at non inverting terminal is $-V_{sat}$ as soon as capacitor voltage becomes twice negative than $- \beta V_{sat}$. One shot goes to stable state.

General Solution for time period T

$$V_C = V_0 = V_{\text{find}} + (V_{\text{initial}} - V_{\text{find}}) e^{-t/RC}$$

$$V_{\text{find}} = -V_{\text{sat}} \quad \& \quad V_{\text{initial}} = V_{D1}$$

$$V_C = -V_{\text{sat}} + (V_{D1} - (-V_{\text{sat}})) e^{-t/RC}$$

$$\text{at } t = T \quad V_C = -\beta V_{\text{sat}}$$

$$-\beta V_{\text{sat}} = -V_{\text{sat}} + (V_{D1} + V_{\text{sat}}) e^{-T/RC}$$

$$(V_{D1} + V_{\text{sat}}) e^{-T/RC} = V_{\text{sat}} (1 - \beta)$$

$$e^{-T/RC} = \frac{V_{\text{sat}} (1 - \beta)}{V_{D1} + V_{\text{sat}}}$$

If $R_1 = R_2$ & $V_{\text{sat}} \gg V_{D1}$ then

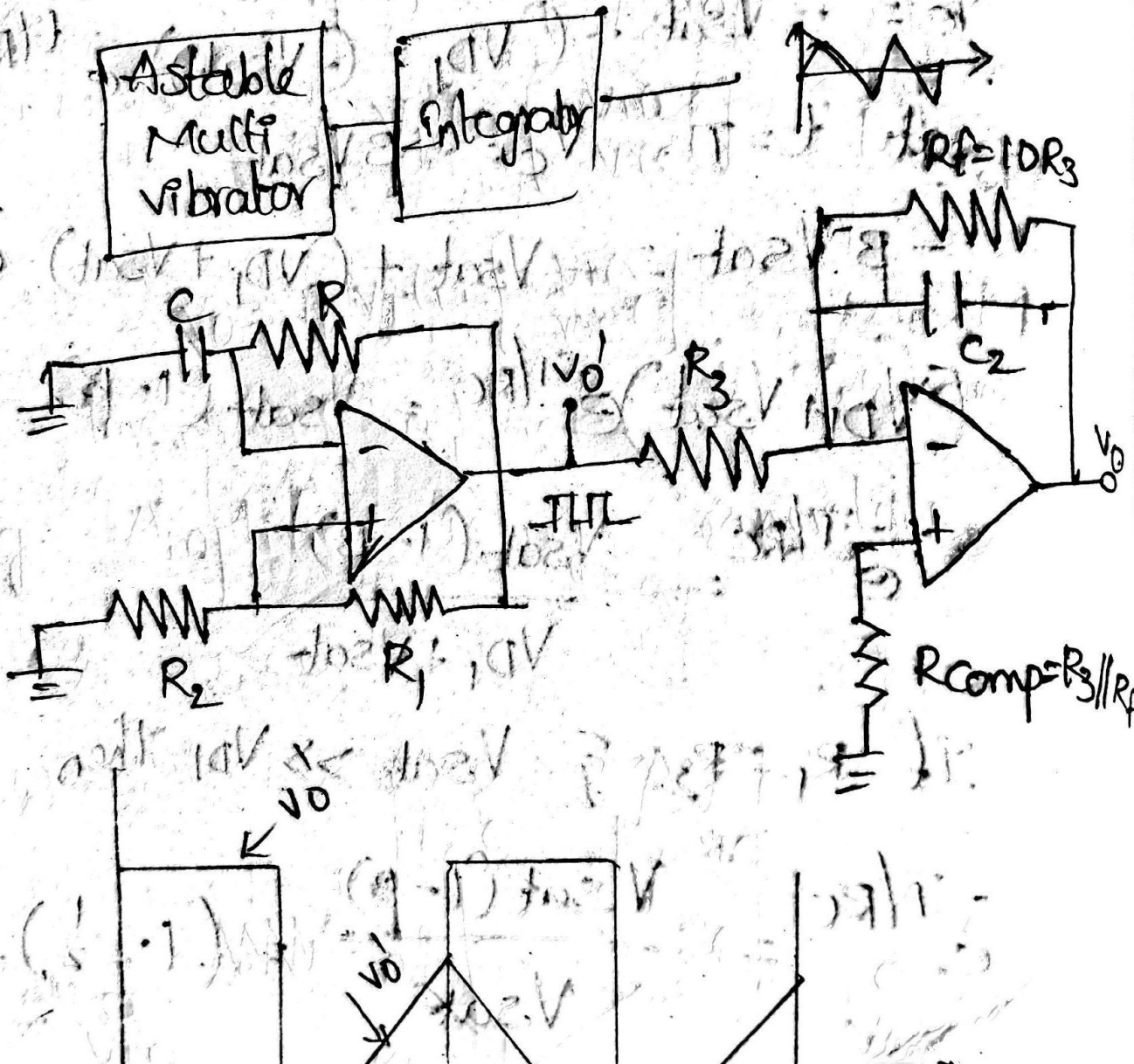
$$e^{-T/RC} = \frac{V_{\text{sat}} (1 - \beta)}{V_{\text{sat}}} = (1 - \frac{1}{2}) = \frac{1}{2}$$

$$T = RC \log_e 2$$

$$\boxed{T = 0.69 RC}$$

Triangular wave generator:-

If Astable Multivibrators output is given to an Integrator we get triangular wave



From $v-i$ characteristic of diode

$$I = I_0 \left(e^{\frac{V}{\eta V_T}} - 1 \right) \approx I_0 e^{\frac{V}{\eta V_T}}$$

$$e^{\frac{V}{\eta V_T}} = \frac{I V}{I_0 V}$$

$$\frac{V}{\eta V_T} = \ln \left(\frac{I V}{I_0 V} \right)$$

$$V = \eta V_T \ln \left(\frac{I}{I_0} \right)$$

here V = diode voltage

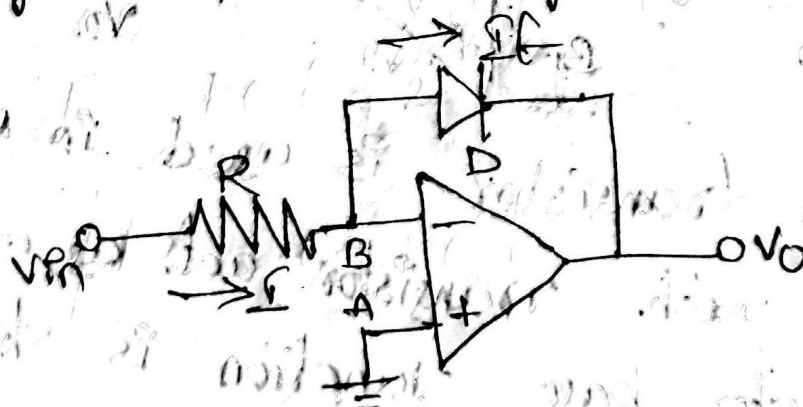
I = diode current

I_0 = reverse saturation current

V_T = volt - equivalent temp = 26mV

$\eta = 1$ (Ge) $\eta = 2$ (Si)

Log - Amplifier using Diode.



$V_A = V_B = 0$ based on virtual ground

$$I = \frac{V_{in} - V_B}{R} = \frac{V_{in}}{R}$$

Voltage across diode = $V_B - V_O = V_O$

$$I_f = I = \frac{V_{in}}{R}$$

$$-V_O = \eta V_T \ln \left[\frac{I_f}{I_0} \right]$$

$$= \eta V_T \ln \left[\frac{V_{in}}{R \cdot I_0} \right]$$

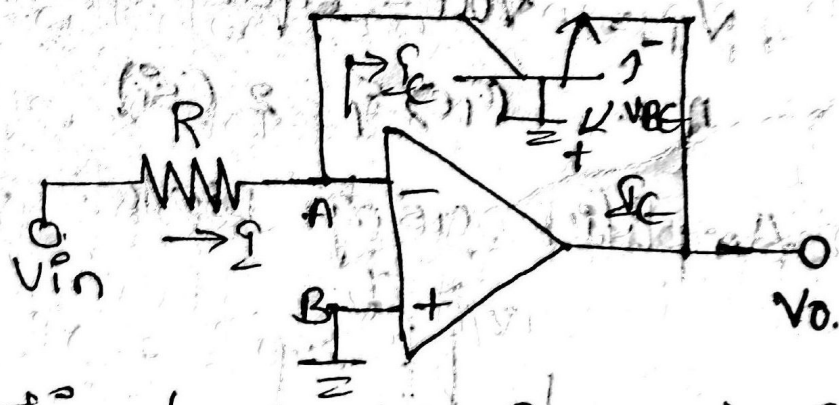
$$= \eta V_T \ln \left[\frac{V_{in}}{V_{ref}} \right]$$

$$I_{OR} = \frac{V_{ref}}{R}$$

$$-V_O = \eta V_T \ln \left[\frac{V_{in}}{V_{ref}} \right]$$

Here V_O , V_T and V_{ref} are constants.

Log-Amplifier using Transistor



In this transistor, is used in negative feedback path. Transistor acts as a diode as collector base junction is shorted.

$$I = \frac{V_{in} - V_A}{R} = \frac{V_{in}}{R}$$

as no current flows into op amp

$$V_{BE} = \eta V_T \ln \left[\frac{I_C}{I_0} \right]$$

But $V_0 + V_{BE} = 0$ $\therefore -V_0 = V_{BE}$

$$-V_0 = \eta V_T \ln \left[\frac{I_C}{I_0} \right]$$

$$V_0 = \eta V_T \ln \left[\frac{V_0}{R I_0} \right]$$

Let $V_{ref} = I_0 R$, then

$$V_0 = -\eta V_T \ln \left[\frac{V_{in}}{V_{ref}} \right]$$

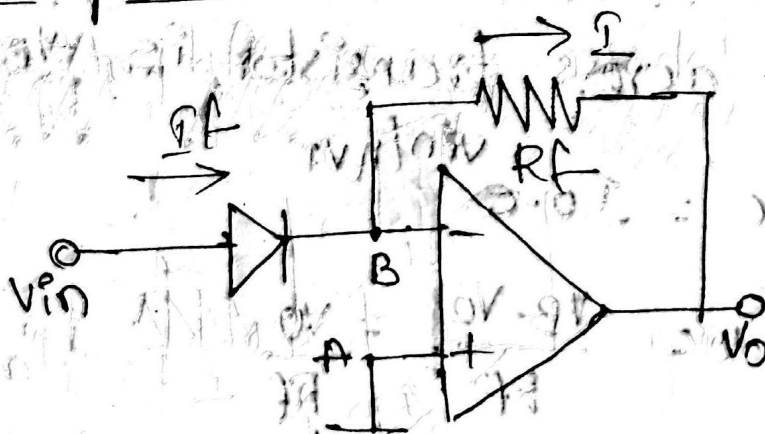
$$\ln \log x = \log x$$

$$\frac{\log x}{\log e} = \frac{\log 10}{0.4343}$$

$$\log e$$

$$0.4343$$

Antilogarithmic Amplifier using diode



* The node A is grounded hence Node B at virtual ground. Therefore $V_A = V_B = 0$.

$$I_f = I_0 e^{V_{in}/\eta V_T} \quad (\because \text{Diode voltage across diode} = V_{in})$$

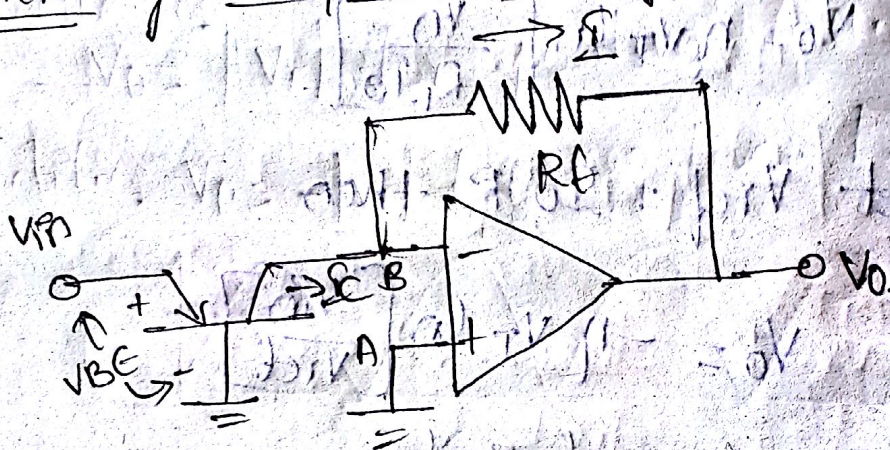
$$I = I_f = \frac{V_B - V_O}{R_f} = \frac{-V_O}{R_f}$$

$$C = \frac{V_B - V_O}{R_f}$$

$$\frac{-V_O}{R_f} = I_0 e^{v_{in}/nV_T}$$

$$V_O = -(I_0 \cdot R_f) e^{v_{in}/nV_T} = -V_{ref} e^{v_{in}/nV_T}$$

Anti Log Amplifier using Transistor



* $V_A = V_B = 0$ as per virtual ground

* Both collector and Base are at ground potential $\therefore V_{CB} = 0$.

Voltage across transistor is $V_{BE} = v_{in}$

$$I_C = I_0 e^{v_{in}/nV_T}$$

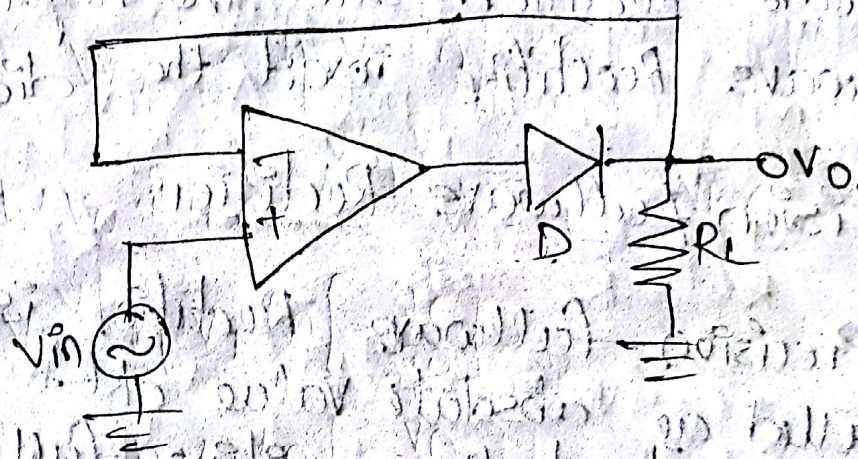
$$I = \frac{V_B - V_O}{R_f} = \frac{-V_O}{R_f}$$

$$\frac{-V_O}{R_f} = I_0 e^{v_{in}/nV_T}$$

$$V_O = -I_0 R_f e^{v_{in}/nV_T}$$

$$V_O = -(V_{ref}) e^{v_{in}/nV_T}$$

Precision Rectifier



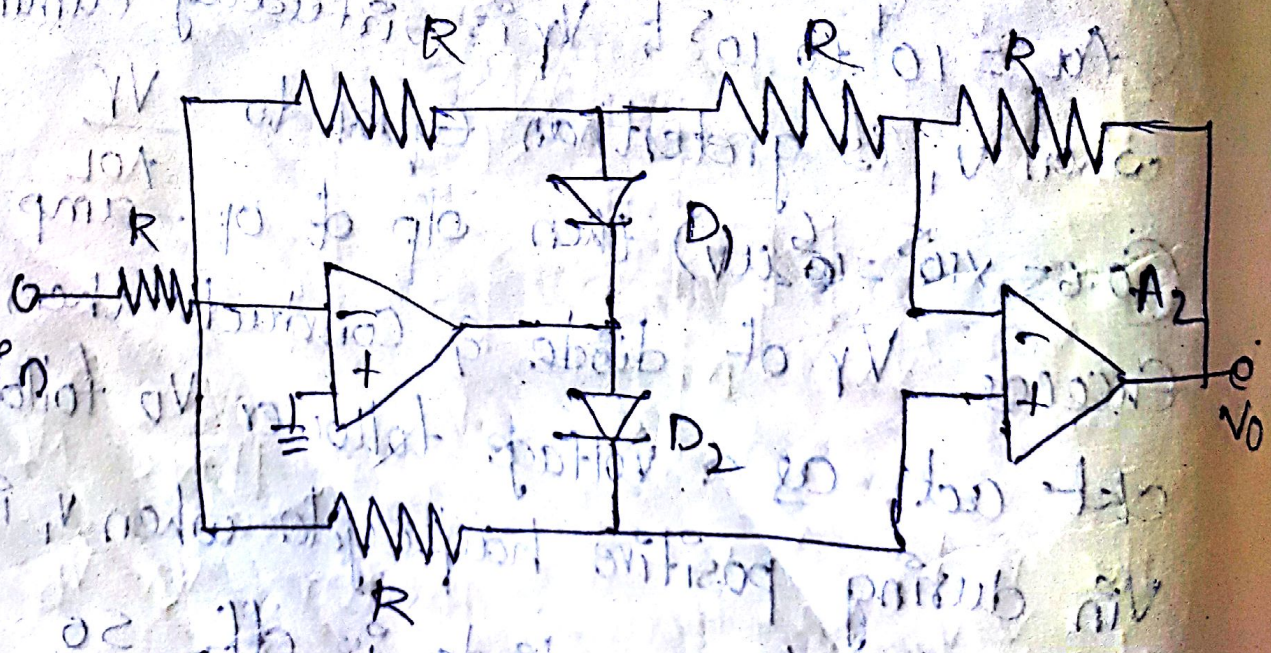
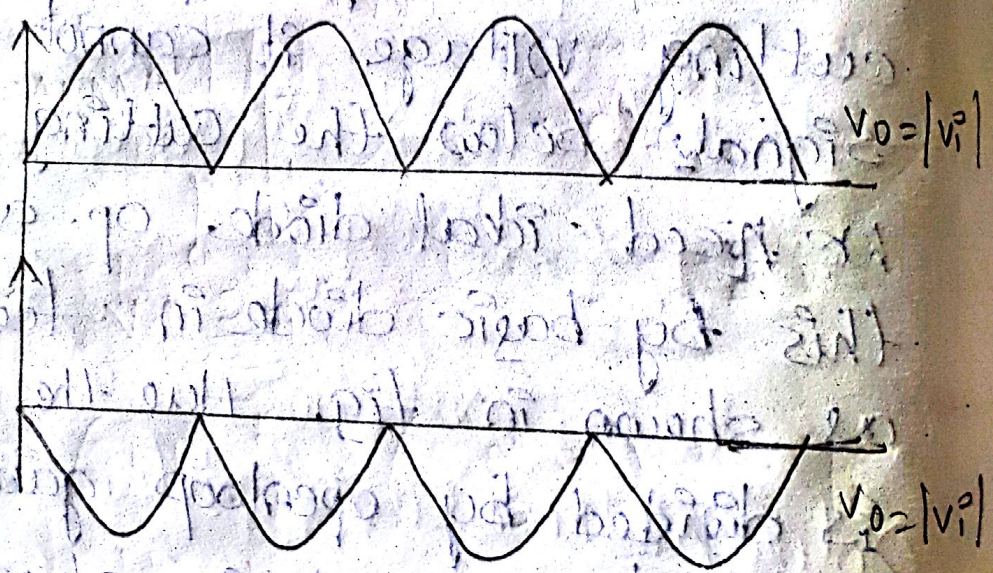
The major drawback of ordinary diode is it can rectify signals greater than cutting voltage. it cannot rectify signals below the cutting voltage. so we need ideal diode, op-amp fulfills this by basic diode in feedback path as shown in fig. here the cut in voltage is divided by openloop gain of op-amp ($A_{OL} = 10^4$ to 10^5) V_r is virtually eliminated when V_i is greater than equal to $\frac{V_r}{A_{OL}}$ ($10.65 \times 10^5 = 10^6 \mu V$) then o/p of op-amp exceeds V_r of diode & conducts then the ckt acts as a voltage follower V_o follows V_{in} during positive half cycle when V_i is -ve or less than $\frac{V_r}{A_{OL}}$ the diode is off so Precision halfwave rectifier is capable of rectifying signals of the order of mV

also called positive precision halfwave Rectifier. But the negative precision halfwave Rectifier, invert the diode.

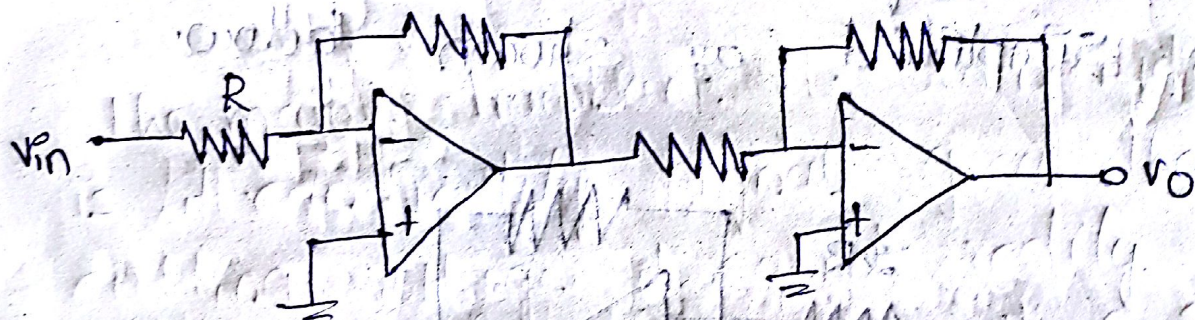
Precision Fullwave Rectifier

Precision fullwave Rectifier is also called as absolute value ckt.

$V_o = |V_i|$ for positive fullwave Rectifier
 $V_o = -|V_i|$ for negative F.W.R



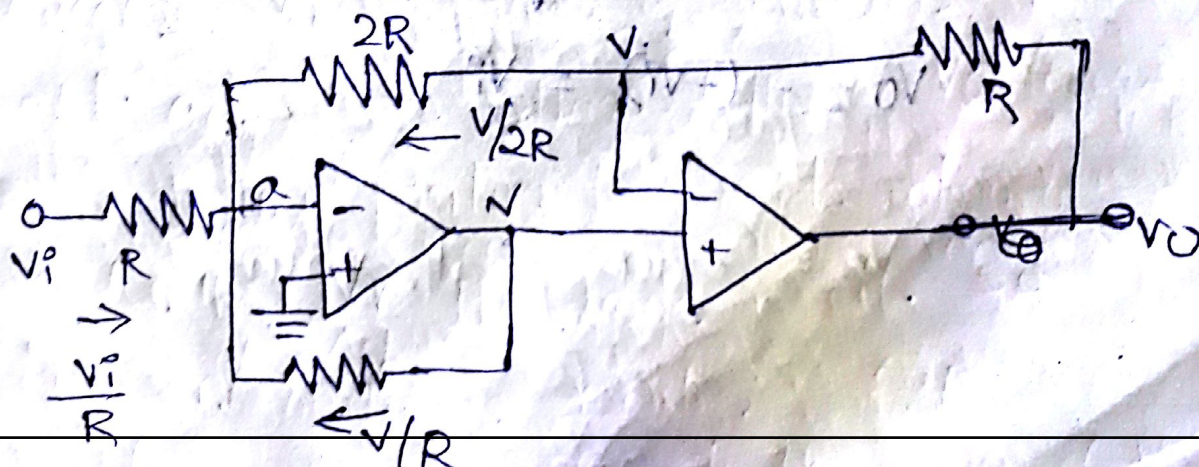
Case (i) when $V_i > 0$, then inverting side of A_1 will force its op to swing negative hence V_1 is forward bias and V_2 is reverse bias. so D_1 is ON, D_2 is OFF and A_1 and A_2 act as inverters the equivalent ckt is shown below.



$$V_1 = -\frac{R_F}{R_1} V_{in} = -\frac{R}{R} V_{in} = -V_{in}$$

$$V_0 = -\frac{R}{R} (-V_{in}) = V_{in}$$

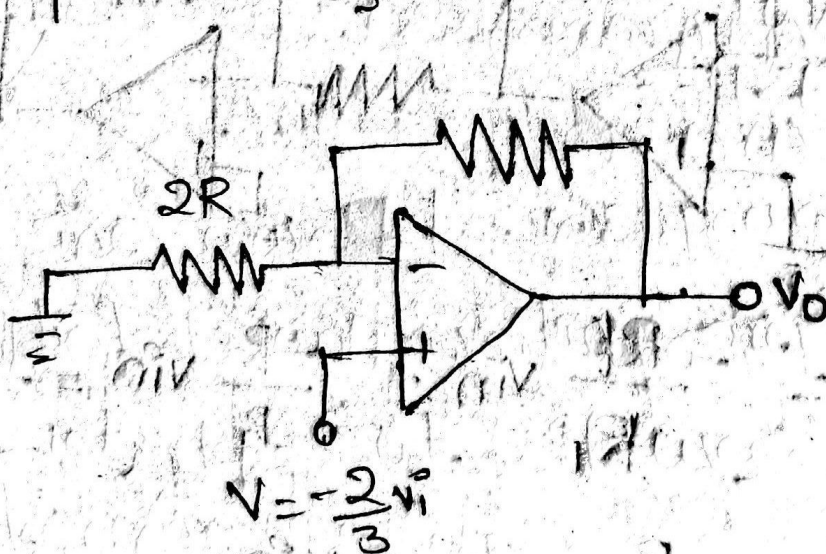
Case (ii) when $V_i < 0$, i.e., negative op voltage of A_1 swings positive making D_1 OFF and D_2 ON the equivalent ckt shown below.



Differential Input If A_2 is zero, the inverting input terminal is at voltage V . Applying KCL to node A gives

$$\frac{V_i}{R} + \frac{V}{R} + \frac{V}{2R} = 0 \Rightarrow V = -\frac{2}{3} V_i$$

The equivalent ckt is further simplified as shown below.



$$V_o = \left(1 + \frac{R}{2R}\right) \left(-\frac{2}{3} V_i\right)$$

$$= \frac{3R}{2R} \times -\frac{2}{3} V_i$$

$$= -V_i$$

The V_i is negative going hence

$$V_o = -(-V_i) = V_i$$

Types of filters:

- (i) Passive : Active
- (ii) Analog : Digital
- (iii) Discrete Time : Continuous Time
- (iv) Time Variant : Time Invariant
- (v) Infinite Impulse Response : Finite Impulse Response
- (vi) Linear : Non-Linear

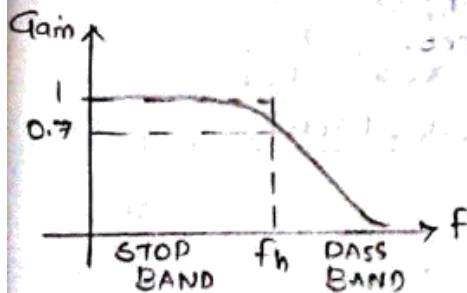
filter is a device which passes the wanted range of frequencies and opposes the unwanted range of frequencies.

Based on operation,

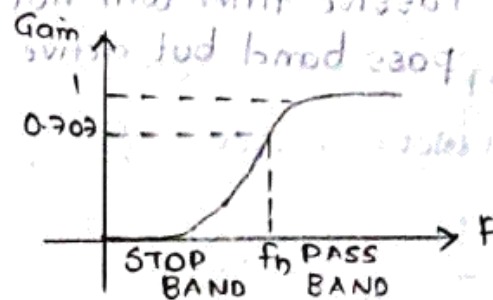
all filters are classified as:

- (i) Low pass filter
- (ii) High Pass filter
- (iii) Band Pass filter
- (iv) Band elimination (or) Band rejection filter
- (v) All pass filter

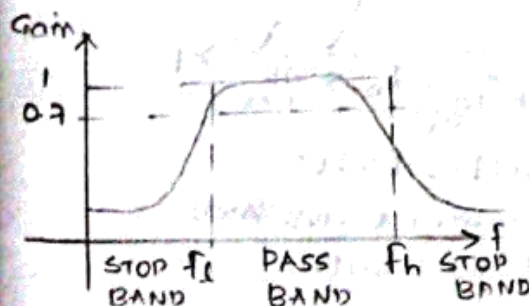
LOW PASS FILTER:



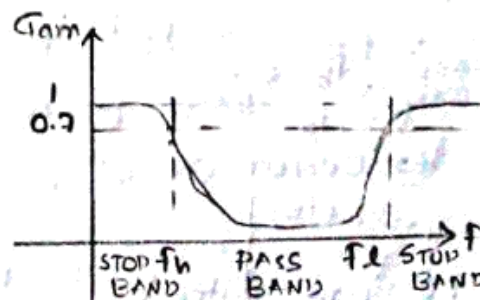
HIGH PASS FILTER:



BAND PASS FILTER:



BAND REJECT FILTER:



It is defined as the frequency at which the gain is:

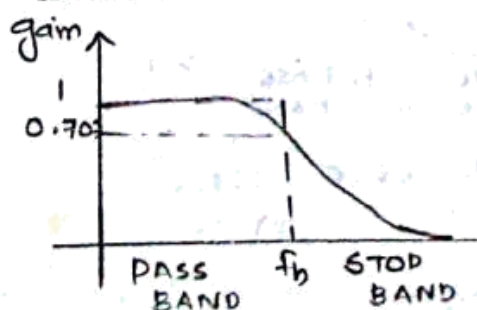
- (i) $1/\sqrt{2}$ of maximum
- (ii) 70% of maximum
- (iii) 3dB lesser than the maximum (in dB)

The filter maximum gain is unity.

Differences between the active filter and passive filters:

- (i) A Passive filters are designed by R, L, C whereas active filters are designed by R, C and any active element like op-amp or transistor.
- (ii) External supply is not needed in passive filter whereas it is used in active filter because the active element has to be operated.
- (iii) Roll-off (slope of the curve between pass band and stop band) is less in passive filter and it is more in active filter (ideal filter, roll-off is infinite)
- (iv) Passive filter will not produce amplification in pass band but active filter produces.

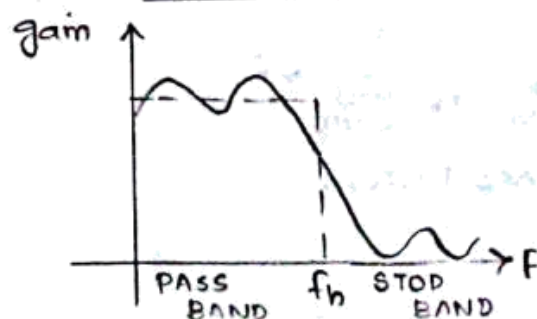
BUTTERWORTH FILTER



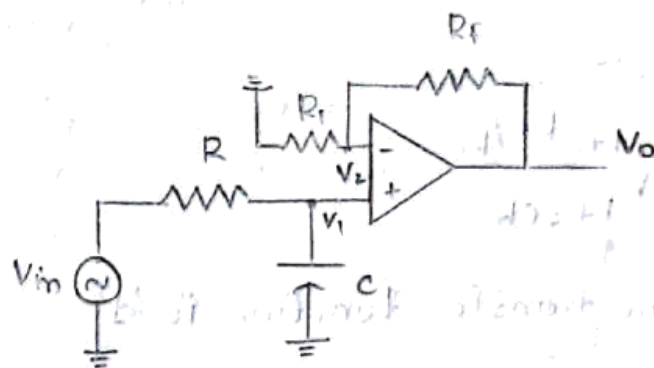
RIPPLES DONOT EXIST

Eg: Low pass filter

CHEBYSHEV FILTER



RIPPLES EXIST
IN STOP BAND AND
PASS BAND



The circuit is in negative feedback.

$$V_1 = V_2$$

and $V_1 = V_2 = 0$ because currents entering into op-amp input terminals is zero.

Applying the nodal analysis at non-inverting terminal of op-amp in Laplace domain,

$$\frac{V_1 - V_{in}(s)}{R} + \frac{V_1 - 0}{1/c_s} + 0 = 0$$

$$-\frac{V_{in}(s)}{R} = -cs[V_1] - \frac{V_1}{R}$$

$$V_1 [1 + sCR] = \cancel{R} \cdot \frac{V_{in}(s)}{\cancel{R}}$$

$$V_1 = \frac{V_{in}(s)}{1 + sCR}$$

Apply the nodal analysis at inverting terminal, (of op-amp)

$$\frac{V_2 - 0}{R_1} + \frac{V_2 - V_o}{R_f} + 0 = 0$$

$$\frac{V_o(s)}{1 + R_f/R_1} = V_2$$

$$V_o(s) = V_2 [1 + R_f/R_1]$$

$$V_o(s) = \frac{V_{in}(s)}{1+sCR} \left[1 + \frac{R_f}{R_i} \right]$$

Transfer function,

$$\frac{V_o(s)}{V_{in}(s)} = \frac{1 + R_f/R_i}{1+sCR}$$

The order of the transfer function is '1'

In frequency domain,

$$\frac{V_o(f)}{V_{in}(f)} = \frac{1 + R_f/R_i}{1+j(2\pi f)RC}$$

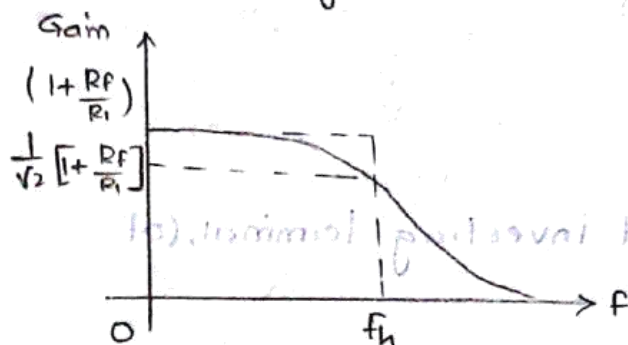
If we apply dc signal as input ($f=0$),

$$\frac{V_o}{V_{in}} = \frac{1 + R_f/R_i}{1+0} = 1 + \frac{R_f}{R_i} > 1$$

Input is an a.c signal with higher frequency $f=\infty$,

$$\frac{V_o}{V_{in}} = 0$$

So, frequency response,



At $f = f_h$,

$$\left| \frac{V_o}{V_{in}} \right| = \frac{1}{\sqrt{2}} \left[1 + \frac{R_f}{R_i} \right]$$

So, at $f = f_h$,

$$\frac{V_o(f_h)}{V_{in}(f_h)} = \frac{1 + R_f/R_i}{1+j(2\pi f_h)RC}$$

$$\left| \frac{V_o(f_h)}{V_{in}(f_h)} \right| = \frac{1 + R_f/R_i}{\sqrt{1+(2\pi f_h RC)^2}}$$

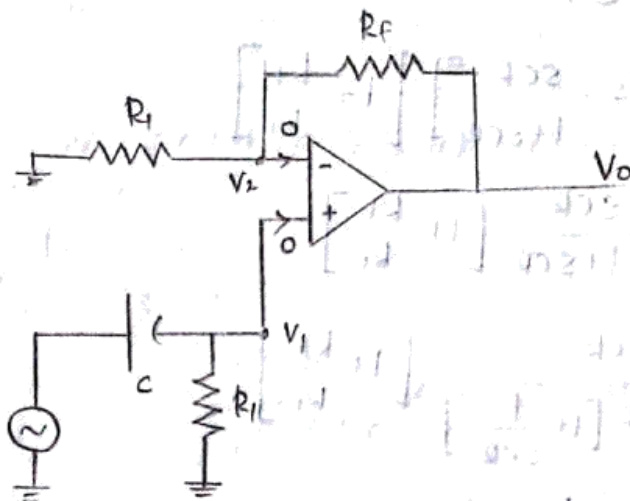
$$\frac{1}{\sqrt{2}} \left[1 + \frac{R_F}{R_1} \right] = \frac{1 + R_F/R_1}{\sqrt{1 + (2\pi f_h RC)^2}}$$

$$1 + 2\pi f_h RC = 2$$

$$f_h = \frac{1}{2\pi RC}$$

22-09-15

1st order Butterworth High Pass filter:



for negative feedback

$$V_1 = V_2 \rightarrow \textcircled{1}$$

Applying Nodal analysis at the non-inverting terminal in Laplace domain,

$$\frac{V_1 - V_{in}(s)}{R_1/sC} + \frac{V_1 - 0}{R} + 0 = 0$$

$$V_1 [sC + \frac{1}{R}] - V_{in}(s) \cdot sC = 0$$

$$V_1 \left[\frac{sCR + 1}{R} \right] - V_{in}(s) \cdot sC = 0$$

$$V_1 = V_{in}(s) \cdot \frac{sCR}{1 + sCR} \rightarrow \textcircled{2}$$

Applying nodal analysis at inverting terminal in Laplace domain,

$$\frac{V_2 - 0}{R_1} + \frac{V_2 - V_0(s)}{R_f} + 0 = 0$$

$$V_2 \left[\frac{1}{R_1} + \frac{1}{R_f} \right] - \frac{V_0(s)}{R_f} = 0$$

$$V_2 \left[\frac{R_1 + R_f}{R_1 R_f} \right] = \frac{V_0(s)}{R_f}$$

$$V_0(s) = V_2 \left[1 + \frac{R_f}{R_1} \right] \rightarrow (3)$$

from (1), (2) and (3),

$$V_0(s) = \left[V_m(s) \cdot \frac{sCR}{1+sCR} \right] \left[1 + \frac{R_f}{R_1} \right]$$

$$\frac{V_0(s)}{V_m(s)} = \frac{sCR}{1+sCR} \left[1 + \frac{R_f}{R_1} \right]$$

$$\begin{aligned} \frac{V_0(s)}{V_m(s)} &= \frac{sCR}{sCR \left[1 + \frac{1}{sCR} \right]} \left[1 + \frac{R_f}{R_1} \right] \\ &= \frac{1 + R_f/R_1}{1 + 1/sCR} \end{aligned}$$

Let, $A_0 = 1 + R_f/R_1$, all the frequency independent part of the transfer function is the DC gain.

$$\frac{V_0(s)}{V_m(s)} = \frac{A_0}{1 + 1/sCR}$$

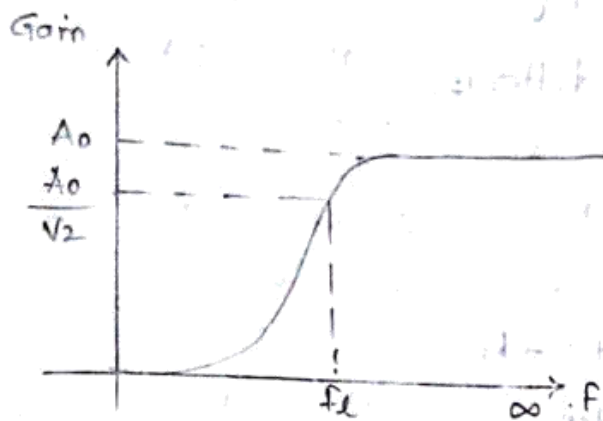
In the frequency domain,

$$\frac{V_0(f)}{V_m(f)} = \frac{A_0}{1 + \frac{1}{j2\pi fRC}}$$

If $f=0$, V_m is a dc signal,

$$\frac{V_0(0)}{V_m(0)} = 0$$

$$\frac{V_o(\infty)}{V_{in}(\infty)} = A_o = 1 + \frac{R_f}{R_1}$$



$$\text{At } f = f_c, \left| \frac{V_o}{V_{in}} \right| = \frac{A_o}{\sqrt{2}}$$

$$\left| \frac{V_o(f)}{V_{in}(f)} \right| = \frac{A_o}{\sqrt{1 + \left(\frac{1}{2\pi f RC} \right)^2}}$$

At $f = f_c$ (cut off frequency),

$$\left| \frac{V_o(f_c)}{V_{in}(f_c)} \right| = \frac{A_o}{\sqrt{1 + \frac{1}{2\pi f_c RC}}}$$

$$\frac{1}{\sqrt{2}} \cdot A_o = \frac{A_o}{\sqrt{1 + (2\pi f_c RC)^{-1}}}$$

$$f_c = \frac{1}{2\pi RC}$$

The maximum gain of the filter is $A_o = 1 + \frac{R_f}{R_1}$ and the cutoff frequency is $f_c = \frac{1}{2\pi RC}$.

Design a butterworth 1st order low pass filter with a maximum gain of 5, with a cutoff frequency 10 kHz and plot the frequency response.

The maximum gain of the filter is,

$$A = 1 + \frac{R_f}{R_i}$$

$$5 = 1 + \frac{R_f}{R_i}$$

$$R_f/R_i = 4 \Rightarrow R_f = 4 R_i$$

Let $R_i = 1 \text{ k}\Omega$, then $R_f = 4 \text{ k}\Omega$

from the expression for time cutoff frequency,

$$f_h = \frac{1}{2\pi RC}$$

$$RC = \frac{1}{2\pi f_h}$$

$$= \frac{1}{2\pi \times 10 \times 1000}$$

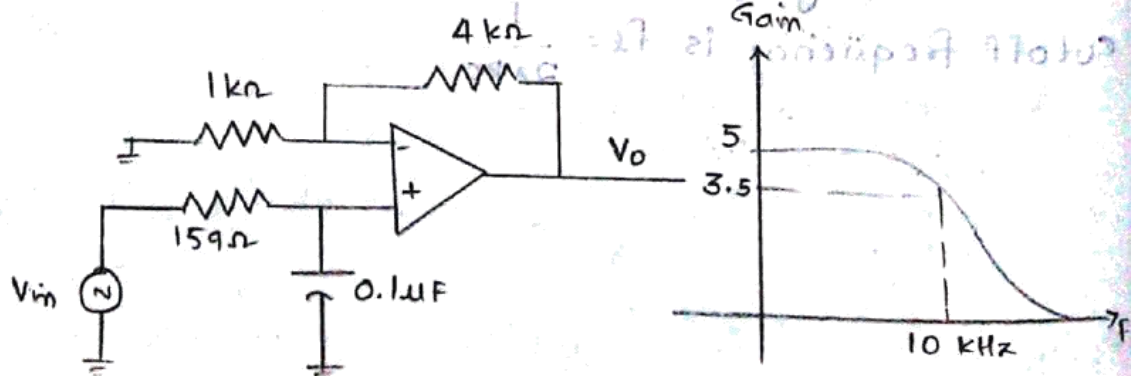
$$= \frac{0.0159}{1000}$$

Let $C = 0.1 \mu\text{F}$,

$$R = \frac{0.0159}{C}$$

$$= \frac{0.0159}{0.1 \times 10^{-6} \times 10^3} = 159 \text{ k}\Omega \times 10^{-3}$$

$$= 159 \Omega$$



Design a non-inverting active low-pass filter with a maximum gain 9, cutoff frequency 1 kHz.

The maximum gain of the filter is,

$$-A_0 = 1 + \frac{R_f}{R_i}$$

$$9 = 1 + \frac{R_f}{R_i}$$

$$R_f = 8R_i$$

Let $R_i = 1 \text{ k}\Omega$, then $R_f = 8 \text{ k}\Omega$

From the expression for cutoff frequency,

$$f_c = \frac{1}{2\pi RC}$$

$$1 \text{ kHz} = \frac{1}{2\pi RC}$$

$$R_c = \frac{1}{2\pi \times 10^3}$$

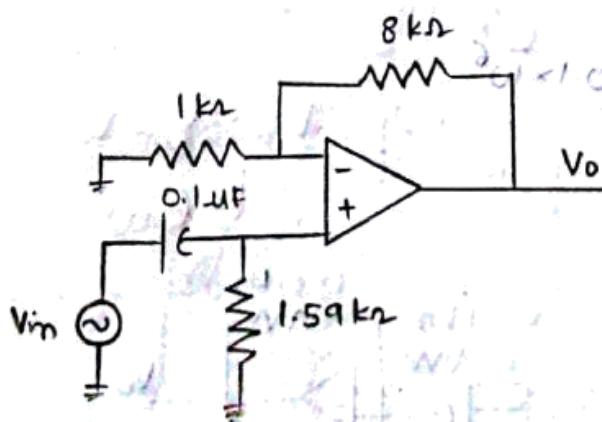
$$= 0.1591 \times 10^{-3}$$

Let $C = 0.1 \mu\text{F}$,

$$R = \frac{1}{2\pi \times 10^3 \times 0.1 \times 10^{-6}}$$

$$= 1591.54 \Omega$$

$$= 1.59 \text{ k}\Omega$$



Design bufferworth and high pass filters with maximum gain 20dB and with cutoff frequency 100kHz and plot the frequency response

The maximum gain,

$$A = 1 + \frac{R_f}{R_i}$$

$$20 \log \left[1 + \frac{R_f}{R_i} \right] = 20$$

$$1 + \frac{R_f}{R_i} = 10$$

$$\frac{R_f}{R_i} = 9$$

$$R_f = 9 R_i$$

Let $R_i = 1 \text{ k}\Omega$, $R_f = 9 \text{ k}\Omega$

As the cutoff frequency is 100kHz,

$$f_c = \frac{1}{2\pi RC}$$

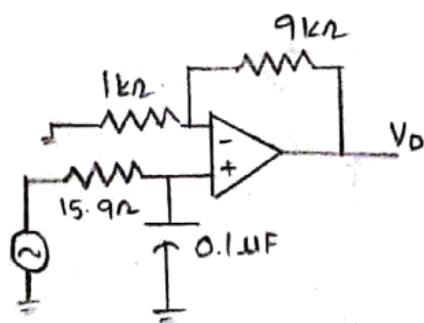
$$10^3 \times 100 = \frac{1}{2\pi RC}$$

$$R = \frac{1}{2\pi \times 10^5 \times C}$$

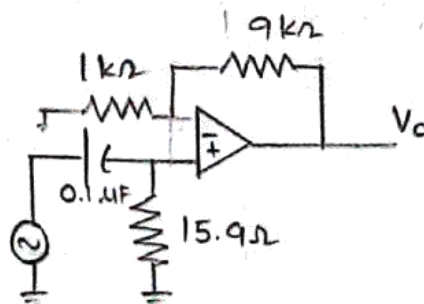
Let $C = 0.1 \mu\text{F}$

$$R = \frac{1}{2\pi \times 10^5 \times 0.1 \times 10^{-6}}$$

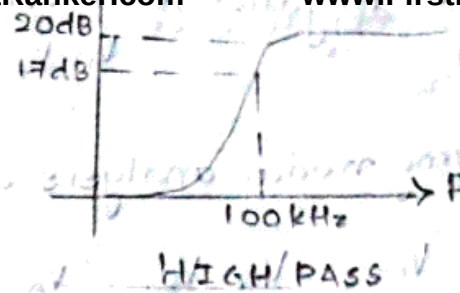
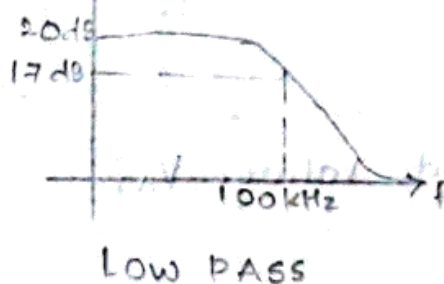
$$= 15.9 \Omega$$



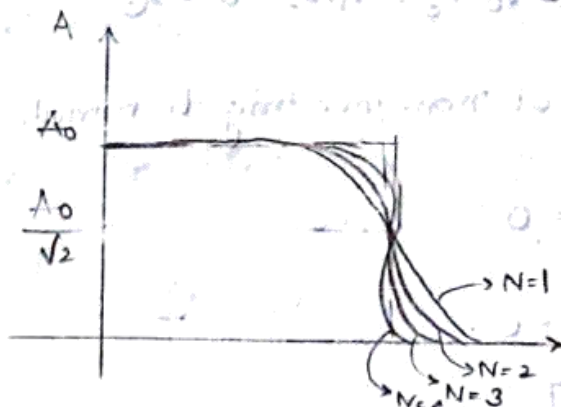
LOW PASS



HIGH PASS



ROLLOFF AND ORDER OF SYSTEM:

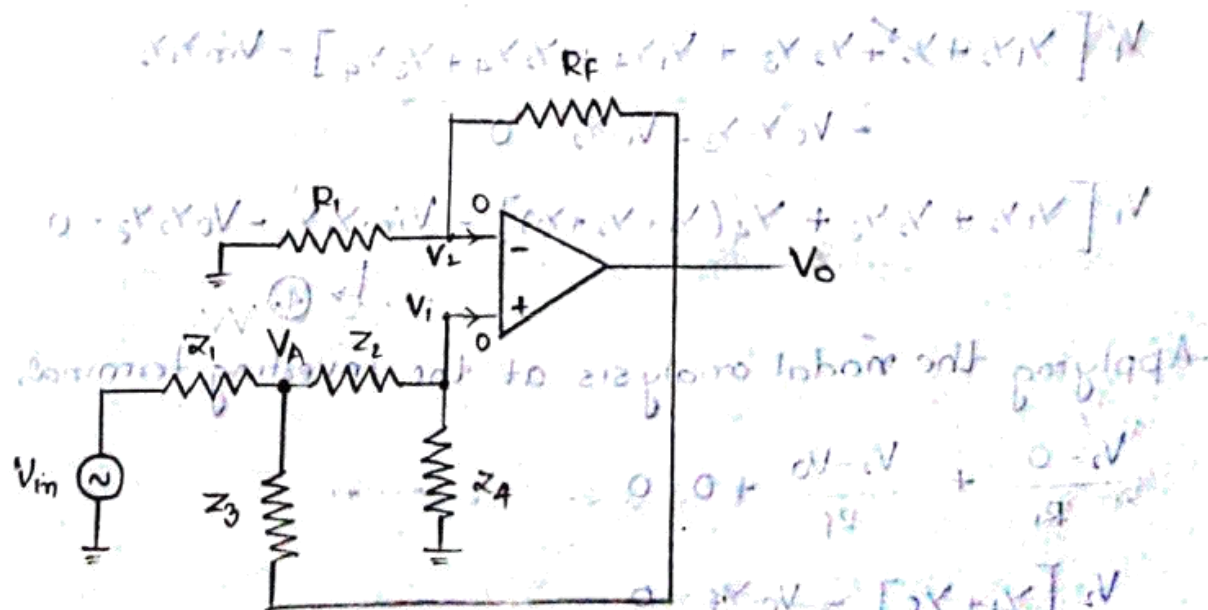


As order of the filter (N) increases, the roll off will be increased. for ideal filter, roll off is infinite

To increase roll off, we have to increase the order

→ Storage elements in the circuit

SALLEN-KEY MODEL:



Due to negative

$$V_1 = V_2 \rightarrow (1)$$

Applying nodal analysis at node voltage V_A ,

$$\frac{V_A - V_{in}}{Z_1} + \frac{V_A - V_0}{Z_3} + \frac{V_A - V_1}{Z_2} = 0$$

$$V_A [Y_1 + Y_2 + Y_3] - V_{in} Y_1 - V_0 Y_3 - V_1 Y_2 = 0 \rightarrow (2)$$

Applying nodal analysis at non-inverting terminal,

$$\frac{V_1 - V_A}{Z_2} + \frac{V_1 - 0}{Z_4} + 0 = 0$$

$$V_1 [Y_2 + Y_4] - V_A Y_2 = 0$$

$$V_A = V_1 \left[1 + \frac{Y_4}{Y_2} \right] \rightarrow (3)$$

Substituting (3) in (2),

$$V_1 \left[1 + \frac{Y_4}{Y_2} \right] [Y_1 + Y_2 + Y_3] - V_{in} Y_1 - V_0 Y_3 - V_1 Y_2 = 0$$

$$V_1 (Y_4 + Y_2) (Y_1 + Y_2 + Y_3) - V_{in} Y_1 Y_2 - V_0 Y_2 Y_3 - V_1 Y_2^2 = 0$$

$$V_1 [Y_1 Y_2 + \cancel{Y_2^2} + Y_2 Y_3 + Y_1 Y_4 + Y_2 Y_4 + Y_3 Y_4] - V_{in} Y_1 Y_2 - V_0 Y_2 Y_3 - \cancel{V_1 Y_2^2} = 0$$

$$V_1 [Y_1 Y_2 + Y_2 Y_3 + Y_4 (Y_1 + Y_2 + Y_3)] - V_{in} Y_1 Y_2 - V_0 Y_2 Y_3 = 0$$

↳ (4)

Applying the nodal analysis at the inverting terminal,

$$\frac{V_2 - 0}{R_1} + \frac{V_2 - V_0}{R_f} + 0 = 0$$

$$V_2 [Y_1 + Y_f] - V_0 Y_f = 0$$

$$V_2 \left[\frac{R_1 + R_F}{R_1 R_F} \right] = \frac{V_O}{R_F}$$

$$V_O = V_2 \left[1 + \frac{R_F}{R_1} \right]$$

$$= V_2 [A_0]$$

$$-A_0 = \frac{V_O}{V_2} \Rightarrow V_2 = \frac{V_O}{A_0} \rightarrow (5)$$

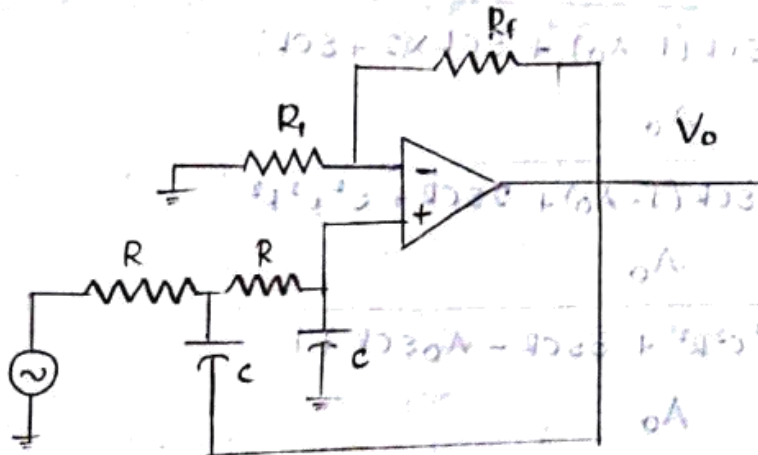
Substituting (5) in (4),

$$\frac{V_O}{A_0} \left[Y_1 Y_2 + Y_2 Y_3 + Y_4 (Y_1 + Y_2 + Y_3) \right] = V_{in} Y_1 Y_2 + V_O Y_2 Y_3$$

$$V_O \left[Y_1 Y_2 + (1 - A_0) Y_2 Y_3 + Y_4 (Y_1 + Y_2 + Y_3) \right] = V_{in} Y_1 Y_2 A_0$$

$$\frac{V_O}{V_{in}} = \frac{Y_1 Y_2 A_0}{Y_1 Y_2 + (1 - A_0) Y_2 Y_3 + Y_4 (Y_1 + Y_2 + Y_3)}$$

Find Butterworth first order Active Low Pass filter:



By comparing the above circuit with Sallen key model,

$$Z_1 = R$$

$$Z_2 = R$$

$$Z_3 = 1/sC$$

$$Z_4 = 1/sC$$

$$Y_2 = 1/R$$

$$Y_3 = sC$$

$$Y_4 = sC$$

$$\frac{V_o(s)}{V_{in}(s)} = \frac{\frac{1}{R} \cdot \frac{1}{R} \cdot A_0}{\frac{1}{R^2} + \frac{sC}{R}(1-A_0) + \frac{sC}{R} + \frac{sC}{R} + s^2C^2}$$

$$= \frac{A_0}{R^2} \cdot \frac{1}{\frac{1}{R^2} + \frac{sC}{R}(1-A_0) + \frac{2sC}{R} + s^2C^2}$$

$$= \frac{A_0/R^2}{\frac{1}{R^2} + \frac{sC}{R}(1-A_0) + \frac{2sC}{R} + s^2C^2}$$

$$= \frac{A_0/R^2}{\frac{1}{R^2} \left[1 + sCR(1-A_0) + sCR(2 + sCR) \right]}$$

$$\frac{V_o(s)}{V_{in}(s)} = \frac{A_0}{1 + sCR(1-A_0) + sCR(2 + sCR)}$$

$$= \frac{A_0}{1 + sCR(1-A_0) + 2sCR + s^2C^2R^2}$$

$$= \frac{A_0}{s^2C^2R^2 + 3sCR - A_0sCR + 1}$$

$$= \frac{A_0}{(sCR)^2 + sCR(3-A_0) + 1}$$

In frequency domain,

$$\frac{V_o(f)}{V_{in}(f)} = \frac{-A_0}{(j2\pi fCR)^2 + (j\omega RC)(3-A_0) + 1}$$

$$= \frac{A_0}{1 - (2\pi fRC)^2 + j2\pi fRC(3-A_0)}$$

$$\left| \frac{V_o(f)}{V_{in}(f)} \right| = \frac{A_0}{\sqrt{(1 - (2\pi fRC)^2)^2 + (2\pi fRC(3 - A_0))^2}}$$

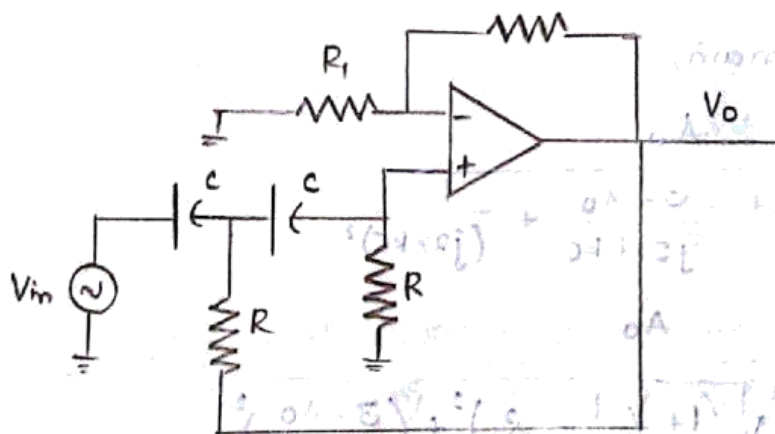
$$\text{Let } f_h = \frac{1}{2\pi RC},$$

$$\begin{aligned} \frac{V_o(f)}{V_{in}(f)} &= \frac{A_0}{\sqrt{(1 - (2\pi fRC)^2)^2 + (2\pi fRC(3 - A_0))^2}} \\ &= \frac{A_0}{\sqrt{[1 - (f/f_h)^2]^2 + [(3 - A_0)^2 (f/f_h)^2]}} \end{aligned}$$

$$\text{At } f = 0, \quad \frac{V_o(f)}{V_{in}(f)} = A_0$$

$$\text{At } f = \infty, \quad \frac{V_o(f)}{V_{in}(f)} = 0.$$

BUTTERWORTH 2nd ORDER ACTIVE-HIGH PASS FILTER



Comparing the above with the Sallen key model,

$$Z_1 = 1/sC$$

$$Z_3 = R$$

$$Z_2 = 1/sC$$

$$Z_4 = R$$

Due to negative feedback,

$$V_1 = V_2$$

$$Y_1 = sC$$

$$Y_2 = sC$$

$$Y_3 = 1/R$$

$$Y_4 = 1/p$$

$$\begin{aligned} \frac{V_o(s)}{V_{in}(s)} &= \frac{(sC)^2 A_o}{(sC)^2 + (1-A_o) \frac{sC}{R} + \frac{1}{R} (sC + sC + \frac{1}{R})} \\ &= \frac{(sC)^2 A_o}{(sC)^2 + (1-A_o) \frac{sC}{R} + \frac{1}{R} (2sC + \frac{1}{R})} \\ &= \frac{(sC)^2 A_o}{(sC)^2 + (3-A_o) \frac{sC}{R} + \frac{1}{R^2}} \\ &= \frac{A_o}{1 + \left(\frac{3-A_o}{sCR} \right) + \frac{1}{(sCR)^2}} \end{aligned}$$

In frequency domain,

$$\frac{V_o(f)}{V_{in}(f)} = \frac{A_o}{1 + \frac{3-A_o}{j2\pi fRC} + \frac{1}{(j2\pi fRC)^2}}$$

$$\left| \frac{V_o(f)}{V_{in}(f)} \right| = \frac{A_o}{\sqrt{\left(1 + \left(\frac{1}{j2\pi fRC}\right)^2\right)^2 + \left(\frac{3-A_o}{2\pi fRC}\right)^2}}$$

The quantity, $f_B = \frac{1}{2\pi RC}$

$$= \frac{A_o}{\sqrt{1 + \left(\frac{1}{\pi RC}\right)^2 + \left(\frac{3-A_o}{2\pi fRC}\right)^2}}$$

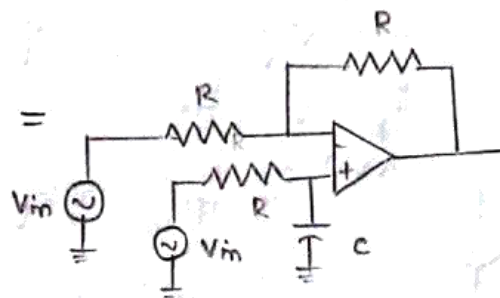
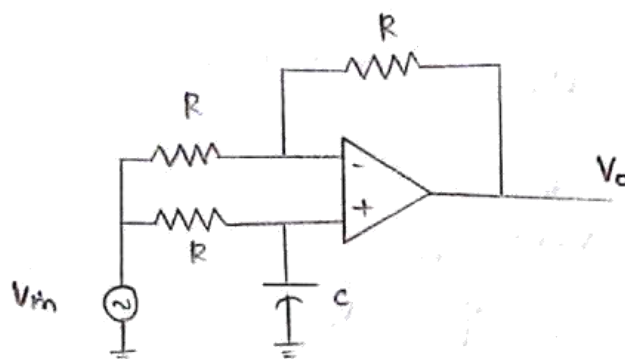
$$= \frac{1 - j(3 - A_0)}{2\pi fRC} + \frac{-1}{(2\pi fRC)^2}$$

$$= \left| \frac{V_o(f)}{V_{in}(f)} \right| = \frac{A_0}{\sqrt{\left(1 - \frac{1}{(2\pi fRC)^2}\right)^2 + \left(\frac{3 - A_0}{2\pi fRC}\right)^2}}$$

Let $f_L = \frac{1}{2\pi RC}$

$$\left| \frac{V_o(f)}{V_{in}(f)} \right| = \frac{A_0}{\sqrt{\left[1 - \left(\frac{f_L}{f}\right)^2\right]^2 + \left[3 - A_0 \cdot \left(\frac{f_L}{f}\right)^2\right]^2}}$$

ALL PASS FILTER:

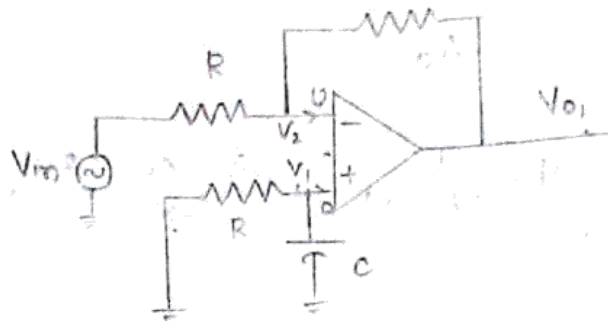


According to the superposition theorem,

In an LTI system consisting of more one source, the total response at one element is equal to algebraic sum of individual responses.

Two cases are obtained,

- i) Output V_{o1}
- ii) Output V_{o2}



for negative feedback,

$$V_1 = V_2$$

Since $V_1 = 0$,

$$V_1 = V_2 = 0$$

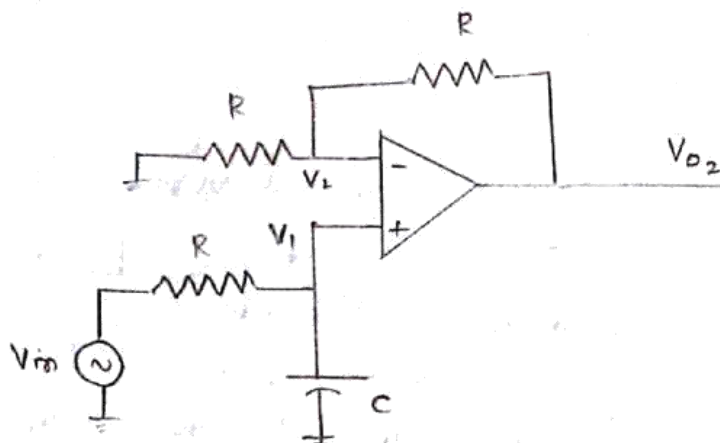
Applying nodal analysis at inverting terminal,

$$\frac{V_2 - V_m}{R} + \frac{V_2 - V_{o1}}{R} = 0$$

$$\therefore V_2 = 0$$

$$V_{o1} = -V_m$$

Case (ii)



Applying voltage divider rule at V_1 ,

$$V_1 = V_m(s) \cdot \frac{1/sC}{1/sC + R}$$

$$= \frac{V_m(s)}{1 + sCR}$$

for negative feedback,

$$V_1 = V_2$$

$$\frac{V_2 - 0}{R} + \frac{V_2 - V_{O2}}{R} = 0$$

$$V_{O2} = RV_2$$

$$V_{O2} = \frac{2}{1+sCR} \cdot V_{in}(s)$$

Total Response,

$$V_o = V_{O1} + V_{O2}$$

$$= -V_{in}(s) + \frac{2}{1+sCR} \cdot V_{in}(s)$$

$$\frac{V_o(s)}{V_{in}(s)} = -1 + \frac{2}{1+sCR}$$

$$= \frac{-1+sCR+2}{1+sCR}$$

$$= \frac{1-sCR}{1+sCR}$$

In frequency domain,

$$\frac{V_o(f)}{V_{in}(f)} = \frac{1-j2\pi fRC}{1+j2\pi fRC}$$

$$\left| \frac{V_o(f)}{V_{in}(f)} \right| = \frac{\sqrt{1+(2\pi fRC)^2}}{\sqrt{1+(2\pi fRC)^2}}$$

$$= 1$$

$$\angle \frac{V_o(f)}{V_{in}(f)} = \tan^{-1}(-2\pi fRC) - \tan^{-1}(2\pi fRC)$$

$$\tan^{-1}(-0) = -\tan^{-1}(0)$$

$$= -\tan^{-1}(2\pi fRC) - \tan^{-1}(2\pi fRC)$$

$$= -2\tan^{-1}(2\pi fRC)$$

$$f \rightarrow 0 \text{ (d.c signal)} \rightarrow \angle \frac{V_o(f)}{V_{in}(f)} = 0$$

$$f \rightarrow \infty \text{ (a.c signal)} \rightarrow \angle \frac{V_o(f)}{V_{in}(f)} = -180^\circ$$

The gain magnitude is 1, i.e., independent of the frequency, so, output is equal to input. But, a phase change exists between the input and output based on the input signal frequency.

It can generate -180° to 0° phase shift between the output and input, i.e., input leads the output.

BAND PASS FILTER:

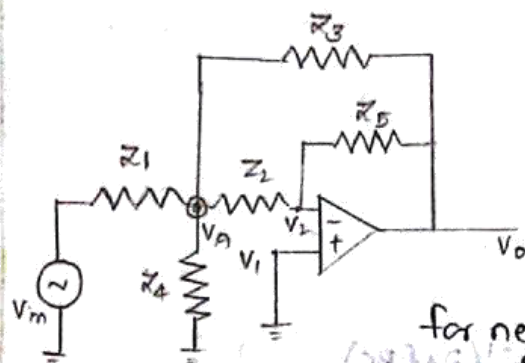
28-09-15

- Narrow Band Pass (B.W is less) $Q > 10$
- Wide Band Pass (B.W is more) $Q < 10$

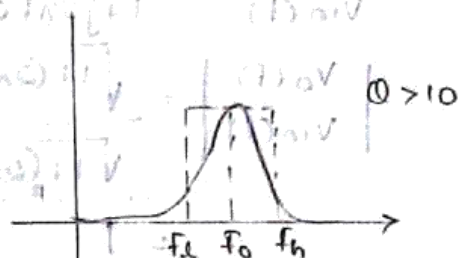
$$Q = \frac{f_0}{\text{B.W}} = \frac{f_0}{f_h - f_l} \quad \text{where } f_0 = \sqrt{f_h f_l}$$

$\downarrow$ Quality factor $\downarrow$ Centre frequency

NARROW BAND PASS FILTER



for negative feedback, $V_1 = V_2$



Nodal analysis at node voltage V_A ,

$$\frac{V_A - V_m}{Z_1} + \frac{V_A - V_2}{Z_2} + \frac{V_A - 0}{Z_4} + \frac{V_A - V_0}{Z_3} = 0$$

But $V_2 = 0$,

$$V_A \left[\frac{1}{Z_1} + \frac{1}{Z_2} + \frac{1}{Z_3} + \frac{1}{Z_4} \right] - \frac{V_m}{Z_1} - \frac{V_0}{Z_3} = 0$$

Applying nodal analysis at inverting node,

$$\frac{V_2 - V_A}{Z_2} + \frac{V_2 - V_0}{Z_5} + 0 = 0$$

But $V_2 = 0$,

$$-V_A \cdot Y_2 = V_0 Y_5$$

$$V_A = -\frac{Y_5}{Y_2} \cdot V_0 \rightarrow (2)$$

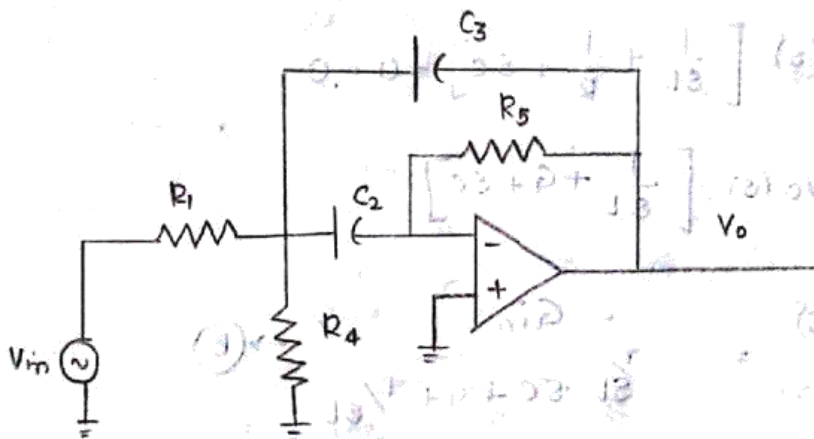
from (1) and (2),

$$-\frac{Y_5}{Y_2} \cdot V_0 [Y_1 + Y_2 + Y_3 + Y_4] = V_{in} Y_1 + V_0 Y_3$$

$$-V_0 Y_5 [Y_1 + Y_2 + Y_3 + Y_4] = V_{in} (Y_1 Y_2) + V_0 (Y_3 Y_2)$$

$$-V_0 [Y_2 Y_3 + Y_5 (Y_1 + Y_2 + Y_3 + Y_4)] = V_{in} (Y_1 Y_2)$$

$$\frac{V_0}{V_{in}} = \frac{-Y_1 Y_2}{Y_2 Y_3 + Y_5 (Y_1 + Y_2 + Y_3 + Y_4)}$$



$$Z_1 = R_1 \quad Z_2 = \frac{1}{sC_2} \quad Z_3 = \frac{1}{sC_3} \quad Z_4 = R_4 \quad Z_5 = R_5$$

$$Y_1 = G_1 \quad Y_2 = sC_2 \quad Y_3 = sC_3 \quad Y_4 = G_4 \quad Y_5 = G_5$$

$$\frac{V_o}{V_{in}} = \frac{-G_1 G_5}{(sG_2)(sG_3) + G_5 [G_1 + sG_2 + sG_3 + G_4]}$$

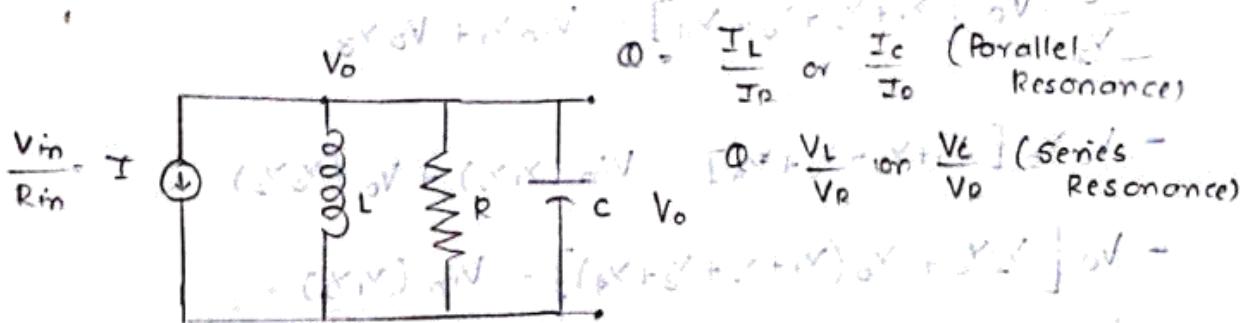
$$= \frac{-G_1 \cdot sG_2}{sG_2 \cdot sG_3 + G_1 G_5 + sG_2 \cdot G_5 + G_5 \cdot sG_3 + G_4 G_5}$$

Dividing with sG_2 ,

$$= \frac{-G_1 \cdot sG_2}{sG_3 + G_5 \left[1 + \frac{G_3}{G_2}\right] + \frac{G_5}{sG_2} [G_1 + G_4]}$$

→ (A)

RLC Parallel Circuit:



Applying Nodal Analysis,

$$I + \frac{V_o(s)}{sL} + \frac{V_o(s)}{R} + \frac{V_o(s)}{1/sC} + 0 = 0 \quad \text{Open circuit}$$

$$\frac{V_{in}}{R_{in}} + V_o(s) \left[\frac{1}{sL} + \frac{1}{R} + sC \right] + 0 = 0$$

$$\frac{V_{in}}{R_{in}} = -V_o(s) \left[\frac{1}{sL} + G + sC \right]$$

$$\frac{V_{in}}{V_o(s)} \cdot \frac{V_o(s)}{V_{in}(s)} = \frac{-G_{in}}{sL \cdot sC + G + 1/sL} \quad \rightarrow (B)$$

Resonance (Central): $\omega_0 = \frac{1}{\sqrt{LC}}$

$$\text{Max. Gain} \left| \frac{V_o}{V_{in}} \right| = \frac{-G_{in}}{G}$$

Quality factor, $Q_0 = \frac{R}{\omega_0 L} = \omega_0 RC$
 Bandwidth = $\frac{f_0}{Q}$ [$\therefore Q = f_0/B.W$].

On comparison with (A) and (B), (the transfer function of RLC Parallel circuit)
 we get.

$$G_{in} = G_1$$

$$G = G_5 \left[1 + \frac{C_3}{C_2} \right]$$

$$C = C_3$$

$$L = \frac{C_2}{G_5 [G_1 + G_4]}$$

Resonant frequency, $\omega_0 = \frac{1}{\sqrt{LC}}$

$$= \frac{1}{\sqrt{\frac{C_2}{G_5 (G_1 + G_4)} \cdot C_3}} = \sqrt{\frac{G_5 (G_1 + G_4)}{C_2 C_3}}$$

Maximum Gain, $A_0 = \left| \frac{V_o}{V_{in}} \right|$

$$= -\frac{G_{in}}{G} = \frac{-G_1}{G_5 \left[1 + \frac{C_3}{C_2} \right]} = \frac{-G_1 C_2}{G_5 (C_2 + C_3)}$$

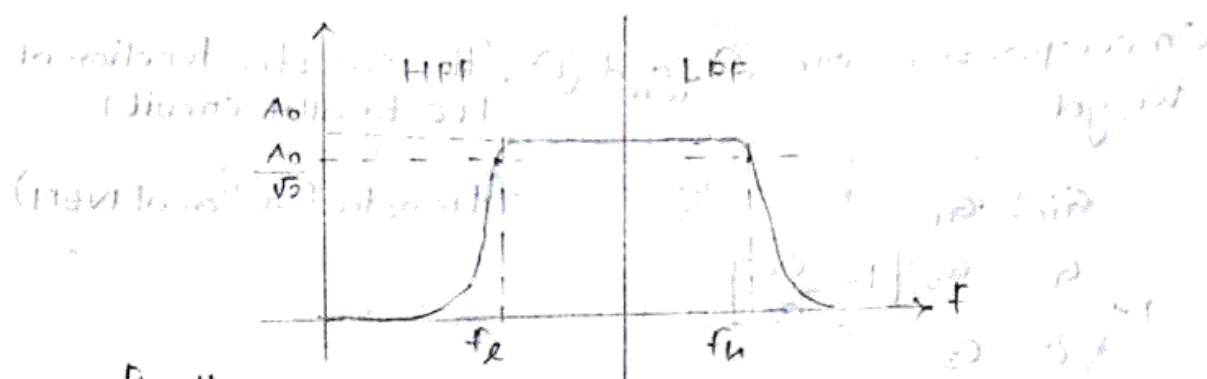
Quality factor, $Q = \frac{R}{\omega_0 L} = \frac{1}{\omega_0 GL}$

$$= \frac{1}{\sqrt{\frac{G_5 (G_1 + G_4)}{C_2 C_3}} \cdot \left[\frac{C_2 + C_3}{C_2} \right] \cdot \frac{C_2}{G_5 [G_1 + G_4]}}$$

$$= \frac{\sqrt{(G_1 + G_4) (C_2 C_3)}}{\sqrt{G_5} (C_2 + C_3)}$$

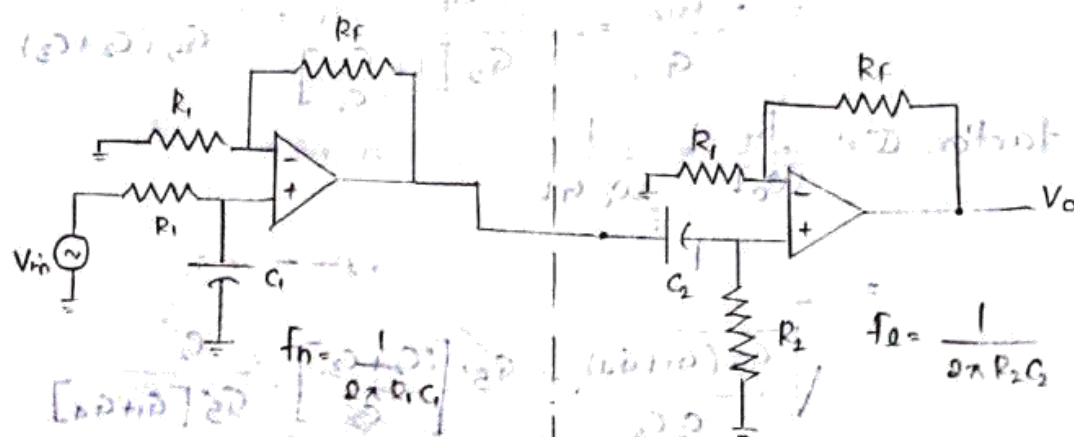
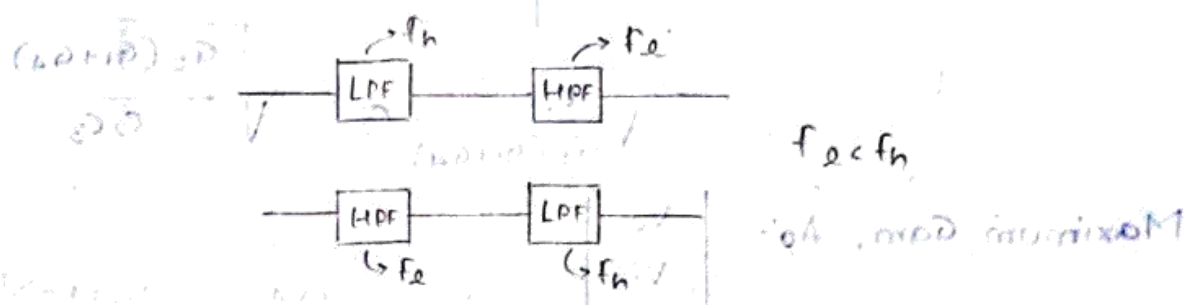
Bandwidth, $= \frac{f_0}{Q} = \frac{\omega_0}{2\pi Q}$

WIDE BAND PASS FILTER:



By the cascade connection of LPF and HPF, we can design the band pass filter.

But the condition is HPF cutoff frequency (f_L) should be lesser than LPF cutoff frequency.



Condition: $f_L < f_H$

$$\frac{1}{2\pi R_1 C_F} < \frac{1}{2\pi R_2 C_2}$$

$$R_1 C_1 < R_2 C_2$$

↓ LPF ↓ HPF

$$\left| \frac{V_o}{V_{o1}} \right| = \left| \frac{V_{o1}}{V_{in}} \right|$$

$$\left| \frac{V_o}{V_{in}} \right| = \underbrace{\left| \frac{V_o}{V_{o1}} \right|}_{\text{HPF}} \underbrace{\left| \frac{V_{o1}}{V_{in}} \right|}_{\text{LPF}}$$

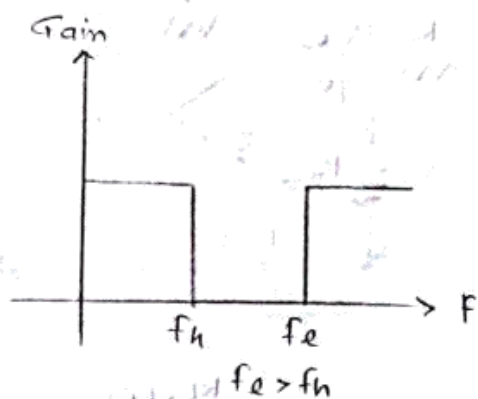
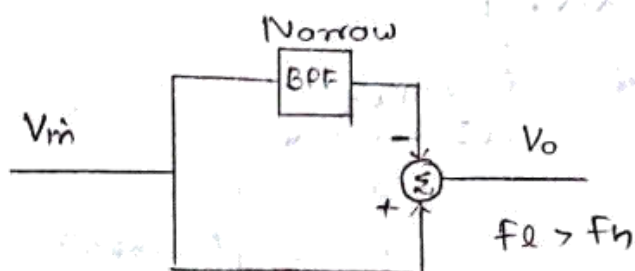
$$\left| \frac{V_o}{V_{in}} \right| = \frac{A_o}{\sqrt{1 + (f_l/f)^2}} \cdot \frac{A_o}{\sqrt{1 + (f/f_h)^2}}$$

$$= \frac{A_o^2}{\sqrt{\left(1 + \left(\frac{f_l}{f}\right)^2\right) \left(1 + \left(\frac{f}{f_h}\right)^2\right)}}$$

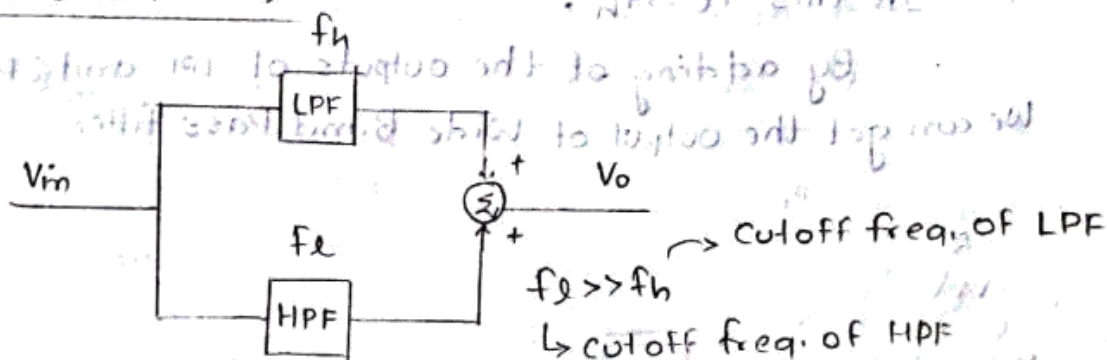
(Max gain = A_o^2
 $A_o = 1 + \frac{R_f}{R_i}$)

BAND REJECT FILTER:

For Narrow BRF,



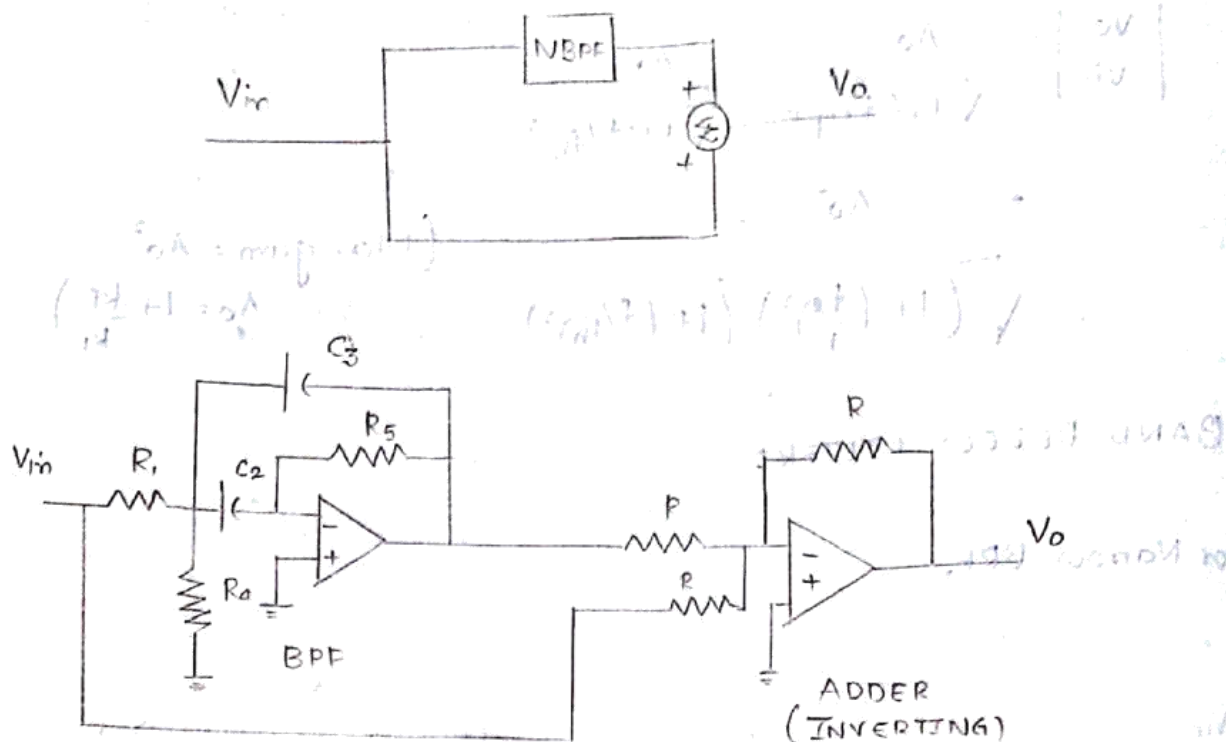
for ~~Narrow~~ Wide BRF,



Narrow Band Reject filter:

for this $f_l > f_h$, but f_l is closer to f_h . To design this, we are using the Band pass filter, i.e. by subtracting the band pass filter output from the input, we can design the band reject filter.
 But in this, the maximum gain of Band Pass Filter should be '1'.

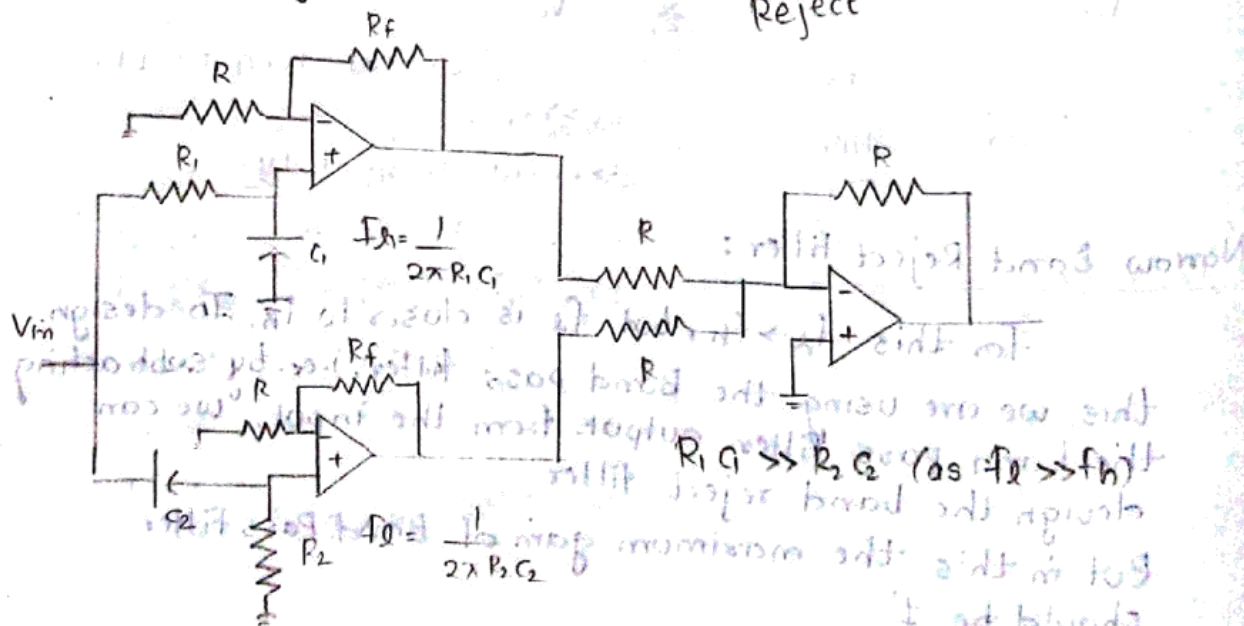
But NBF filter output is negative (Gain)
So, instead of subtracting from the input, we are adding the NBF output to the input.



REJECT WIDE BAND PASS FILTER:

In this $f_l \gg f_h$,

By adding of the outputs of LPF and BPF, we can get the output of Wide Band Pass filter.



4. 555 TIMER

- 555 timer is mainly used to generate accurate time delays or oscillations
- It can give time delay for microseconds and to hours
- first manufactured by Signetics Corporation

SE 555 / NE 555

- It can work in a supply range +5V to +18V and can drive load upto 200mA.
- It can be designed with TTL and CMOS logic circuits.
- Applications are :
 - Oscillator
 - Pulse Generator
 - Ramp and Square Wave Generator
 - Mono-shot Multivibrator
 - Burglar Alarm
 - Traffic light control
 - Voltage Monitor

- Temperature Range:

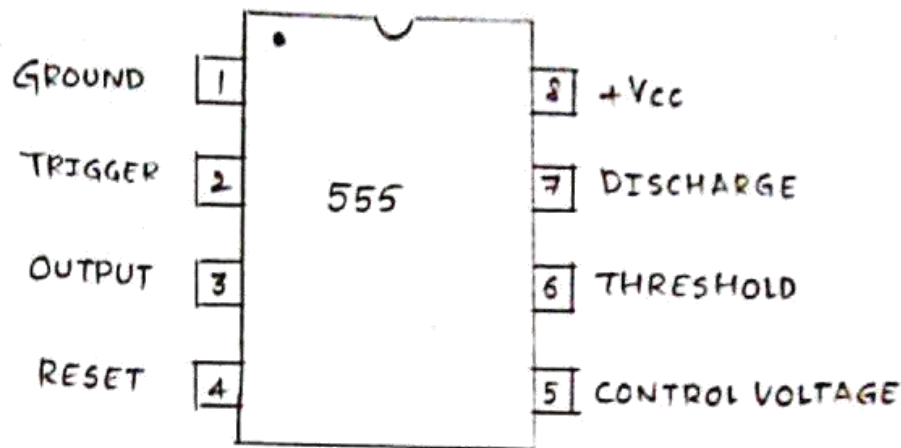
SE 555 : -55°C to 125°C

NE 555 : 0 to 70°C

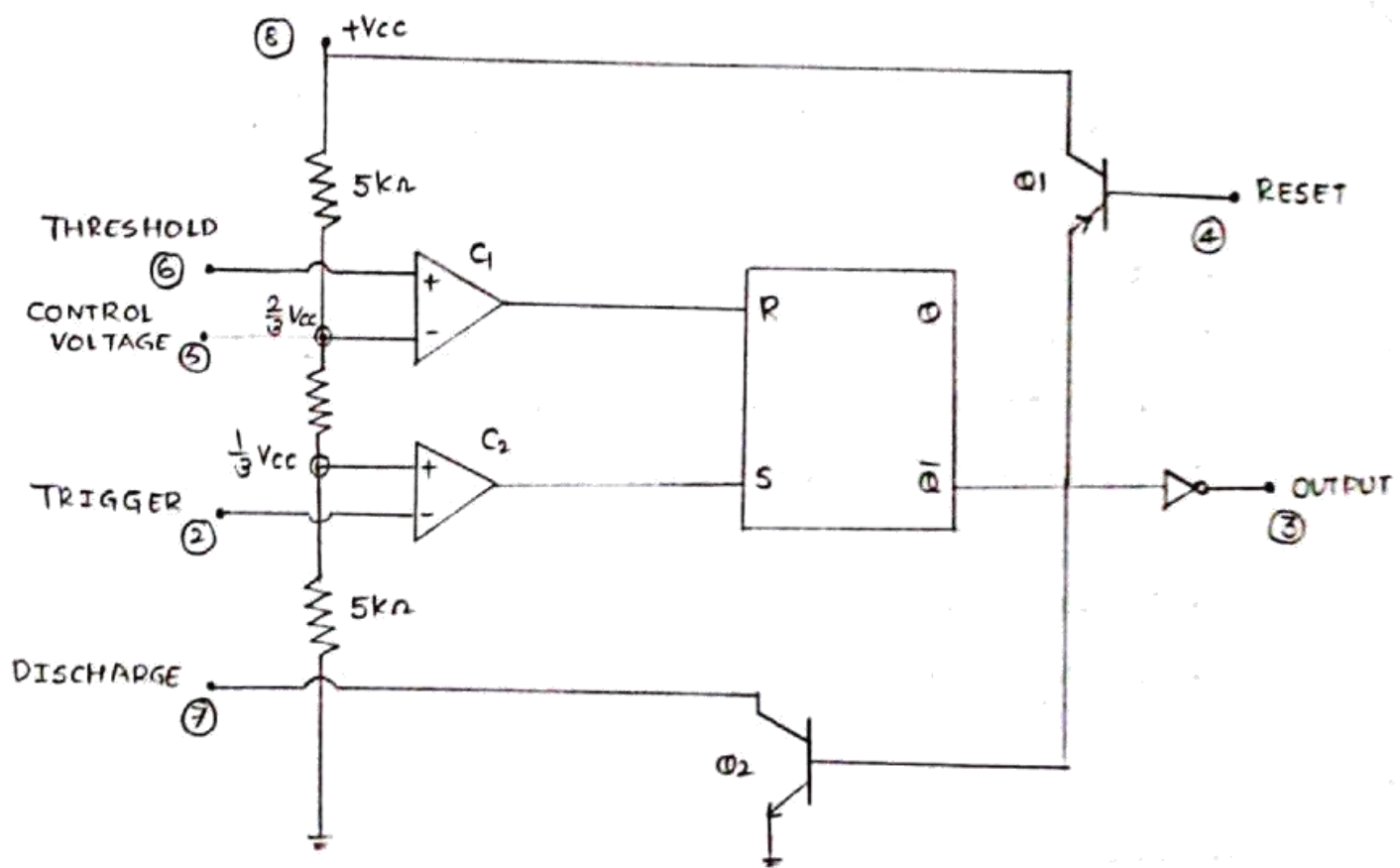
- Functional Diagram

Internally, it consists of 3 Resistors ($5k\Omega$), 2 Comparators, 1 SR flip flop, 1 Inverter, 1 npn transistor, 1 PNP transistor.

555 timer basically consists of 8 pins (I_c)



INTERNAL STRUCTURE:



FUNCTIONALITY OF EACH BLOCK:

• Comparator - 1 : C1

This compares input voltages threshold and $\frac{2}{3} V_{cc}$
Output is R. So,

$$R = \begin{cases} 1 & \text{Threshold} > \frac{2}{3} V_{cc} \\ 0 & \text{Threshold} < \frac{2}{3} V_{cc} \end{cases}$$

• Comparator 2 : c2

This compares input voltages $\frac{1}{3}V_{cc}$ and trigger.

Output is S. So,

$$S = \begin{cases} 1 & \frac{1}{3}V_{cc} > \text{trigger} \\ 0 & \frac{1}{3}V_{cc} < \text{trigger} \end{cases}$$

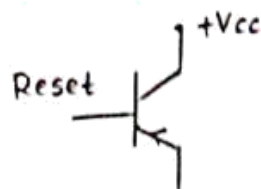
• Flip Flop

S	R	Q_n	$\bar{Q}_n$
0	0	Prev	Prev
0	1	0	1
1	0	1	0
1	1	—	—

- In 555 timer, output is connected to $\bar{Q}$ of SR flip flop through inverter. So,

$$\boxed{O/p = Q}$$

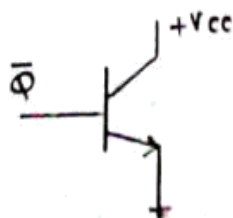
• PNP Transistor : Q_1



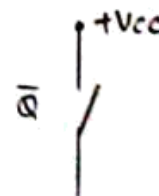
IF Reset = 0 Q_1 is ON
 = 1 Q_1 is OFF



• NPN Transistor : Q_2



IF $\bar{Q} = 0$, Q_2 is OFF
 = 1, Q_2 is ON



- IF RESET = Low [0], then Q_1 is ON so, output = Low
 $\bar{Q}$ = HIGH so, Q_2 is ON. so, discharge terminal is connected to ground.

- So, if RESET = 0, Output = 0, If RESET = HIGH [1], then normal operation will be continued [i.e. output depends on inputs]
So, RESET is connected to Vcc pin
- Control Voltage [5th pin] is used for noise cancellation. For this, 0.01μF capacitor is connected in between 3rd and 1st terminals, i.e. ground.

555 TIMER AS SCHMITT TRIGGER:

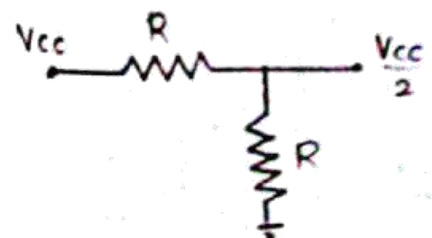
- Our 555 timer is comparing the input signal threshold and trigger with $\frac{2}{3}V_{cc}$ and $\frac{1}{3}V_{cc}$ respectively, i.e. both are +ve voltages.
- If we apply a perfect AC signal, (sinusoidal), then it consists +ve and -ve values. But 555, thresholds are +ve. So, if we apply this perfect AC to Schmitt [555], there might not be perfect output.
- For this, we are adding a dc voltage [which is equal to the average of two thresholds]

$$\frac{\frac{1}{3}V_{cc} + \frac{2}{3}V_{cc}}{2} = \frac{V_{cc}}{2}$$

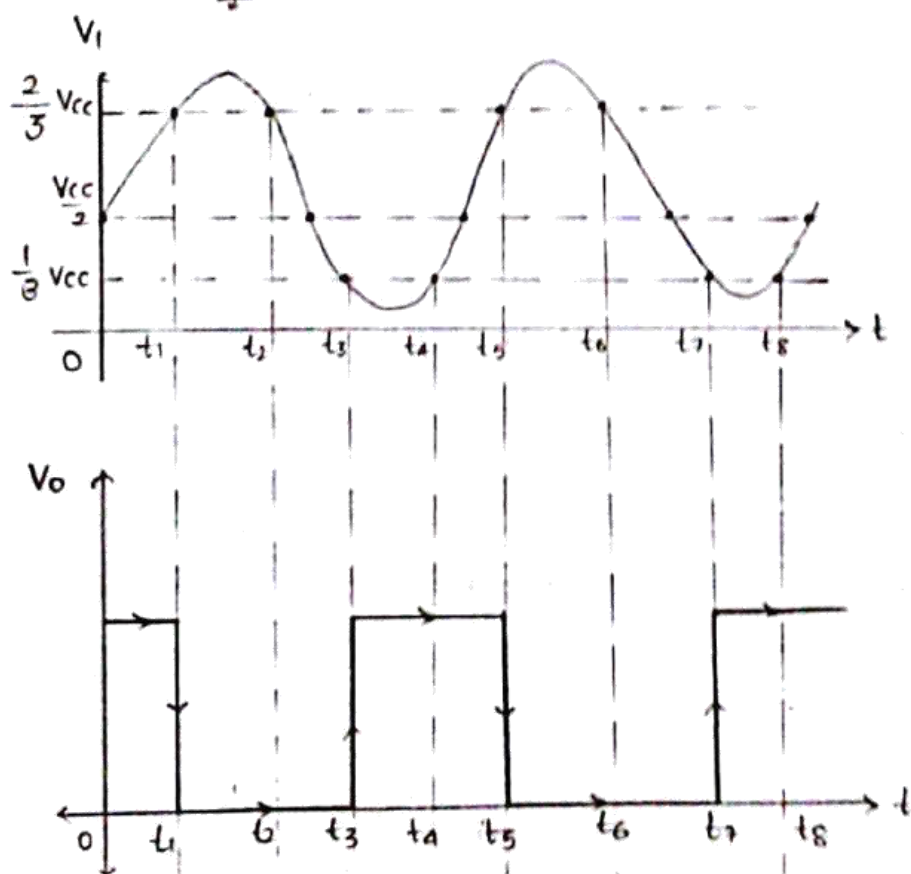
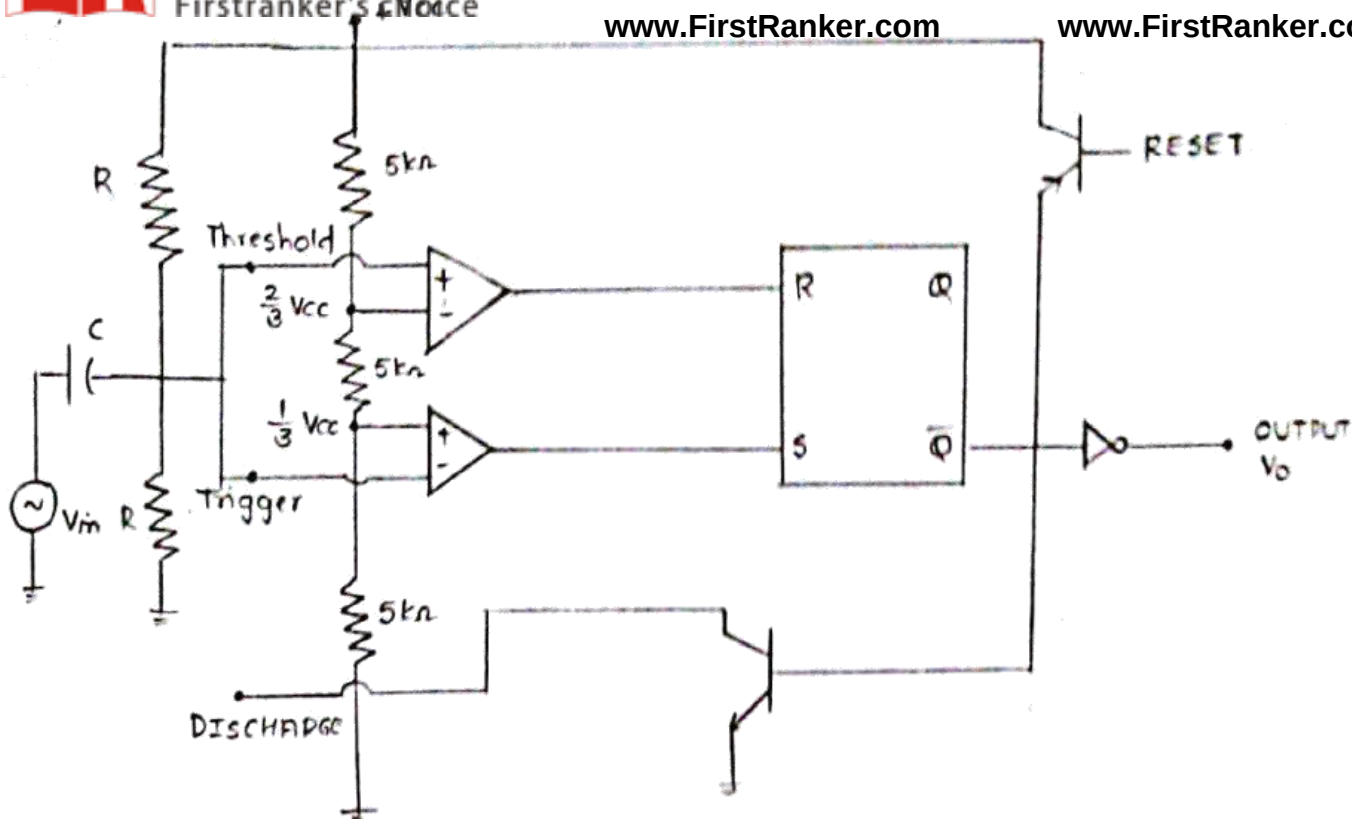
- Then, we are connecting this signal to the threshold and trigger inputs. We are not connecting discharge terminal to any element.

$$V_i = V_{in}(AC) + \frac{V_{cc}}{2}$$

We are adding $\frac{V_{cc}}{2}$ by using voltage divider and we are connecting input signal through a capacitor to filter unwanted dc term in input.



$$V_i = \text{threshold} = \text{trigger}$$



First plot input signal V_i and indicate thresholds $\left[\frac{V_{CC}}{3} \text{ and } \frac{2V_{CC}}{3}\right]$ then mark the intersection point between input signal and thresholds. Then indicate time slots. In between time slots, compare the input with the thresholds and plot output.

OPERATION:

- Initially, output of 555 timer is high [1]
- from 0 to t_1 ,

$V_1 < \frac{2}{3} V_{cc}$	$R = 0$	Output = Φ = Prev = High
$V_1 > \frac{1}{3} V_{cc}$	$S = 0$	
- t_1 to t_2

$V_1 > \frac{2}{3} V_{cc}$	$R = 1$	Output = $\Phi = 0$
$V_1 > \frac{1}{3} V_{cc}$	$S = 0$	
- t_2 to t_3

$V_1 < \frac{2}{3} V_{cc}$	$R = 0$	Output = Φ = Prev = Low = 0
$V_1 > \frac{1}{3} V_{cc}$	$S = 0$	
- t_3 to t_4

$V_1 < \frac{2}{3} V_{cc}$	$R = 0$	Output = $\Phi = 1$
$V_1 < \frac{1}{3} V_{cc}$	$S = 1$	
- t_4 to t_5

$V_1 < \frac{2}{3} V_{cc}$	$R = 0$	Output = Φ = Prev = 1
$V_1 > \frac{1}{3} V_{cc}$	$S = 0$	
- t_5 to t_6

$V_1 > \frac{2}{3} V_{cc}$	$R = 1$	Output = $\Phi = 0$
$V_1 > \frac{1}{3} V_{cc}$	$S = 0$	
- t_6 to t_7

$V_1 < \frac{2}{3} V_{cc}$	$R = 0$	Output = Φ = Prev.
$V_1 > \frac{1}{3} V_{cc}$	$S = 0$	

• t_7 to t_8

$$V_i < \frac{2}{3} V_{cc} \quad R=0$$

$$V_i < \frac{1}{3} V_{cc} \quad S=1$$

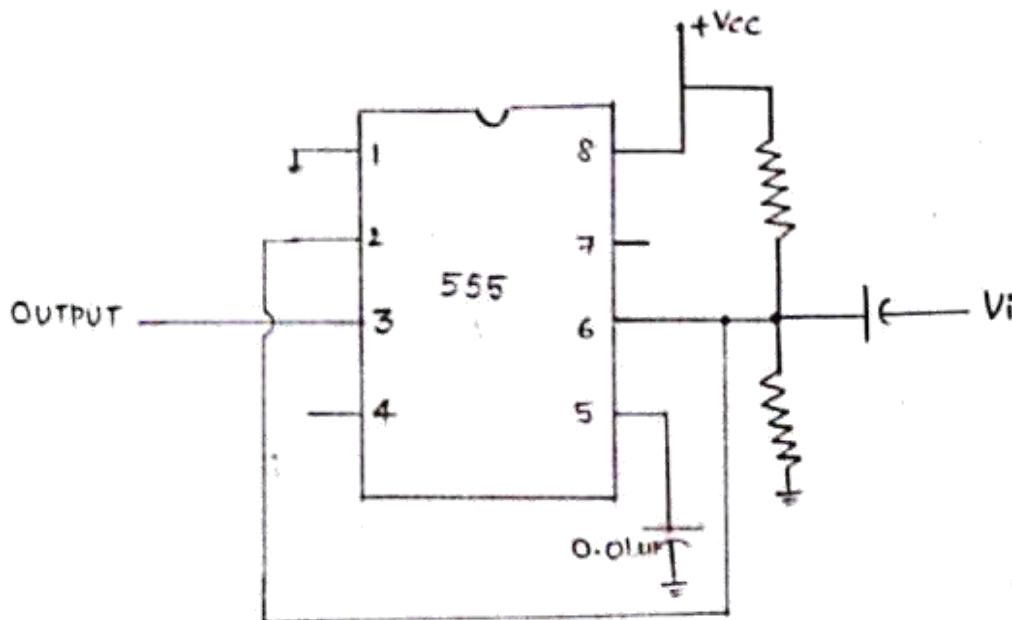
$$\text{Output} = Q=1$$

• Output is a square wave.

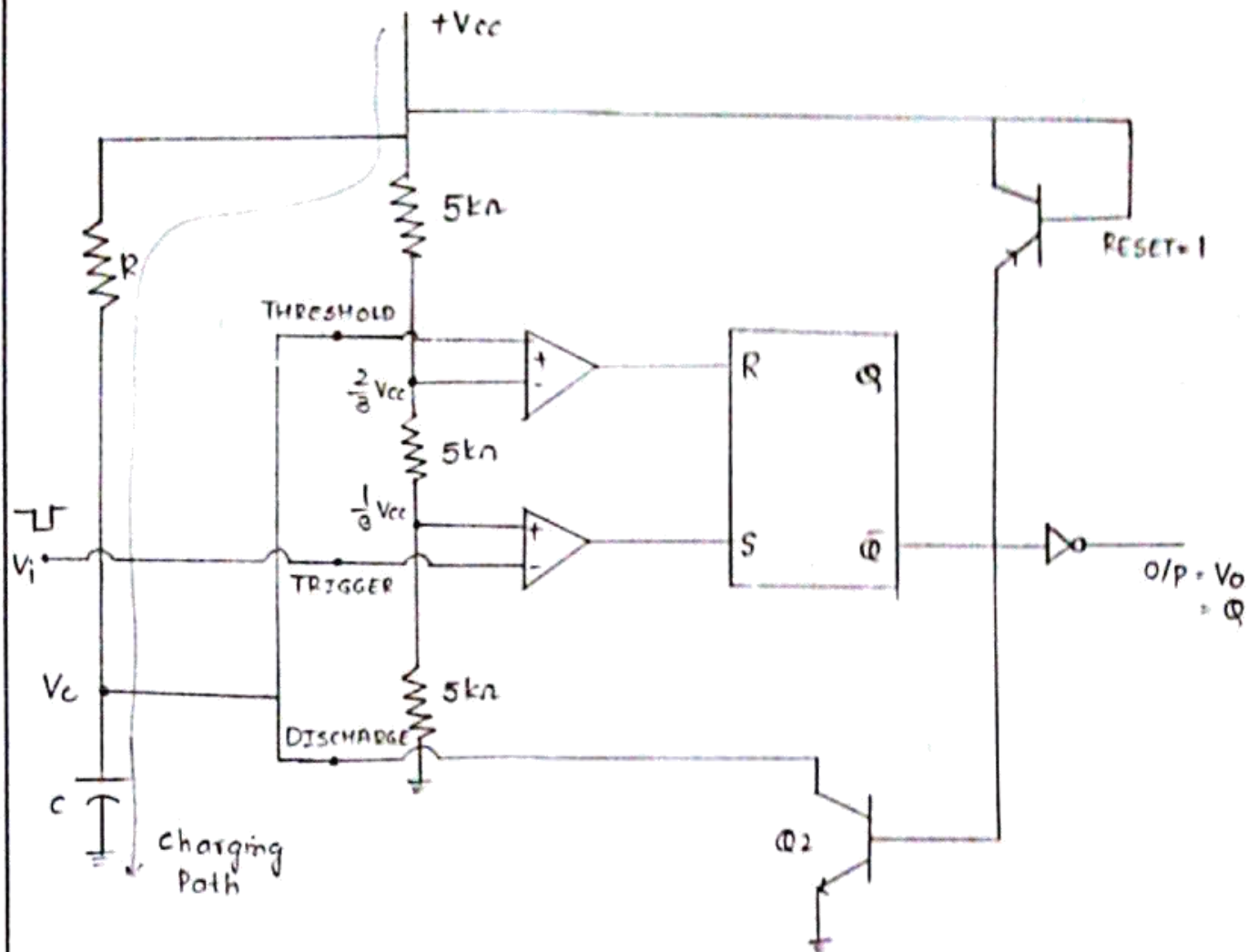
$$\text{i.e., } t_1 = t_2 - t_1 = t_3 - t_2 = t_4 - t_3$$

• If we add a dc voltage other than $\frac{V_{cc}}{2}$ to the input. Then output is not a square wave, it is a rectangular wave

SCHMITT TRIGGER CIRCUIT WITH IC



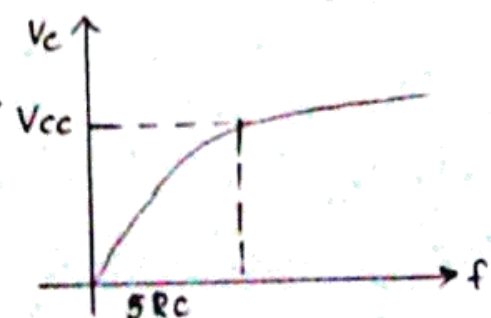
555 TIMER AS MONOSTABLE MULTIVIBRATOR

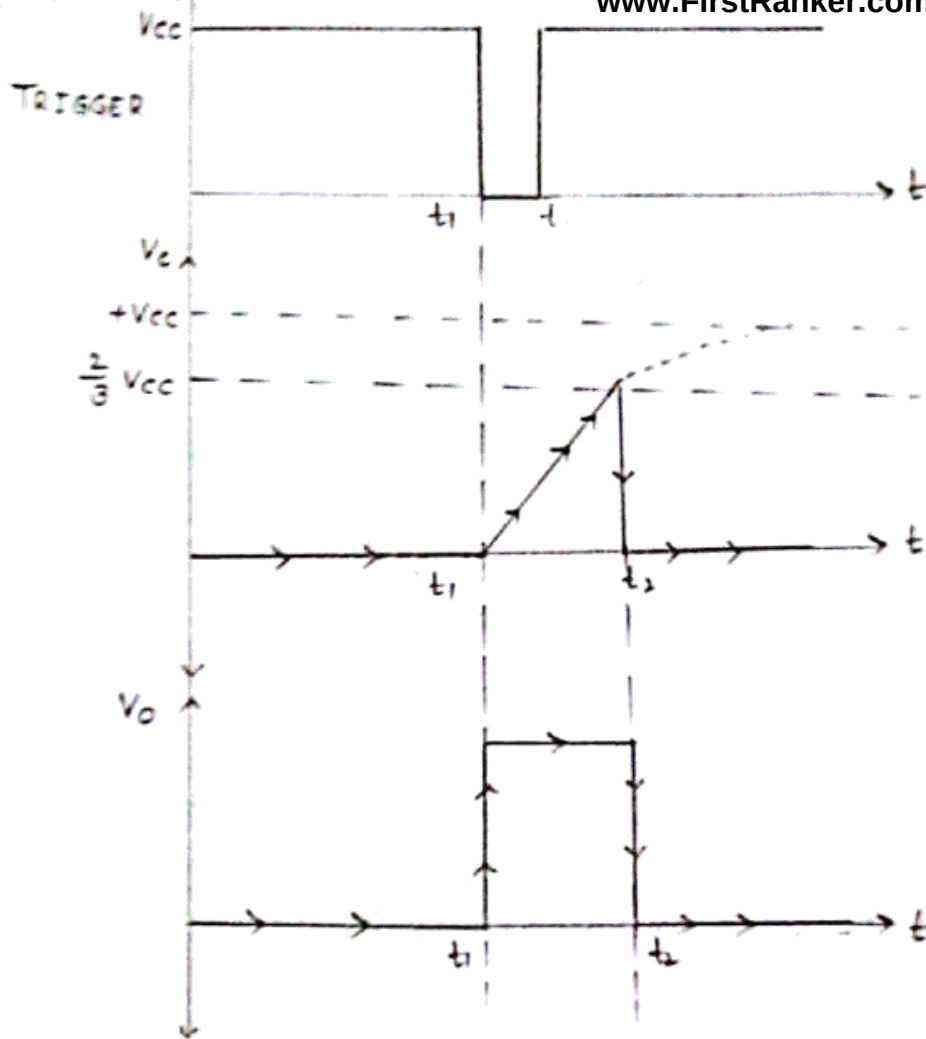


- In this, capacitor voltage is connected to threshold and discharge terminals.
- A negative pulse of limited time period (very less) is applied as input to the trigger input
- Initially,

Capacitor will charge upto maximum applied voltage V_{CC} in exponential path.

After 5 time constants [5RC seconds],
 V_C will be equal to V_{CC}





- Initially, $V_c = 0$ and $\text{Trigger} = V_{cc}$

So,

$$V_c < \frac{2}{3} V_{cc} \quad \text{so, } R=1 \quad \text{Output} = 0 \text{ [Low]}$$

$$\text{Trig} > \frac{1}{3} V_{cc} \quad \text{so, } S=0$$

Output $\phi = 0$, so $\bar{\phi} = 1$ [HIGH] then ϕ_2 will be ON, i.e., capacitor terminal is connected to ground. So, $V_c = 0$

- But, at $t = t_1$, trigger is pressed, i.e., -ve pulse.

So, $\text{trigger} = 0$

$$V_c < \frac{2}{3} V_{cc} \quad R=0 \quad \text{Output} = 1 \text{ [HIGH]}$$

$$\text{Trig} < \frac{1}{3} V_{cc} \quad S=1$$

$\bar{\Phi} = 0$, So Q2 transistor is off, i.e., capacitor is connected to V_{CC} through resistor so it tries to charge upto V_{CC}

But at $t = t_2$,

Capacitor charges upto $\frac{2}{3} V_{CC}$. As time increases, it tries to charge more than $\frac{2}{3} V_{CC}$.

So,

$t = t_2^+$

$$V_C > \frac{2}{3} V_{CC}$$

$$R = 1$$

output = 0 [Low]

$$\text{trigger} = V_{CC}$$

$$S = 0$$

$$> \frac{1}{3} V_{CC}$$

As $\bar{\Phi} = 1$, capacitor is connected to ground. So, V_C becomes zero within short period.

After $t = t_2$, Output will be zero and V_C will be zero until the next trigger is applied.

If applied, then again one pulse exists at the output

PULSE TIME CALCULATION:

from t_1 to t_2 , pulse is ON. In this duration, capacitor is trying to charge from zero to V_{CC} but at $t = t_2$, $V_C = \frac{2}{3} V_{CC}$.

$$\text{Let } t_1 = 0. \quad t_2 - t_1 = \text{Pulse Period} = t_2 = T$$

$$\text{Initial Value} = 0, \quad \text{final Value} = V_{CC} \quad \tau = RC$$

So,

$$V_C(t) = V_F + [V_i - V_F] e^{-t/\tau}$$

$$\begin{aligned} V_C(t) &= V_{CC} + [0 - V_{CC}] e^{-t/RC} \\ &= V_{CC} [1 - e^{-t/RC}] \end{aligned}$$

At $t = t_2$,

$$V_C(t_2) = \frac{2}{3} V_{CC} \quad (\text{We know } t_2 = T)$$

So,

$$\frac{2}{3} V_{CC} = V_{CC} [1 - e^{-t_2/RC}]$$

$$e^{-T/RC} = 1/3$$

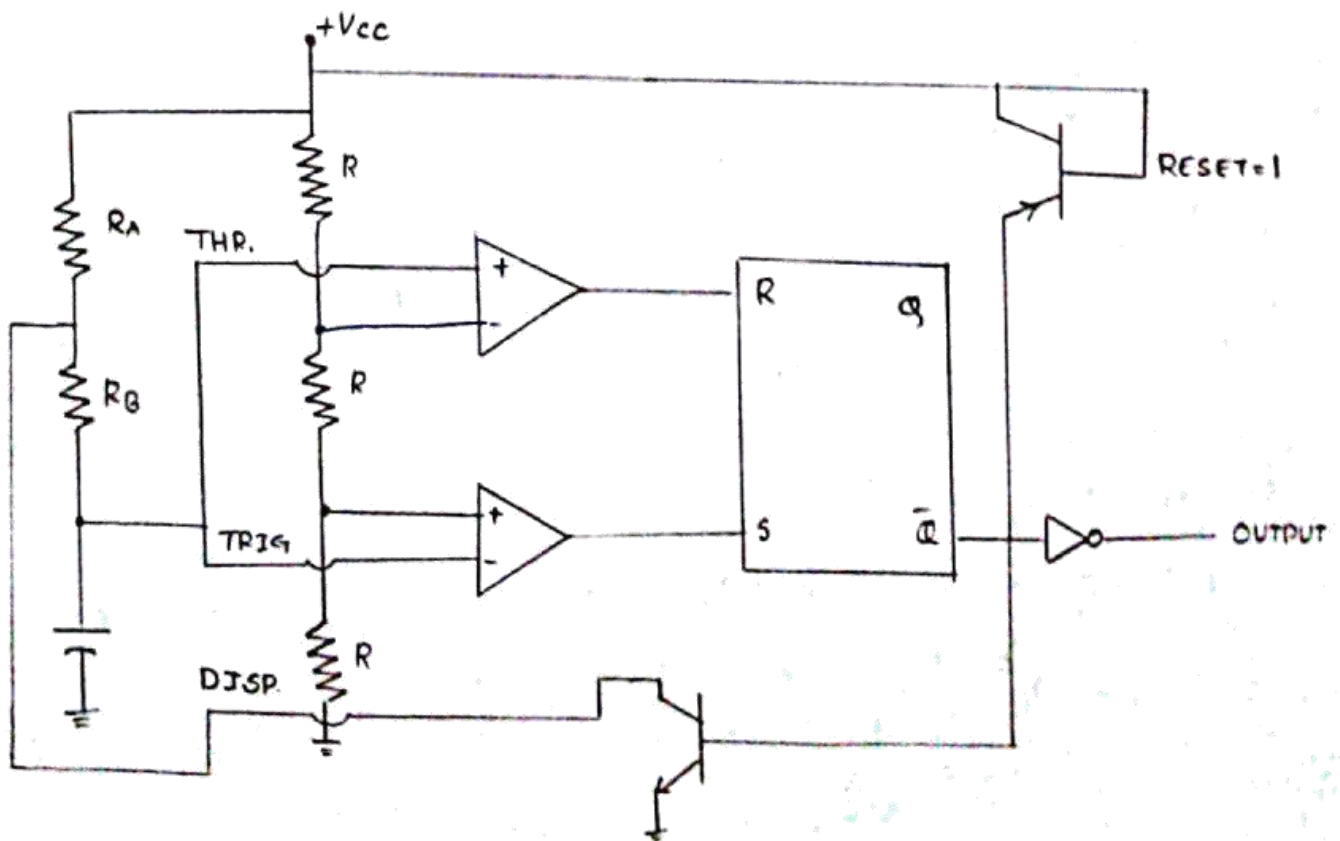
$$T = RC \ln 3$$

$$T = 1.1 RC$$

Applications:

- i) Missing Pulse detector
- ii) Linear Ramp Generator
- iii) Frequency divider
- iv) PWM

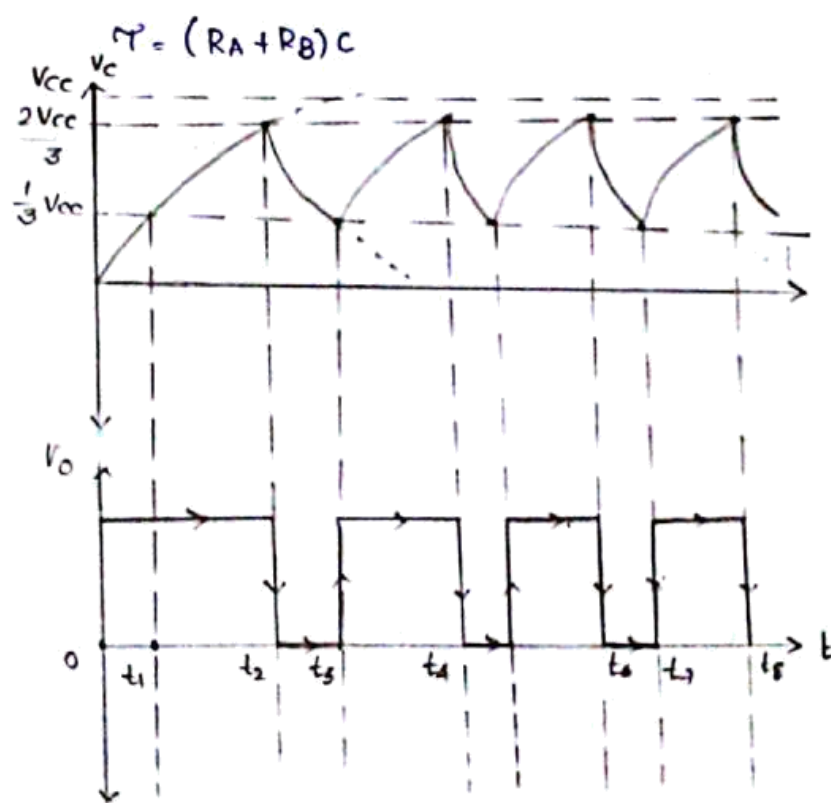
ASTABLE MULTIVIBRATOR:



- A Low pass filter with two resistors and one capacitor output is connected to threshold and trigger terminals
- Discharge terminal is connected in between the two resistors

OPERATION:

- Initially, output of the 555 timer is **HIGH**. So transistor Q2 is ON. Capacitor voltage is zero. So, now it tries to charge up to max. value V_{CC} with time constant.



At $t=t_1$, V_c crosses $\frac{1}{3}V_{CC}$

- At $t=t_1^+$, $V_c > \frac{1}{3}V_{CC}$ and $V_c < \frac{2}{3}V_{CC}$

So, $\text{Thres} < \frac{2}{3}V_{CC}$ $\therefore R=0$

$\text{Trig} > \frac{1}{3}V_{CC}$ $\therefore S=1$

Output = 1 [HIGH]

So, output $\bar{Q}$ = Low, so Q_2 is OFF so capacitor charges.

- At $t = t_2$, capacitor value crosses $\frac{2}{3} V_{CC}$

So, $t = t_2 +$ $V_C > \frac{2}{3} V_{CC}$ $V_C > \frac{1}{3} V_{CC}$

Thresh $> \frac{2}{3} V_{CC}$ $R=1$

$T_{ing} > \frac{1}{3} V_{CC}$ $S=0$

Output = 0 [Low]

So, $\bar{Q}$ is high. So Q_2 transistor is ON. So, capacitor is connected to ground through resistor R_B . It tries to discharge upto 0V. with time constant $\tau = R_C$

- But at $t = t_3$ it tries to cross $\frac{1}{3} V_{CC}$

$V_C < \frac{1}{3} V_{CC}$ and $V_C < \frac{2}{3} V_{CC}$

Thresh $< \frac{2}{3} V_{CC}$ $R=0$

$T_{ing} < \frac{1}{3} V_{CC}$ $PS=1$

Output = 1 [High]

So, $\bar{Q}$ = Low so Q_2 is OFF so capacitor tries to charge upto V_{CC} .

- So, V_C value will not exceed $\frac{2}{3} V_{CC}$ and will not decrease than $\frac{1}{3} V_{CC}$. When capacitor is charging output is high. When capacitor is discharging output is low
- Capacitor is charging with time constant $(R_A + R_B)C$
- Capacitor is discharging with time constant $R_B C$

CALCULATION OF T_{ON} :

$$= t_2 - t_1 = t_4 - t_3 = t_6 - t_5 = \dots$$

While this duration, capacitor is trying to charge upto V_{CC} from $\frac{1}{3} V_{CC}$ with time constant $(R_A + R_B)C$

So,

$$V_i = \frac{1}{3} V_{CC}, V_f = V_{CC} \quad \tau = (R_A + R_B)C$$

$$V_c(t) = V_{CC} + \left(\frac{1}{3} V_{CC} - V_{CC} \right) e^{-t/(R_A + R_B)C}$$

at $t = T_{ON}$

$$= V_c(T_{ON}) = \frac{2}{3} V_{CC}$$

$$\frac{2}{3} V_{CC} = V_{CC} \left[1 - \frac{2}{3} e^{-T_{ON}/(R_A + R_B)C} \right]$$

$$\frac{2}{3} e^{-T_{ON}/(R_A + R_B)C} = \frac{1}{3}$$

$$T_{ON} = (R_A + R_B)C \ln 2$$

$$T_{ON} = 0.69 (R_A + R_B)C$$

CALCULATION OF T_{OFF}

$$t_3 - t_2 = t_5 - t_4 = t_7 - t_6 = \dots$$

While this duration capacitor is discharging from $\frac{2}{3} V_{CC}$ to zero with time constant $R_B C$

$$\text{So, } V_i = \frac{2}{3} V_{CC}, V_f = 0 \quad \tau = R_B C$$

So,

$$V_c(t) = 0 + \left(\frac{2}{3} V_{CC} - 0 \right) e^{-t/R_B C}$$

At $t = T_{OFF}$

$$V_c(T_{OFF}) = \frac{1}{3} V_{CC}$$

$$\frac{1}{3} V_{CC} = \frac{2}{3} V_{CC} \cdot e^{-T_{OFF}/R_B C}$$

$$T_{OFF} = R_B C \ln 2$$

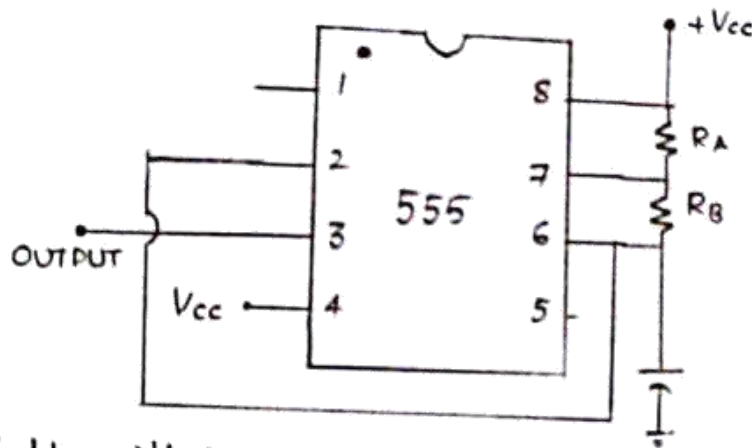
$$T_{OFF} = 0.69 R_B C$$

$$\text{Duty Cycle} = \frac{T_{ON}}{T_{ON} + T_{OFF}} \times 100$$

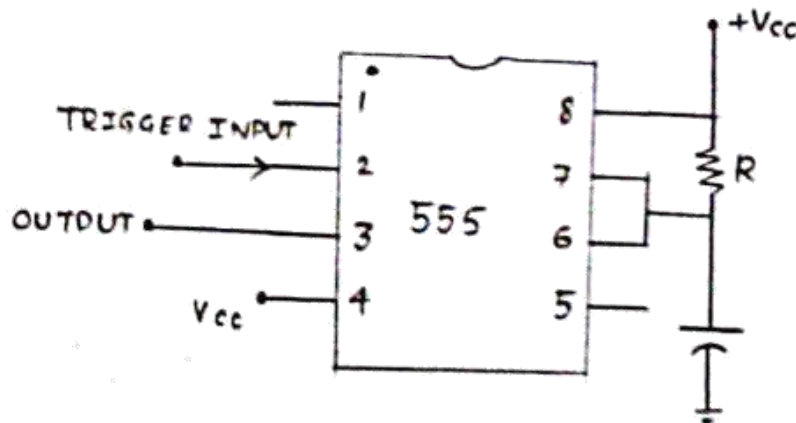
$$= \frac{0.69 (R_A + R_B) C}{0.69 (R_A + 2R_B) C} \times 100$$

$$\% D = \frac{R_A + R_B}{R_A + 2R_B} \times 100$$

Astable Connection to IC:



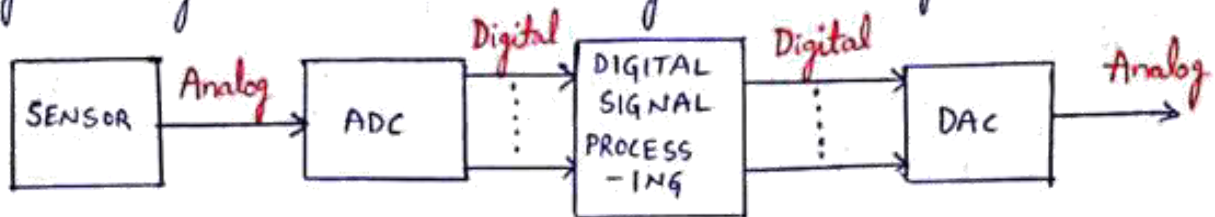
Monostable with 555:



All sensors o/p's are analog in nature but analog signal processing is more complex and costly. IC package density is also less and noise effect on the analog signals is more. The voltage levels in analog is more.

Digital signal is nothing but only two levels either 1 or 0 i.e. high or low. Digital signal processing is very easy and very accurate. IC package density is also very high. Error correction is easy in digital.

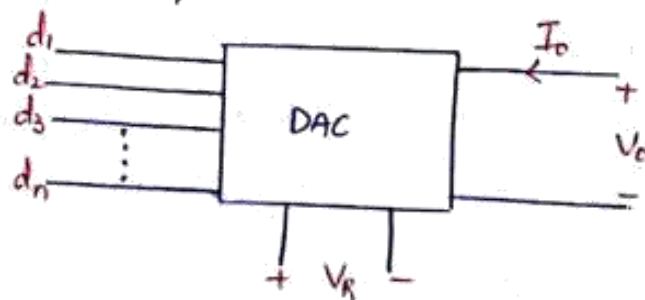
So we prefer digital processing more than analog signal processing. But all sensor o/p's are analog. So, we have to convert this analog signal into digital and process this data. Then we have to again convert digital signal into analog signal. So for this we need ADC and DACs. Analog to Digital converter and Digital to analog converter.



→ DAC

An n -bit digital data is represented as $d_1 d_2 d_3 \dots d_n$
 $\uparrow$ MSB $\uparrow$ LSB

→ Basic DAC Technique:



→ $d_1, d_2, d_3 \dots d_n$ is the digital i/p. d_1 - MSB, d_n - LSB

→ V_o, I_o are o/p voltage and currents

→ V_R - Reference voltage

→ o/p may be represented in terms of voltage or current.

If it is represented in terms of voltage then

$$V_o = K \cdot V_{FS} \left[\frac{d_1}{2} + \frac{d_2}{2^2} + \frac{d_3}{2^3} + \dots + \frac{d_n}{2^n} \right]$$

V_o - o/p voltage ; V_{FS} - Full scale voltage (i.e o/p when all i/p's are high)

Types of DACs

- Weighted Resistor DAC
- R-2R Ladder DAC
- Inverted R-2R Ladder DAC

→ For n-bit digital data, it consists of total 2^n levels.

→ Resolution: Resolution is defined as

- 1) Difference b/w two successive o/p voltage levels (or)
- 2) Ratio of difference of max. o/p voltage and min. o/p voltage level to $2^n - 1$

i.e

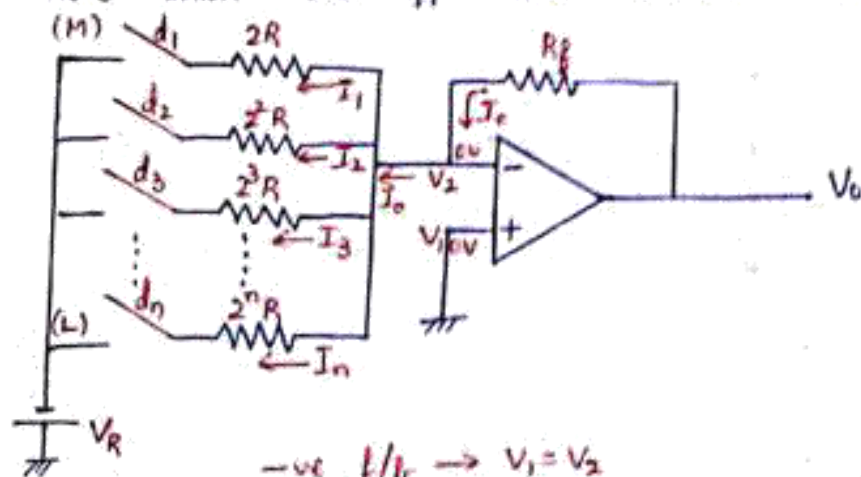
$$\text{Resolution} = \frac{V_{\max} - V_{\min}}{2^n - 1}$$

$V_{\max}$ - o/p when all i/p's are high = V_{FS}

$V_{\min}$ - o/p when all i/p's are zeros

1) Weighted Resistor DAC:

This circuit is same as inverting amplifier but it consists of more than one i/p with various resistors.



-ve f/b → $V_1 = V_2$

$V_1 = 0 \Rightarrow V_2 = 0$

the operation of the switch is as follows:

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$$V = \begin{cases} 0, & d=0 \\ -V_R, & d=1 \end{cases}$$

So $V = d(-V_R)$

Apply Nodal analysis at inverting terminal:

$$\frac{0 - (-V_R d_1)}{2R} + \frac{0 - (-V_R d_2)}{2^2 R} + \frac{0 - (-V_R d_3)}{2^3 R} + \dots + \frac{0 - (-V_R d_n)}{2^n R} + \frac{0 - V_o}{R_f} = 0$$

$$V_o = V_R \cdot \frac{R_f}{R} \left[\frac{d_1}{2} + \frac{d_2}{2^2} + \frac{d_3}{2^3} + \dots + \frac{d_n}{2^n} \right]$$

$V_{\max} = V_{FS} \leftarrow$ all i/p's are high

$$\rightarrow V_{FS} = V_R \frac{R_f}{R_1} \left[\frac{1}{2} + \frac{1}{2^2} + \frac{1}{2^3} + \dots + \frac{1}{2^n} \right]$$

$n=3$; $V_{FS} = V_R \frac{R_f}{R_1} \times \frac{7}{8}$

$n=5$; $V_{FS} = V_R \frac{R_f}{R_1} \times \frac{31}{32}$

For n bit $V_{FS} = V_R \cdot \frac{R_f}{R_1} \cdot \frac{2^n - 1}{2^n}$

$V_{\min} \leftarrow$ all i/p's are zeros

So $V_{\min} = V_R \frac{R_f}{R_1} \left[\frac{0}{2} + \frac{0}{2^2} + \dots + \frac{0}{2^n} \right]$

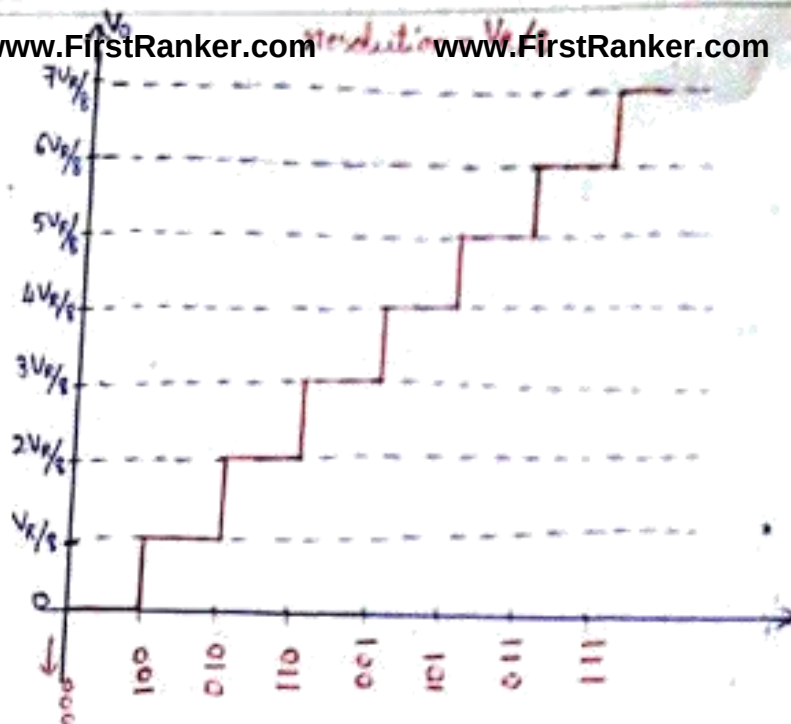
$V_{\min} = 0$

So Resolution = $\frac{V_R \frac{R_f}{R_1} \cdot \frac{2^n - 1}{2^n}}{2^n - 1}$

$$\text{Resolution} = V_R \cdot \frac{R_f}{R_1} \cdot \frac{1}{2^n}$$

Let if $n=3$ and $R_2 = R_1$

$d_1 d_2 d_3$	V_o
000	0
001	$V_R/8$
010	$2V_R/8$
011	$3V_R/8$
100	$4V_R/8$
101	$5V_R/8$
110	$6V_R/8$
111	$7V_R/8$



→ Draw backs:

As no. of i/p bits increase, we need more resistors with multiples of $2R$

i.e $n=3 \rightarrow 2R, 2^2R, 2^3R$

$n=8 \rightarrow 2R, 2^2R, \dots, 2^8R$

$n=15 \rightarrow 2R, 2^2R, \dots, 2^{15}R$

We may not get accurate resistors with higher values.

→ Switches with binary i/p may disturb the circuit in currents

Choice of $R = 2.5K\Omega$ to avoid loading effect

2 → R-2R Ladder Type DAC:

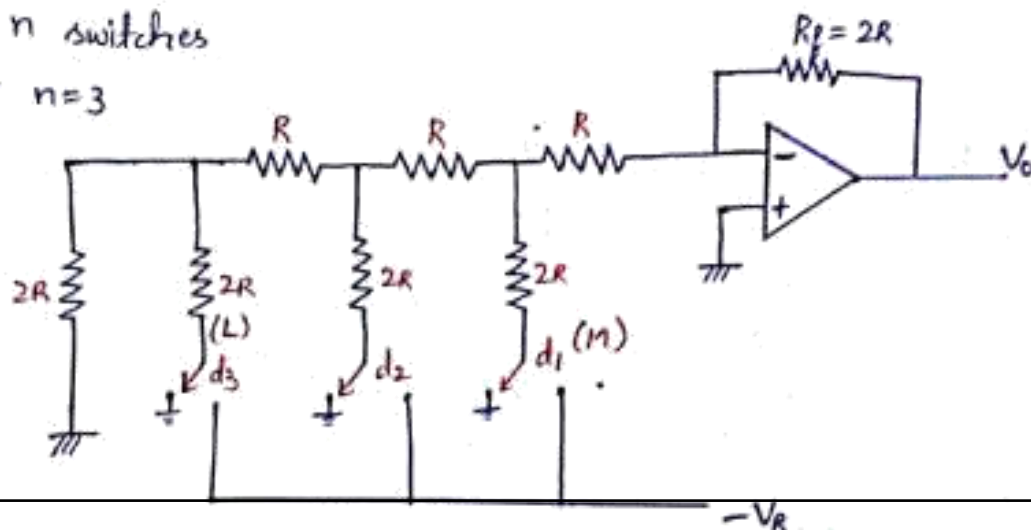
To design this with n -bit i/p, we need

→ n resistors with value R

→ $n+2$ resistors with value $2R$

→ n switches

Let $n=3$



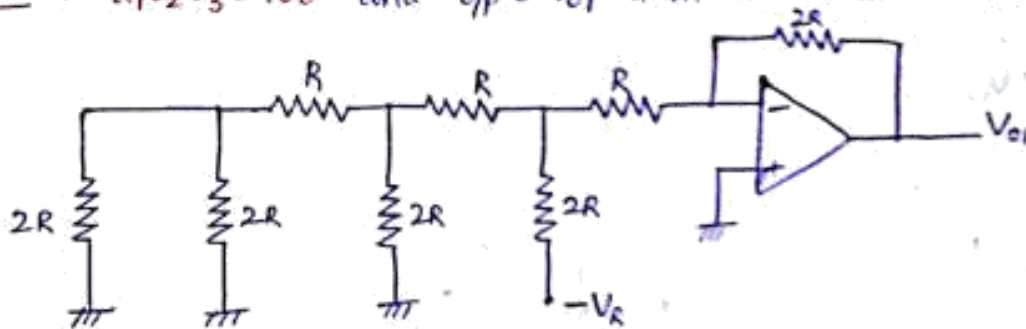
→ Switch operation:

$$-V_R \xrightarrow{d} \downarrow \quad V = \begin{cases} -V_R & d=1 \\ 0 & d=0 \end{cases} \Rightarrow \boxed{V = -dV_R}$$

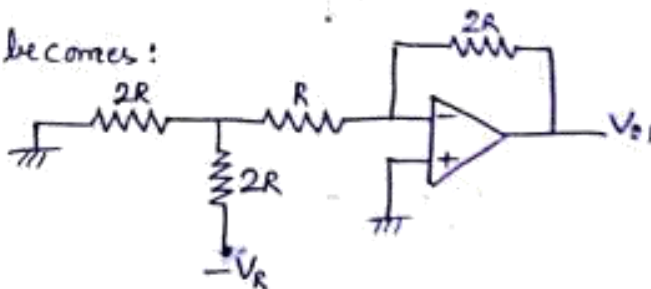
To get the o/p equation V_o we are using super position theorem i.e first we have to take one source as active and remaining all as inactive.

So $V_o = \text{o/p (when } d_1 d_2 d_3 = 100) + \text{o/p (when } 010) + \text{o/p (when } 001)$ — ①

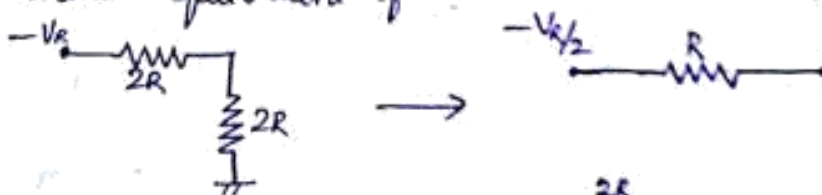
Case-1 : $d_1 d_2 d_3 = 100$ and $\text{o/p} = V_{o1}$ then the circuit becomes



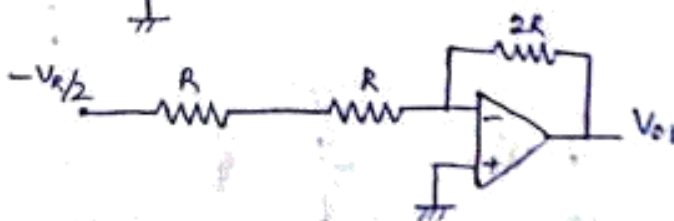
Circuit becomes:



Thvenins equivalent of

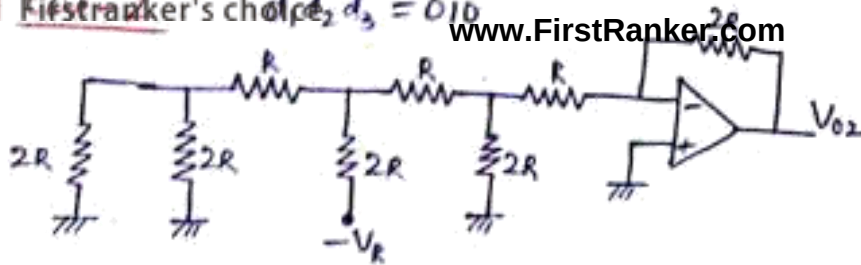


So

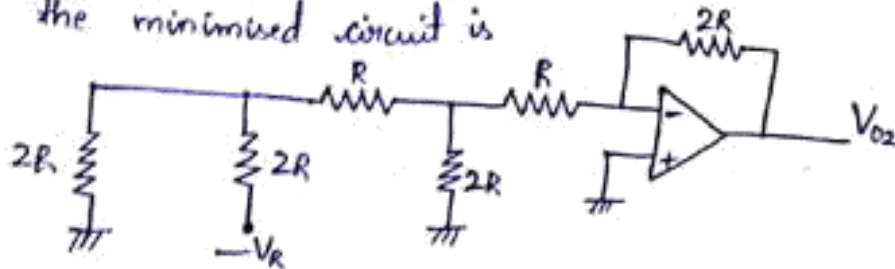


Applying nodal analysis:

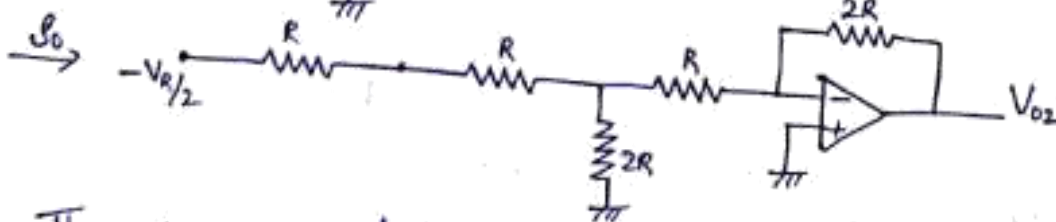
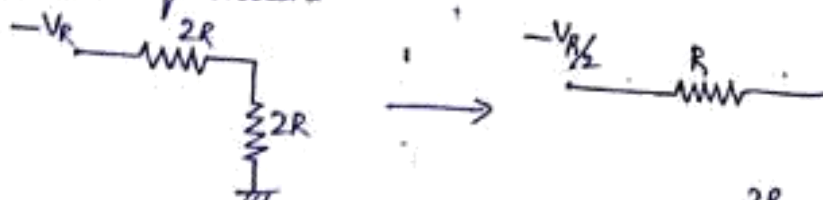
$$\frac{0 - (-V_R/2)}{2R} + \frac{0 - V_{o1}}{2R} = 0 \Rightarrow \boxed{V_{o1} = \frac{V_R}{2}} \text{ — ②}$$



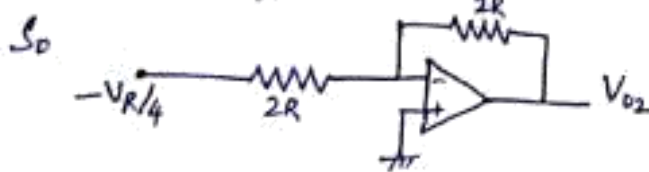
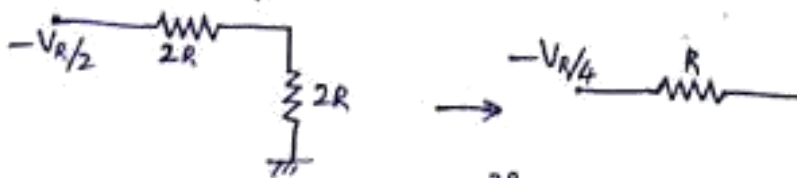
So the minimised circuit is



Thevenin's equivalent



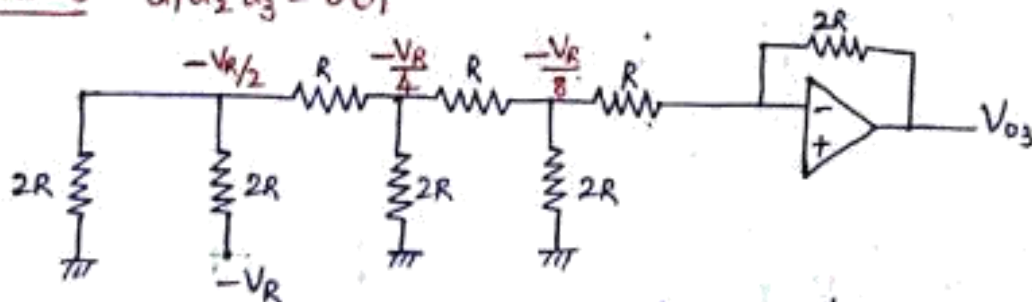
Thevenin's equivalent:



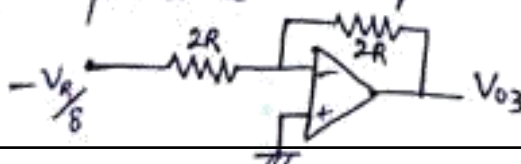
$$\frac{0 - (-V_R/4)}{2R} + \frac{0 - V_{02}}{2R} = 0$$

$$V_{02} = \frac{-V_R}{4} \quad (3)$$

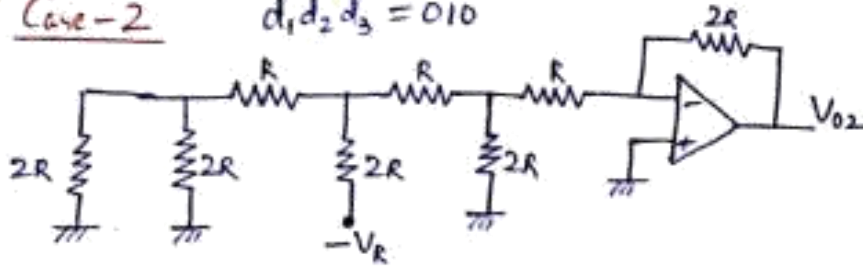
Case-3 $d_1 d_2 d_3 = 001$



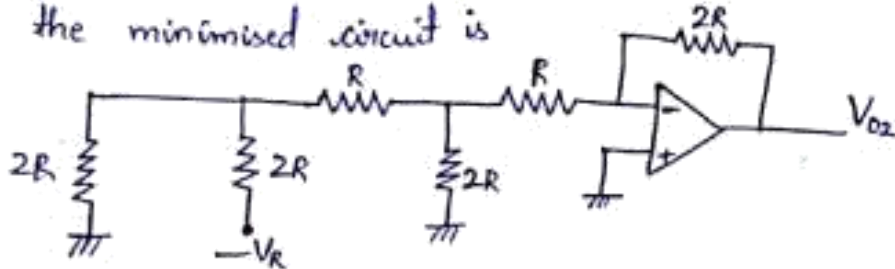
So, As previous procedure the equivalent circuit is



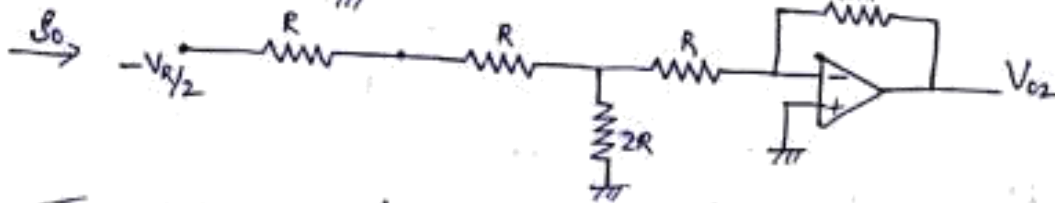
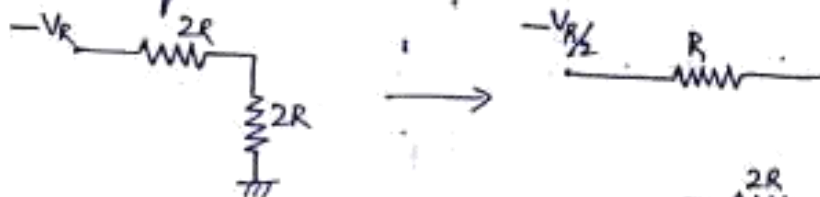
Q Case-2 $d_1 d_2 d_3 = 010$



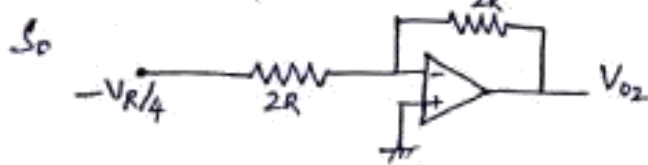
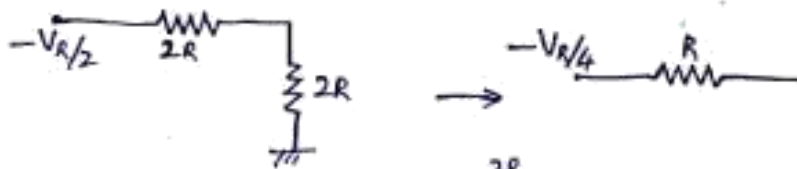
So the minimised circuit is



Thevenin's equivalent



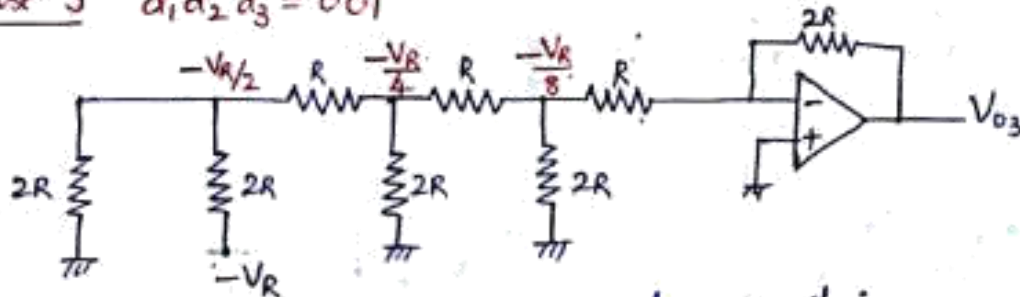
Thevenin's equivalent:



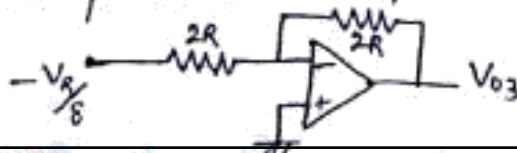
$$\frac{0 - (-V_R/4)}{2R} + \frac{0 - V_{O2}}{2R} = 0$$

$$V_{O2} = -\frac{V_R}{4} \quad (3)$$

Case-3 $d_1 d_2 d_3 = 001$



So, As previous procedure the equivalent circuit is



$$\frac{0 - (-V_R)}{2R} + \frac{0 - V_{O3}}{2R} = 0 \Rightarrow V_{O3} = \frac{V_R}{8} \quad \text{--- (4)}$$

From (1), (2), (3) and (4) we can write that

$$V_O = V_{O1}d_1 + V_{O2}d_2 + V_{O3}d_3$$

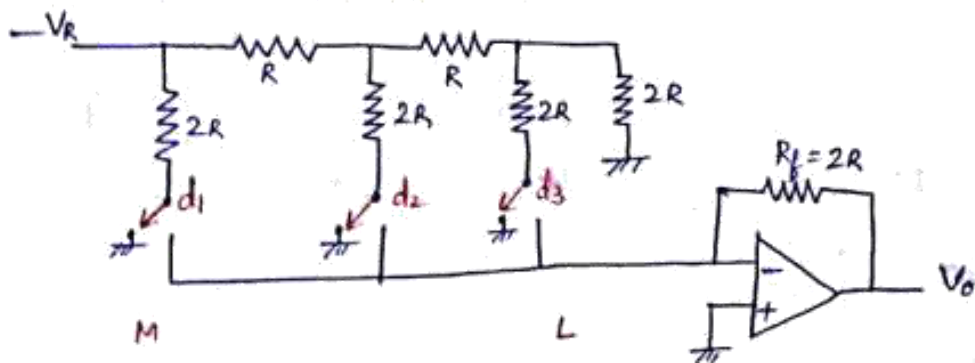
So $V_O = \frac{V_R}{2}d_1 + \frac{V_R}{4}d_2 + \frac{V_R}{8}d_3 \Rightarrow V_O = V_R \left[\frac{d_1}{2} + \frac{d_2}{2^2} + \frac{d_3}{2^3} \right]$

Advantage:

As no. of digital i/p bits increases we need more R and 2R resistors only

→ Inverted R-2R Ladder Type:

To design this for n-bit i/p we need
 n+2 → resistors with value 2R
 n-1 → resistors with value R



d=1 → Switch connected to source $-V_R$

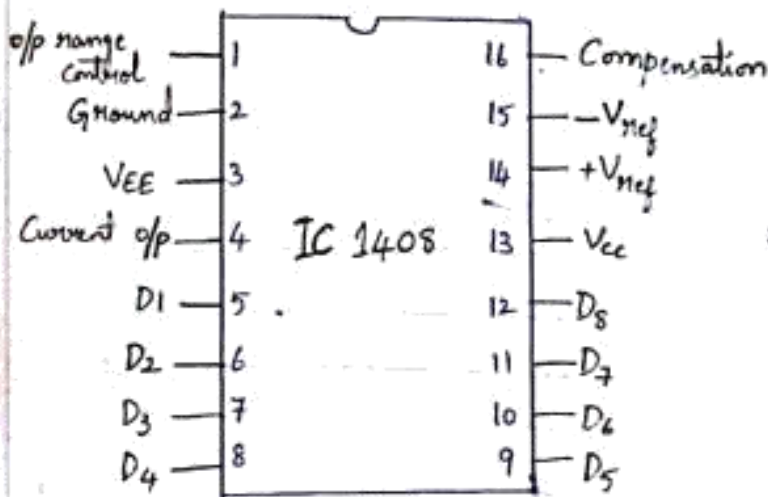
d=0 → Switch connected to ground

$$V_O = V_R \left[\frac{d_1}{2} + \frac{d_2}{4} + \frac{d_3}{8} \right]$$

→ Monolithic DAC : IC 1408

This monolithic IC 1408 is a R-2R ladder type DAC.

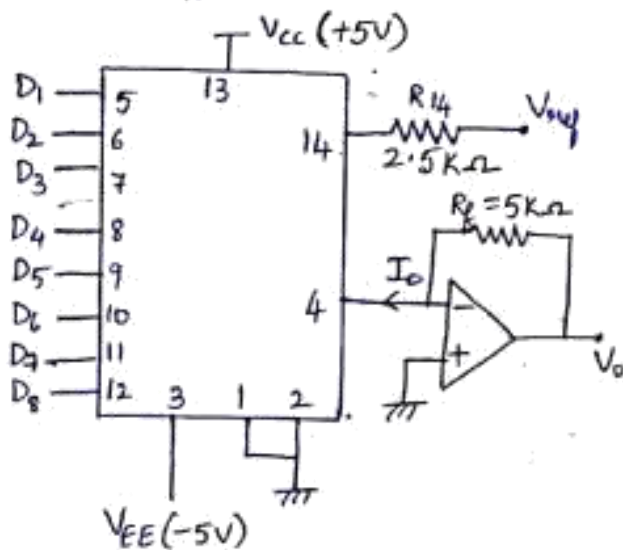
It is a 16 pin DIP. It converts 8 bit digital data into the analog form in form of o/p current I_O . The pin diagram of IC is as shown



1) $D_1, D_2, D_3, D_4, D_5, D_6, D_7, D_8$ are the 8 bit digital i/ps
 D_1 - MSB and D_8 - LSB

2) 4th pin is o/p terminal.
o/p is in the form of current I_o
 I_o direction is into the IC

Case-1: o/p is $0 \rightarrow 10V$



o/p of IC 1408 is in the form of current. To get in the form of voltage we are using .or .
connecting a I to V converter to the o/p terminal 4

The Basic relation in b/w I_o and digital data is

$$I_o = \frac{V_{ref}}{R_{14}} \left[\frac{D_1}{2} + \frac{D_2}{4} + \frac{D_3}{8} + \frac{D_4}{16} + \dots + \frac{D_8}{256} \right]$$

then based on I-V converter eq-n

$$V_o = I_o R_f$$

So

$$V_o = V_{ref} \frac{R_f}{R_{14}} \left[\frac{D_1}{2} + \frac{D_2}{4} + \dots + \frac{D_8}{256} \right]$$

If $V_{ref} = 5V$, $R_f = 5K\Omega$, $R_{14} = 2.5K\Omega$ then

$V_o(\min)$ (when all i/p's are zeros) is

$$V_{o\min} = 5 \times \frac{5K}{2.5K} \left[\frac{0}{2} + \frac{0}{4} + \dots + \frac{0}{256} \right]$$

$$V_{o\min} = 0$$

$V_{0 \max}$ (when all i/p's are 1)

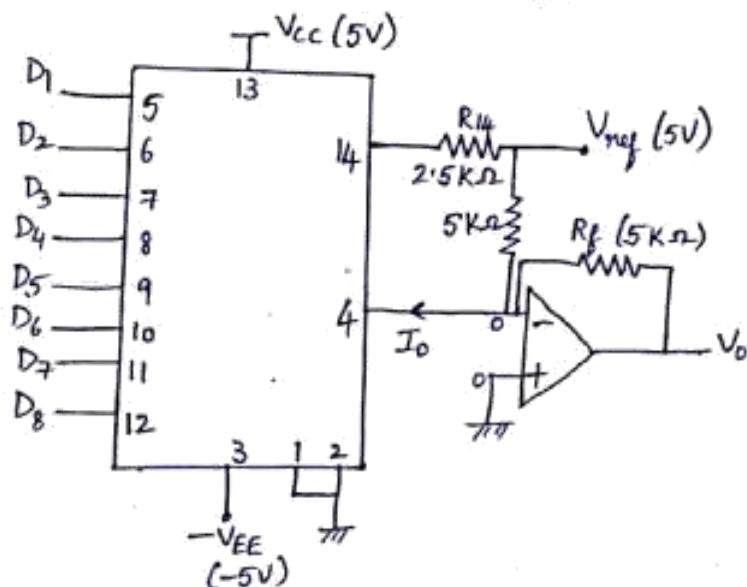
$$V_{0 \max} = 5 \times \frac{2.5K}{2.5K} \left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256} \right]$$

$$= 10 [0.9961] \Rightarrow \boxed{V_{0 \max} = 9.961 V} = V_{FS}$$

Step size is $\frac{V_{\max} - V_{\min}}{2^n - 1}$, here $n=8$

So resolution = step size = $\frac{9.961 - 0}{2^8 - 1} = 0.039$

Case-2 o/p is $-5 \rightarrow +5V$



The change in b/w this circuit and previous circuit is that we placed a resistor in b/w V_{ref} and inverting terminal of op-amp

Nodal analysis at inverting terminal

$$I_0 + \frac{0 - V_{ref}}{5K} + \frac{0 - V_0}{R_f} = 0 \Rightarrow \frac{V_0}{R_f} = I_0 - \frac{5}{5K}, \quad R_f = 5K\Omega$$

$$\boxed{V_0 = I_0 \times 5K - 5}$$

So, $V_0 = \frac{V_{ref}}{R_{14}} \times 5K \left[\frac{D_1}{2} + \frac{D_2}{4} + \dots + \frac{D_8}{256} \right] - 5$

$$V_0 = \frac{5}{2.5K} \times 5K \left[\frac{D_1}{2} + \frac{D_2}{4} + \dots + \frac{D_8}{256} \right] - 5$$

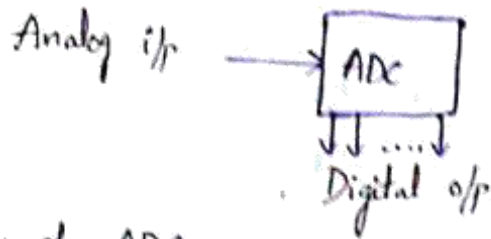
$$V_0 = 10 \left[\frac{D_1}{2} + \frac{D_2}{4} + \dots + \frac{D_8}{256} \right] - 5$$

$$V_{\min} = 10 \left[\frac{0}{2} + \frac{0}{4} + \dots \right] - 5 \Rightarrow \boxed{V_{\min} = -5V}; \quad V_{\max} = 10 \left[\frac{1}{2} + \frac{1}{4} + \dots + \frac{1}{256} \right] - 5$$

$$\boxed{V_{\max} = 4.961 V}$$

Resolution = step size = $\frac{4.961 - (-5)}{2^8 - 1} = 0.039 V$

→ Analog to Digital conversion:



Types of ADCs:

- 1) Parallel comparator or flash type
- 2) Counter type
- 3) Servo tracking ADC
- 4) Successive approximation type
- 5) Dual slope ADC

→ Various parameters:

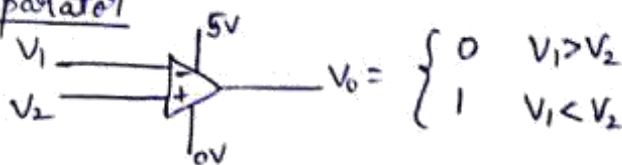
→ V_{FS} - Full scale voltage when all o/p's are 1's

$$\text{Resolution} = \frac{V_{FS} - V_{min}}{\text{No. of levels}}$$

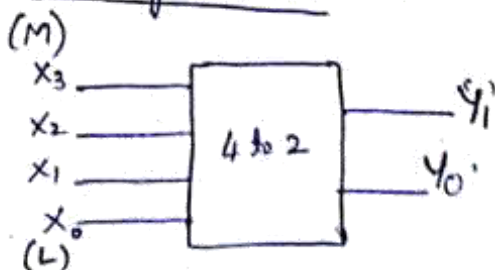
1) Parallel comparator (Flash type) ADC:

To design n -bit digital o/p ADC (flash), we need 2^n comparators and one 2^n to n priority encoder, 2^n - resistor (of same value)

→ Comparator



→ Priority encoder Let $n=2 \rightarrow$ so 2^2 to $2 \rightarrow 4$ to 2



Truth table X - don't care i/o

X_3	X_2	X_1	X_0	Y_1	Y_0
0	0	0	1	0	0
0	0	1	X	0	1
0	1	X	X	1	0
1	X	X	X	1	1

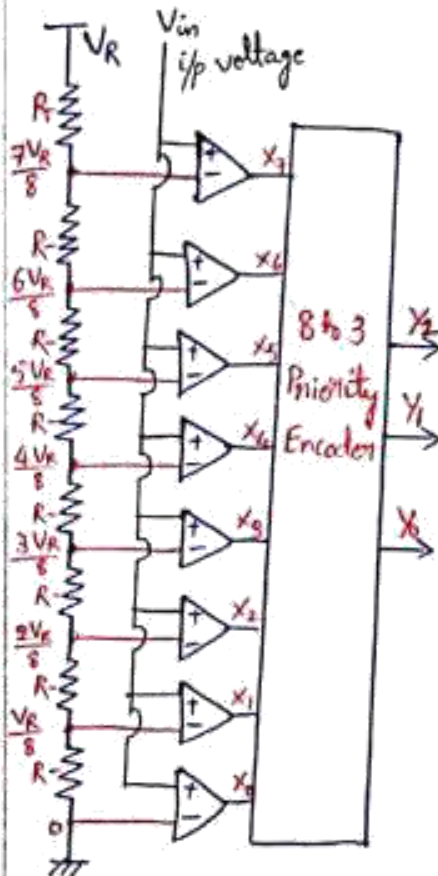
This priority encoder is different than normal encoder. In this, it reads the i/p from MSB to LSB. If any bit is '1' then it will not check the remaining LSB bits, produces the o/p

Let 3 bit digital o/p flash ADC

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- Comparators : $2^3 = 8$
- Resistors : $2^3 = 8$
- Priority encoder : 2^3 to 3 → 8 to 3

Circuit:



I/p Range	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
$0 \rightarrow \frac{V_R}{8}$	0	0	0	0	0	0	0	1	0	0	0
$\frac{V_R}{8} \rightarrow \frac{2V_R}{8}$	0	0	0	0	0	0	1	1	0	0	1
$\frac{2V_R}{8} \rightarrow \frac{3V_R}{8}$	0	0	0	0	0	1	1	1	0	1	0
$\frac{3V_R}{8} \rightarrow \frac{4V_R}{8}$	0	0	0	0	1	1	1	1	0	1	1
$\frac{4V_R}{8} \rightarrow \frac{5V_R}{8}$	0	0	0	1	1	1	1	1	1	0	0
$\frac{5V_R}{8} \rightarrow \frac{6V_R}{8}$	0	0	1	1	1	1	1	1	1	0	1
$\frac{6V_R}{8} \rightarrow \frac{7V_R}{8}$	0	1	1	1	1	1	1	1	1	1	0
$\frac{7V_R}{8} \rightarrow V_R$	1	1	1	1	1	1	1	1	1	1	1

Here i/p voltage is applied to all +ve terminals of comparators and thresholds are connected to -ve terminals.

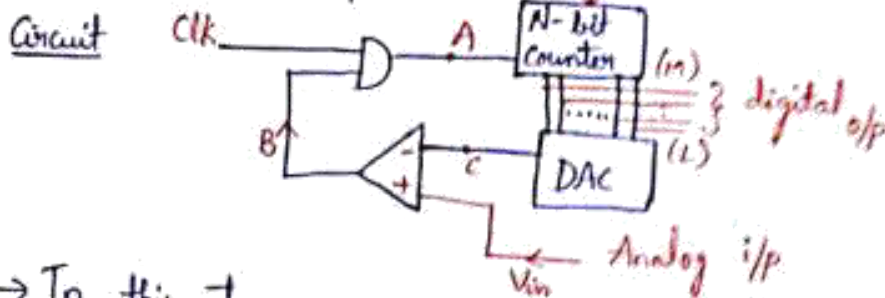
Advantage: This is the fastest ADC

Disadvantage: As no. of o/p bits increase, no. of comparators, resistors and priority encoder range (value) also increases. So complexity and cost increases.

→ Counter Type ADC

Counter is used to count the no. of clock cycles entered into the counter, as clock cycle enters counter value incremented (up-counter) or decremented (down counter)

Here we are using up counter



- In this type ADC we are using DAC also
- Here counter i/p is A if A is a clock signal then counter will be incremented, if zero counter will be at previous state only (i.e. not changed)
- B is comparator o/p this is '1' or '0'. It controls A.
If $B=1$ then $A=clk$, if $B=0$ then $A=0$
- C is DAC o/p i.e. counter content (count) is converted into analog and it is compared with i/p analog signal.

The total operation is

$$B = \begin{cases} 1 & V_{in} > C \\ 0 & V_{in} \leq C \end{cases}$$

$$A = clk \cdot B$$

$C =$ Counter content

A reset button is present for counter. After every conversion reset will be activated then counter will be re-initiated to zero i.e. all bits are zeros.

Operation:

Let i/p is 5V and digital o/p length (no. of bits) is 3 and step size is 1 then operation will be

V_{in}	C	B	A	$o/p = C$ (Initially)
5	0	1	clk-①	001
5	1	1	clk-②	010
5	2	1	clk-③	011
5	3	1	clk-④	100
5	4	1	clk-⑤	101
5	5	0	0	101

So after 5 clock cycle conversions reset will be activated then counter will be zero. Let next i/p is 3. then

3	0	1	Clk-①	001
3	1	1	Clk-②	010
3	2	1	Clk-③	011
3	3	1	0	<u>011</u>

So after 3 clock cycle conversions

if i/p sequence is 5, 3, 2, 4, 6, 1, 7 then total time taken to convert total sequence is $5+3+2+4+6+1+7 = 28$ clock cycles (when step size is 1V)

If step size is not 1V then to convert 'X' volts into digital then we need $\frac{X}{\text{step size}}$ clock cycles for single conversion.

If step size is 0.5V for previous eg. sequence total time taken is

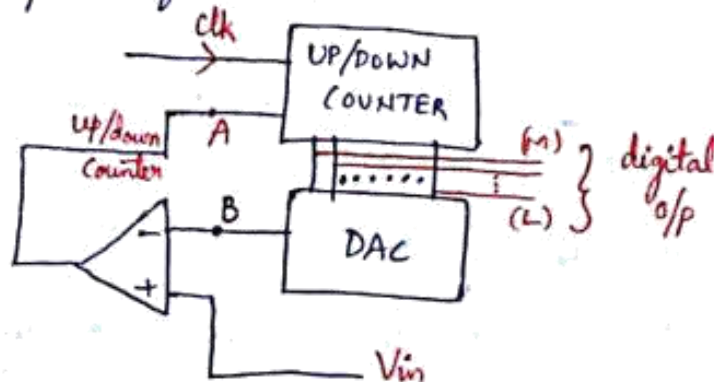
$$\frac{5}{0.5} + \frac{3}{0.5} + \frac{2}{0.5} + \frac{4}{0.5} + \frac{6}{0.5} + \frac{1}{0.5} + \frac{7}{0.5} = \frac{28}{0.5} = 56 \text{ clock cycles}$$

Disadvantages 1) Conversion type is more

2) Internally it consists of a comparator and DAC. So we have to consider these delays also for every iteration. So time taken to convert is more

→ Servo tracking ADC:

This is a modification of counter type ADC. Here we use up/down counter in place of normal counter.



This is similar to counter type but the change is

$$\Rightarrow A = \begin{cases} 1 & V_{in} > B \\ 0 & V_{in} = B \\ -1 & V_{in} < B \end{cases}, \quad 2) \text{ Counter type} = \begin{cases} \text{up} & A=1 \\ \text{down} & A=-1 \\ \text{stops} & A=0 \end{cases}$$

In this there is no reset button. So after every conversion, counter will not be changed, it stays in the same state.

If i/p is 5, 3, 4 and o/p length is 3 bit.

V _{in}	B	A	Counter Type	o/p (ooo)
① 5	0	1	up	001
② 5	1	1	up	010
③ 5	2	1	up	011
④ 5	3	1	up	100
⑤ 5	4	1	up	101
⑥ 5	5	0	stops	101
① 3	5	-1	down	100
② 3	4	-1	down	011
③ 3	3	0	stops	011
① 4	3	1	up	100
② 4	4	0	stops	100

So to convert 5, 3, 4 sequence we need 8 clock cycles when step size is 1

$$\text{i.e. } 5 + |3-5| + |4-3| = 5 + 2 + 1 = 8$$

→ If i/p sequence is 5, 3, 2, 4, 6, 1, 7 then time taken is
 $5 + |3-5| + |2-3| + |4-2| + |6-4| + |1-6| + |7-1| = 23$ clock cycles

So this count is less than counter type

If step size is not '1' then $= \frac{23}{\text{Step size}}$

→ This type ADC is advantageous when and only when i/p is linearly varying i.e. change b/w this i/p and previous i/p and this i/p and next i/p is less

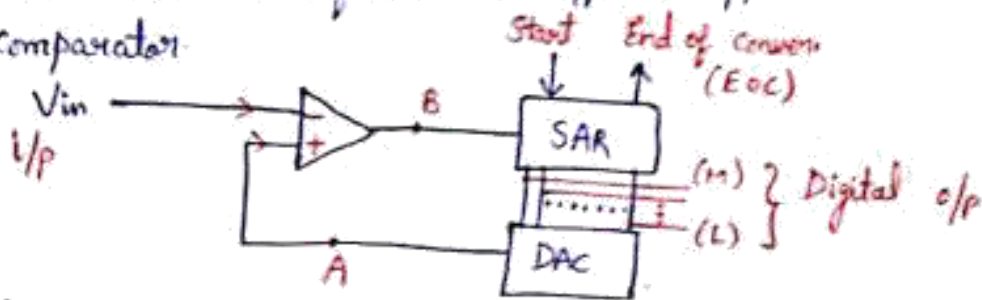
→ If i/p is not linear then tracking error will be encountered.

Successive Approximation Type:

This is more advantageous than counter and servo tracking types. Here we don't use a counter, we use a register i.e.

SAR (successive approximation register)

→ One more modification is i/p is applied to -ve terminal of the comparator.



Here A is DAC o/p and B is SAR i/p

$$B = \begin{cases} 1 & A > V_{in} \\ 0 & A < V_{in} \end{cases}$$

About SAR:

For n-bit digital o/p ADC, we need n-bit SAR.

→ Initially it consists of n-bits, as all bits are zeros except MSB (MSB-1) i.e. if $n=3 \rightarrow 100$; $n=4 \rightarrow 1000$

→ Then compare the SAR content (A) with V_{in} then SAR content will be changed.

In X^{th} level: $X = 1, 2, \dots, n+1$

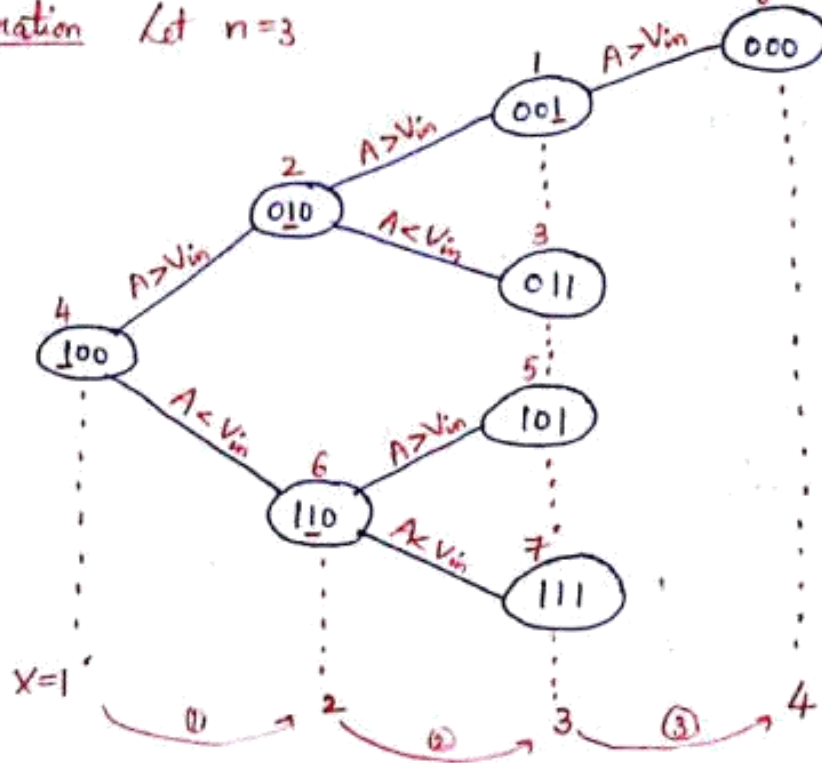
→ If $V_{in} > A$ then A has to be increased, then SAR content's X^{th} MSB is right shifted by '1'

→ If $V_{in} < A$ then A has to be decreased, then SAR content's X^{th} MSB is right shifted by '0'

Here $X = 1, 2, \dots, n+1$ (n-no. of o/p bits)

The remaining MSBs are as same as previous level

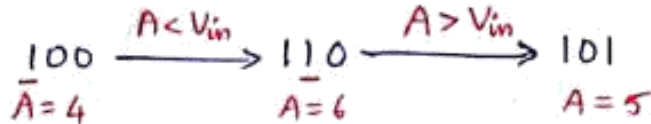
Operation Let $n=3$



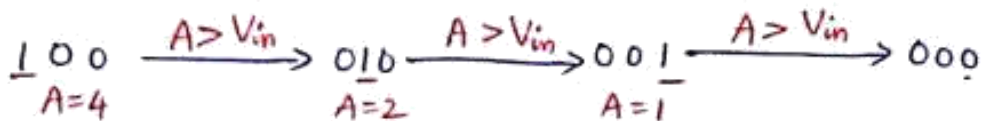
So max. no. of clock cycles needed for 3 bit conversion is 3 clock cycles only. For n bit we need n -clock cycles.

Ex:

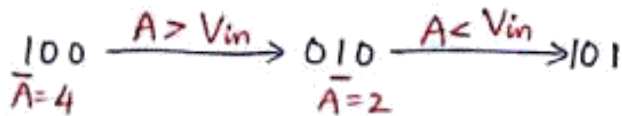
1) I/p is 5V



2) i/p is 0V



3) i/p is 3V



4) if $n=4$, i/p is 10V then

