Pulse & Digital Circuits

CONTENTS

Pulse & Digital Circuits

1. Linear Wave Shaping

SYLLABUS:

High Pass and Low Pass RC Circuits and their Response for Sinusoidal, Step Voltage, Pulse, Square Wave and Ramp Inputs. High Pass RC Circuit as a Differentiator. Low Pass RC Circuit as an Integrator. Attenuators and their application as CRO Probe. RL and RLC Circuits and their response for step input. Ringing circuit.

Linear wave shaping:

Introduction:

If a circuit is designed with components like R, L and C then it is called linear circuit. When sinusoidal signal is applied, the shape of the signal is preserved at the output with or without change in the amplitude and shape. But a non-sinusoidal signal alters the output when it is transmitted through a linear circuit. The process whereby the form of non-sinusoidal signals such as step, pulse, square wave, ramp and exponential is altered by transmission through a linear network is called linear wave shaping.

1.1 High pass RC circuit:
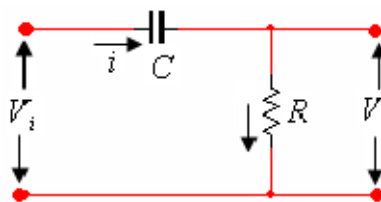
Consider high pass RC circuit as shown in fig.1 below.

Fig.1 highpass rc circuit

The capacitor offers high reactance at low frequency and low reactance at high frequency. Hence low frequency components are not transmitted, but high frequencies are with less attenuation. Therefore the output is large and the circuit is called a high pass circuit.

Let us see now is, what will be the response if different types of inputs, such as, sinusoidal ,step, pulse, square wave, exponential and ramp are applied to a high pass circuit.

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1.2 Response of high pass RC for sinusoidal input:

(i) sinusoidal input:

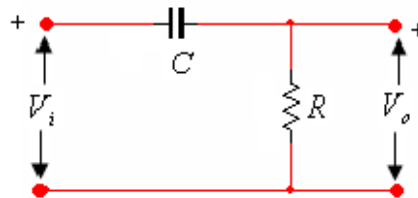First consider the response of a high pass RC circuit.

Fig.2 high pass RC circuit

$$V_o = V_i \frac{R}{R + 1/j\omega C}$$

$$\left|\frac{V_o}{V_i}\right| = \frac{R}{\sqrt{R^2 + \left(\frac{1}{\omega C}\right)^2}} = \frac{R}{R\sqrt{1 + \left(\frac{1}{\omega CR}\right)^2}} = \frac{1}{\sqrt{1 + \left(\frac{1}{\omega CR}\right)^2}}$$

Let $\omega_1 = \frac{1}{CR}$

$$\left|\frac{V_o}{V_i}\right| = \frac{1}{\sqrt{1 + \left(\frac{\omega_1}{\omega}\right)^2}}$$

At $\omega = \omega_1$

$$\left|\frac{V_o}{V_i}\right| = \frac{1}{\sqrt{2}} = 0.707$$

Hence, f_1 is the lower cut-off frequency of the highpass circuit.
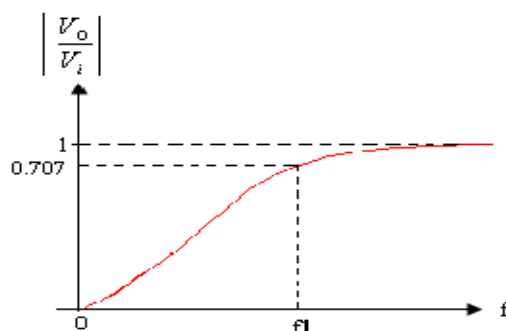
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Fig.3 frequency response curve for sinusoidal input.

1.3 High Pass RC response for Step signal input.

(ii) Step input

A Step voltage is defined as,
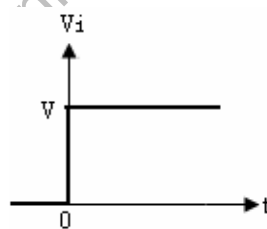
$V_i = 0$ for t < 0

and $V_i = V$ for t ³ 0

Fig.4 Step Voltage

The output voltage is of the form

$$V_o = B_1 + B_2 \, e^{-t/\tau}$$

Where τ = RC, the time constant of the circuit.

B1 is the steady state value as t → ∞, and hence $o\ V → $ B1

Let the final value be which we denote as V_f.

Then $V_f = $ B1.

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B2 is determined by the initial output voltage.

At t = 0, $V_i = V_o = B1 + B2$

Therefore, $B2 = V_i - B1$

$$= V_i - V_f$$

Hence the general solution is

$$V_o = V_f + (V_i - V_f) e^{-t/}$$

Fall time t_f: When a step is applied, the time taken for the output voltage to fall from 90□of its initial value to 10% of its initial value is the fall time. It indicates how fast the output reaches its steady state value.

The output voltage at any instant of time, in high pass circuit, is given by

$$V_o(t) = Ve^{-t/\tau}, \quad \text{At } t = t_1, \quad V_o(t_1) = 90\% \text{ of } V = 0.9V$$

$$0.9 = e^{-t_1/\tau}$$

$$e^{t_1/\tau} = 1/0.9 = 1.11$$

$$t_1/\tau = \ln(1.11)$$

$$t_1 = \tau \ln(1.11) = 0.1\tau$$

At $t = t_2$, $V_o(t) = 10\%$ of $V = 0.1V$

$$0.1 = e^{-t_2/\tau}$$

$$e^{t_2/\tau} = 1/0.1 = 10$$

$$t_2 = \tau \ln(10) = 2.3\tau$$

fall time, $t_f = t2 - t1 = 2.3\tau - 0.1\tau = 2.2\tau$

The lower half power frequency of the highpass circuit is

$$f_1 = \frac{1}{2\pi RC}$$

$$\tau = RC = \frac{1}{2\pi f_1}$$

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$$\text{Fall time} = t_f = 2.2\ \tau = \frac{2.2}{2\pi f_1} = \frac{0.35}{f_1}$$

Hence, the fall time is inversely proportional to f1, the lower cut-off frequency.

1.4 High Pass RC response for Square signal input.

(iii)**Pulse input:** A pulse can be expresseds combination of a positive (negative) step followed by negative(positive) step w.r.t. times i.e.V_i = Vu (t) - Vu (t – tp) where tp is the duration of the pulse as shown below in fig.5

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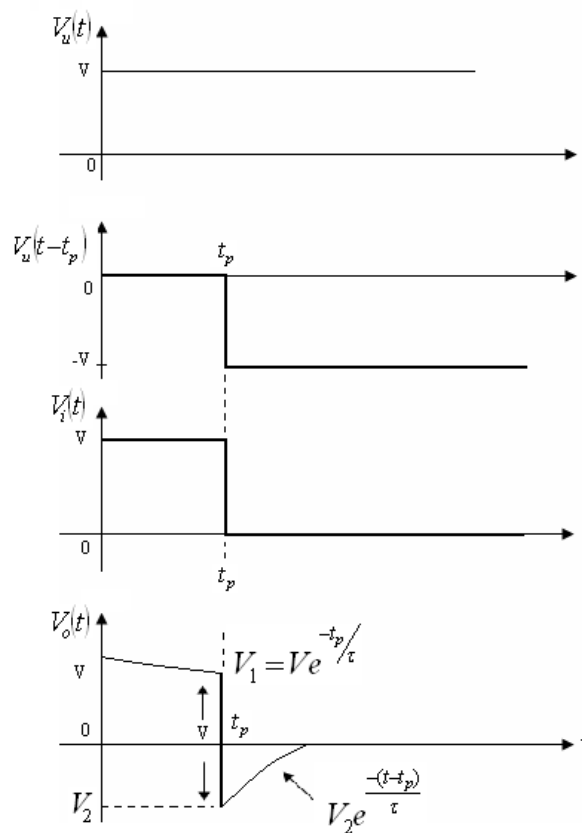
Fig.5 Pulse input and output of a high pass circuit

Consider a pulse signal is applied to the input of a high pass circuit.

At t=0,V_i abruptly rises to V . As the capacitor is connected between the input and output, the output also changes by the same amount. As the input remains constant, the output decays exponentially to V_1 at t = tp.

Therefore, $V_1 = Ve^{-t_p/\tau}$

At t = t_p, the input abruptly falls by V.V_o also falls by the same amount.

At t = t_p, $V_o = V_1 - V$

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Since $V1$ is less than V, Vo is negative and its value is $V2$ and this decays to zero exponentially.
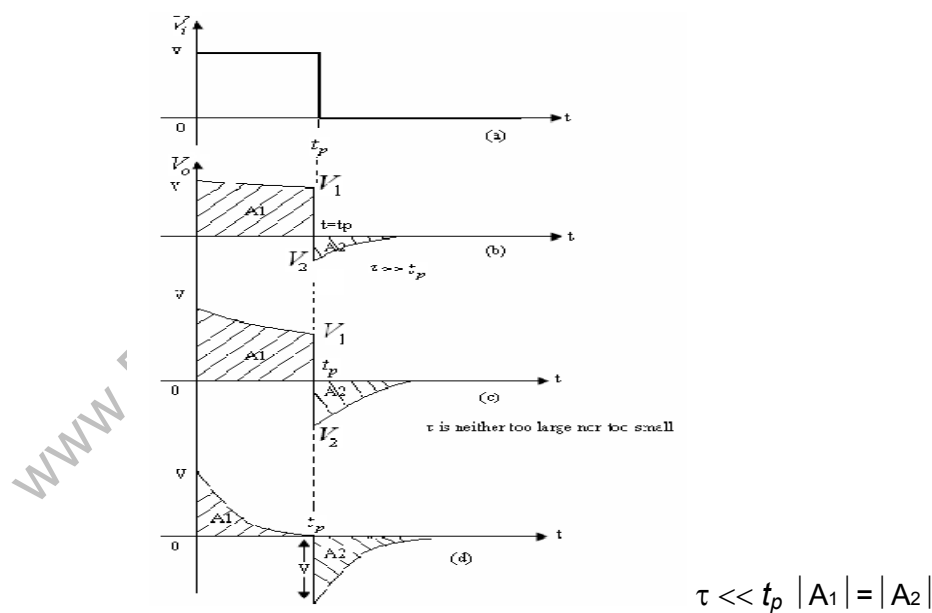
For t > tp,

$$V_o = (V_1 - V)e^{-(t-t_p)/\tau}$$

But

$$V_1 = Ve^{-t_p/\tau}$$

$$\therefore V_o = V(e^{-t_p/\tau} - 1)e^{-(t-t_p)/\tau}$$

The response of a high pass circuit with pulse input for different values of τ is plotted in fig.1.6.

$$\tau << t_p \quad |A_1| = |A_2|$$

Fig.6 Response of a high pass circuit for pulse input

It is very clear that output has distortion when a pulse is passing through a high pass RC circuit. The shape of the pulse at the output is almost preserved when the time constant □

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is very large (fig.6b) whereas in fig.6c there is a tilt at the top of the pulse and an undershoot at the end of the pulse.

If $\tau \ll t_p$ (fig.1.6d), the output consists of a positive spike at the beginning of the pulse and a negative spike at the end of the pulse, that means a highpass circuit converts a pulse into spikes called 'peaking'. To have a less distortion, τ must be very much larger than the time period of the input pulse. In general, there is an undershoot at the end of the pulse. The area above the axis (A1) is always equal to the area below (A2).

Area A1:

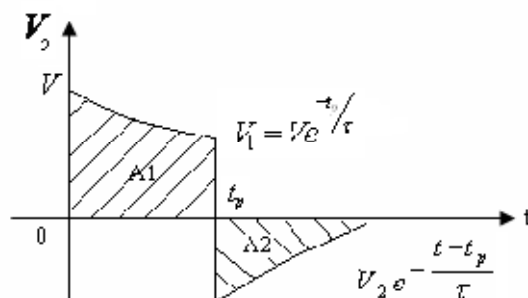$0 < t < t_p$

$$V_o = V e^{-t/\tau}$$

Fig.7 Calculation of A1 and A2

$$A_1 = \int_0^{t_p} V e^{-t/\tau} dt = \left[-V\tau e^{-t/\tau} \right]_0^{t_p}$$

$$A_1 = \left[-V\tau e^{-t_p/\tau} + V\tau \right] = V\tau(1 - e^{-t_p/\tau})$$

Similarly

$$A_2 = \int_{t_p}^{\infty} V(e^{-t_p/\tau} - 1) e^{-(t-t_p)/\tau} dt$$

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$$= \int_{t_p}^{\infty} \left[Ve^{-t/\tau} - Ve^{-(t-t_p)/\tau} \right] dt$$

$$= \left[\frac{Ve^{-t/\tau}}{-1/\tau} \right]_{t_p}^{\infty} - \left[V\frac{1}{-1/\tau} e^{-(t-t_p)/\tau} \right]_{t_p}^{\infty}$$

$$A_2 = \left[V\tau e^{-t_p/\tau} - V\tau \right] = -V\tau(1 - e^{-t_p/\tau})$$

$$|A_1| = |A_2|$$

(iv)   Square wave-Average level

A waveform that has a constant amplitude ' V for a time T1 and has another constant Amplitude ' V for a time T2 and which is repetitive with a time T= (T1+ T2) is called a square Wave. If T1= T2 =T/2, then it is called a symmetric square wave and the typical input-output

Waveforms of the high pass circuit are shown in fig below.
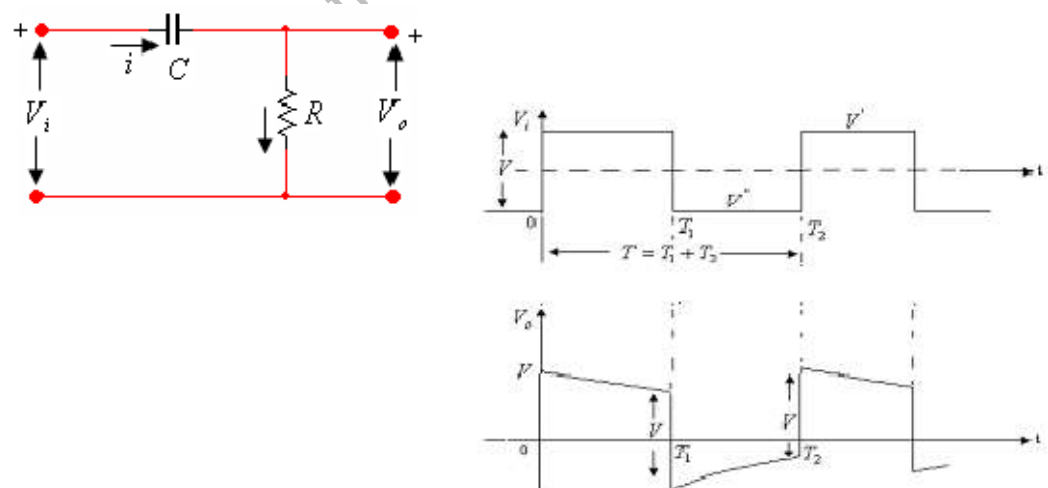
Fig.8 output of a high pass for symmetric square wave input

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Whatever is the dc component associated with the periodic input, waveform the dc level of the Steady state output signal for the high pass circuit is always zero.

This can be verified by using KVL equation

$$V_i = \frac{q}{C} + V_o$$

where q is the capacitor charge

Differentiating with respect to t

$$\frac{dV_i}{dt} = \frac{1}{C}\frac{dq}{dt} + \frac{dV_o}{dt}$$

$$\text{But } i = \frac{dq}{dt}$$

Substituting above condition

$$\frac{dVi}{dt} = \frac{i}{C} + \frac{dV_o}{dt}$$

since $V_o = iR, \quad i = \dfrac{V_o}{R} \quad$ *and* $RC = \tau$

Multiplying by dt and integrating over the time period T we get

$$\therefore \frac{dV_i}{dt} = \frac{V_o}{\tau} + \frac{dV_o}{dt}$$

Multiplying by dt and integrating over the time period T we get

$$\int_0^T dV_i = \left[V_i\right]_0^T = V_i(T) - V_i(0)$$

$$\int_0^T \frac{V_o}{\tau} dt = \frac{1}{\tau}\int_0^T V_o dt$$

$$\int_0^T dV_o = \left[V_o\right]_0^T = V_o(T) - V_o(0)$$

From above equations

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$$V_i(T) - V_i(0) = \frac{1}{\tau} \int_0^T V_o \, dt + [V_o(T) - V_o(0)]$$

Under steady-state conditions, the output and the input waveform are repetitive with a time period T. Therefore,

$$\int_0^T V_o \, dt = 0 \qquad\qquad V_i(T) = V_o(T) \text{ and } V_i(0) = V_o(0)$$

Since this integral represents the area under the output waveform over one cycle, it is evident that the dc in the steady state is always zero.

1.5 High pass RC response for Square wave input:

Now consider the response of the high pass RC circuit for a square wave input for different values of the time constant, τ, fig below.
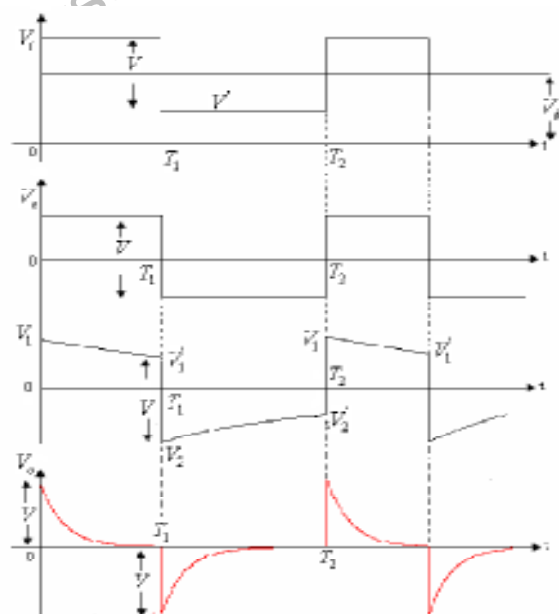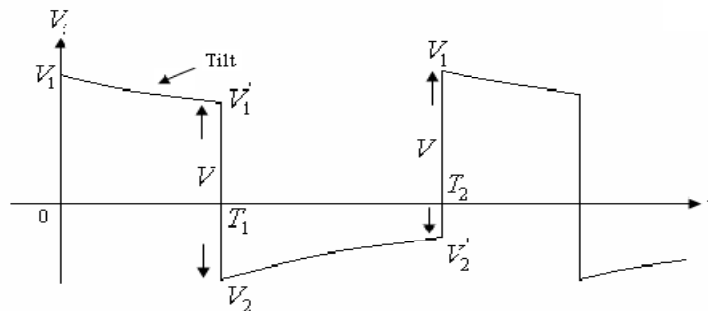
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Fig.9 Response of a highpass circuit for square input

a) Square Wave input

(b) Response $\tau \gg T1$ and $\tau \gg T2$

(c) Response when τ is neither too large nor too small

(d) Response when τ is very small

Consider the typical response of the highpass circuit for square wave input, fig.10

Fig.10 response of a highpass RC circuit for squarewave input

We know that $V_1' = V_1 e^{-T_1/\tau}$ and $V_1' - V_2 = V$

And $V_2' = V_2 e^{-T_2/\tau}$ and $V_1 - V_2' = V$

For a symmetric square wave

$$T_1 = T_2 = \frac{T}{2}$$

And because of symmetry'

$$V_1 = -V_2 \quad and \quad V_1' = -V_2'$$

'From equation

$$V_1' - V_2 = V$$

But

$$V_1' = V_1 e^{-T_1/\tau}$$

Therefore

$$V_1 e^{-T_1/\tau} - V_2 = V$$

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From

$$V_1 = -V_2$$

Substituting, we have

$$V_1 e^{-T/\tau} + V_1 = V$$

$$V_1(1 + e^{-T/\tau}) = V$$

Thus, $$V_1 = \frac{V}{1 + e^{-T/\tau}}$$

For a symmetric squarewave as $T_1 = T_2 = \frac{T}{2}$,

Therefore

$$V_1 = \frac{V}{1 + e^{-T/2\tau}}$$

But ' $V_1' = V_1 e^{-T/2\tau}$

$$V_1' = V \frac{e^{-T/2\tau}}{(1 + e^{-T/2\tau})}$$

There is a tilt in the output waveform. The percentage tilt is defined as

$$\% \text{ Tilt} = P = \frac{V_1 - V_1'}{V/2} \times 100\%$$

$$= \frac{\dfrac{V}{1 + e^{-T/2\tau}} - \dfrac{V e^{-T/2\tau}}{1 + e^{-T/2\tau}}}{V/2} \times 100\%$$

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If $\dfrac{T}{2\tau} \ll 1$

$$P \cong \dfrac{T}{2\tau} \times 100\% \quad \text{since } \dfrac{T}{2t} \ll 1$$

$$P = \dfrac{T}{2\tau} \times 100\%, \text{ for a symmetrical squarewave}$$

The lower cut-off frequency, $f_1 = \dfrac{1}{2\pi\tau}$

Therefore $\dfrac{1}{2\tau} = \pi f_1$

$$P = \pi f_1 T \times 100\%$$

Therefore, $P = \dfrac{\pi f_1}{f} \times 100\%$, since $T = \dfrac{1}{f}$

1.6 High Pass RC response for Ramp signal input.

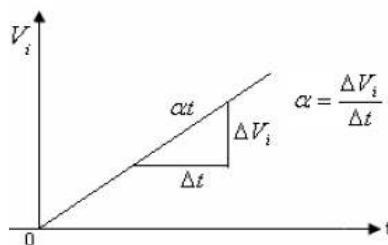(v) **Ramp input:** Ramp waveform is one which increases linearly with time for t> 0 and is zero for t<0.

fig.13 ramp input

Let the input to the high pass circuit be $V_i = \alpha t$ where α is the slope fig.13

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$$V_i = \frac{1}{\tau}\int V_o \, dt + V_o$$

$$\alpha t = \frac{1}{\tau}\int V_o \, dt + V_o$$

solving for V_o

$$V_o(t) = \alpha\tau\left[1 - e^{\frac{-t}{\tau}}\right]$$

If $\dfrac{t}{\tau} << 1$

$$e^{\frac{-t}{\tau}} = 1 - \frac{t}{\tau} + \frac{t^2}{2\tau^2}$$

Therefore $V_o(t) = \alpha\tau\left[1 - 1 + \dfrac{t}{\tau} - \dfrac{t^2}{2\tau^2}\right]$

$$V_o(t) = \alpha t\left[1 - \frac{t}{2\tau}\right]$$
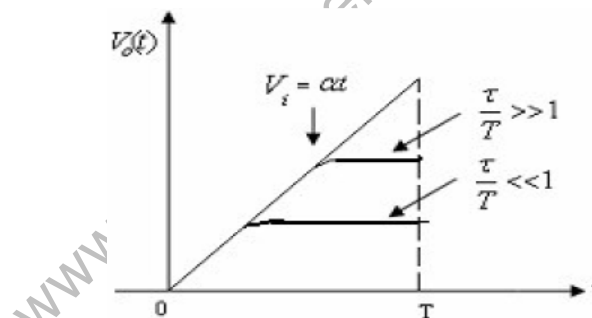
The output falls away from the input, fig.

Fig. 14 Response of a highpass circuit to ramp input

Transmission error is defined as the deviation from linearity and is given by

$$e_t = \frac{V_i - V_o}{V_i}$$

$$V_i = \alpha t$$

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At $t = T$, $V_i = \alpha T$, And $V_o = \alpha T\left(1 - \dfrac{T}{2\tau}\right)$

Therefore $e_t = \dfrac{\alpha T - \alpha T(1 - \dfrac{T}{2\tau})}{\alpha T} = \dfrac{\dfrac{\alpha T^2}{2\tau}}{\alpha T} = \dfrac{T}{2\tau}$

Thus, $e_t = \dfrac{T}{2\tau} = \prod f_1 T$ as $\dfrac{1}{2\tau} = \pi f_1$

1.7 HighPass RC Circuit as Differentiator

If the time constant of the RC highpass circuit is very much smaller than the time period of the input signal, then the circuit behaves as a differentiator. Then the voltage drop across R is very small when compared to the drop across C.
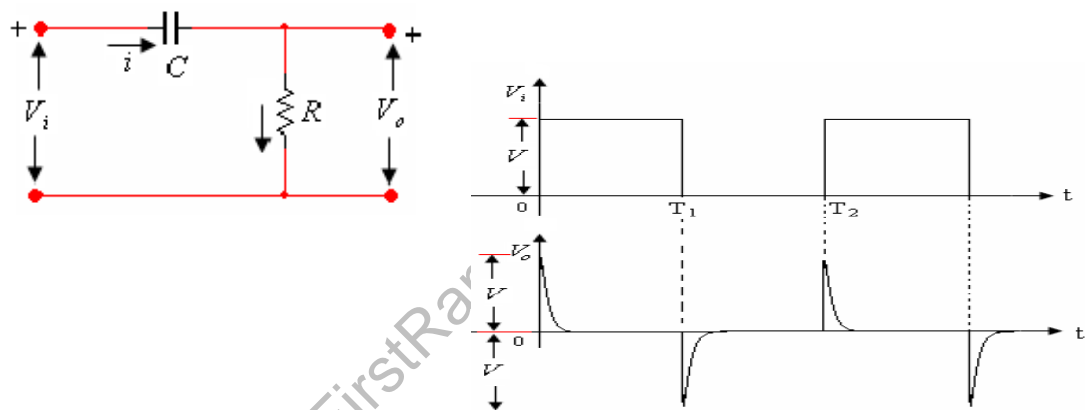

Fig.15 output of a differentiator

$V_i = \dfrac{1}{C}\int i\,dt + iR$

But $iR = V_o$ is small

Therefore $V_i = \dfrac{1}{C}\int i\,dt$

$i = \dfrac{V_o}{R}$

$\therefore V_i = V_i = \dfrac{1}{\tau}\int V_o\,dt = \dfrac{1}{\tau}\int V_o\,dt$

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Differentiating

$$\frac{dV_i}{dt} = \frac{V_o}{\tau}$$

$$V_o = \tau \frac{dV_i}{dt}$$

$$\therefore V_o \propto \frac{dV_i}{dt}$$

The output is proportional to the differential of the input signal.

LOWPASS CIRCUITS:

Introduction:

Low pass circuit is one which allows low frequencies with less attenuation and high frequencies with maximum attenuation. This is because capacitance offers high reactance at low frequencies and hence there is an output.

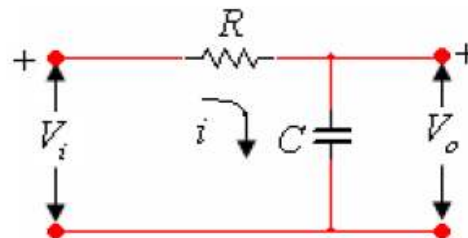**1.8 LOWPASS RC CIRCUIT:** Following is the low pass RC circuit.

Fig.16 Low pass RC Circuit

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At low frequencies the reactance of C is large and as frequency increases its Reactance decreases. Hence the output is larger for smaller frequencies and is smaller for larger frequencies. Hence this circuit is called a low pass circuit.

Consider the response of this circuit for different types of inputs.

1.9 Low Pass RC response for Sine signal input.

i) SINUSOIDAL INPUT: For the circuit shown above, if sinusoidal signal is applied as an input, the output Vo is given by

$$V_o = V_i \frac{\frac{1}{j\omega C}}{R + \frac{1}{j\omega C}}$$

$$\frac{V_o}{V_i} = \frac{1}{1 + j\omega CR}$$

$$\left|\frac{V_o}{V_i}\right| = \frac{1}{\sqrt{1 + (\omega CR)^2}} = \frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_2}\right)^2}} \qquad \text{,where } \omega_2 = \frac{1}{CR}$$

$$\text{At} \quad \omega = \omega_2, \quad \left|\frac{V_o}{V_i}\right| = \frac{1}{\sqrt{2}} = 0.707$$

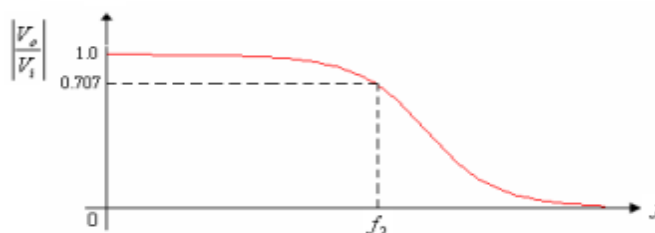Hence, f2 is the upper cut-off frequency as shown in the response curve below.

Fig.17 Response of low pass circuit to sinusoidal input

1.10 Low Pass RC response for Step signal input.

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(ii) STEP INPUT: When a step voltage is applied as input to the lowpass circuit the output will be appeared as shown in fig. below.
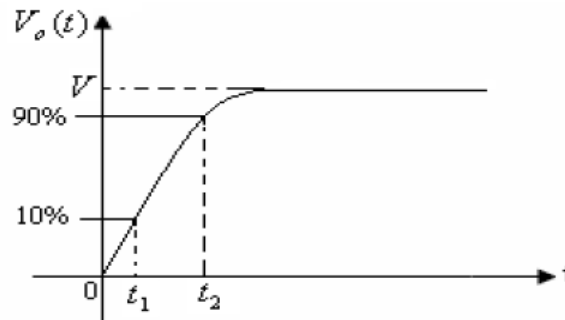

Fig.18 Response of lowpass circuit to step input

We have $RC = \tau$

$$V_o = V_f + \left(V_i - V_f\right)e^{\frac{-t}{\tau}}$$

Here, $V_f = V$ and $V_i = 0$

$$\therefore V_o(t) = V - Ve^{\frac{-t}{\tau}} = V\left(1 - e^{\frac{-t}{\tau}}\right)$$

As $t \to \infty$, $V_o(t) \to V$

On the other hand, the output can be obtained by solving the differential equation.

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$$V = V_i = Ri + \frac{1}{C}\int i\,dt$$

We know that $\quad \dfrac{1}{C}\int i\,dt = V_o$

$$\frac{i}{C} = \frac{dV_o}{dt}$$

$$i = C\frac{dV_o}{dt}$$

$$V = RC\frac{dV_o}{dt} + V_o$$

$$V = \tau\frac{dV_o}{dt} + V_o \qquad \text{Solving for}$$

$$V_o(t) = V_o = V - Ve^{\frac{-t}{\tau}} = V\left(1 - e^{\frac{-t}{\tau}}\right)$$

Rise time: The time taken for the output to reach from 10% of its final value to 90% of its final value is called rise time.

From equation

$$0.9 = 1 - e^{\frac{-t}{\tau}}$$

$$e^{-t_2/\tau} = 0.1$$

$$t_2 = 2.3\tau$$

Rise time $t_r = t_2 - t_1 = 2.3\,\tau - 0.1\,\tau = 2.2\,\tau$

Also $\quad f_2 = \dfrac{1}{2\pi RC}$

$$RC = \tau = \frac{1}{2\pi f_2}$$

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1.11Low pass RC response for pulse input:

Let the input of low pass rc is a pulse signal with pulse width T the response of low pass RC for pulse input under different conditions will be as follows.
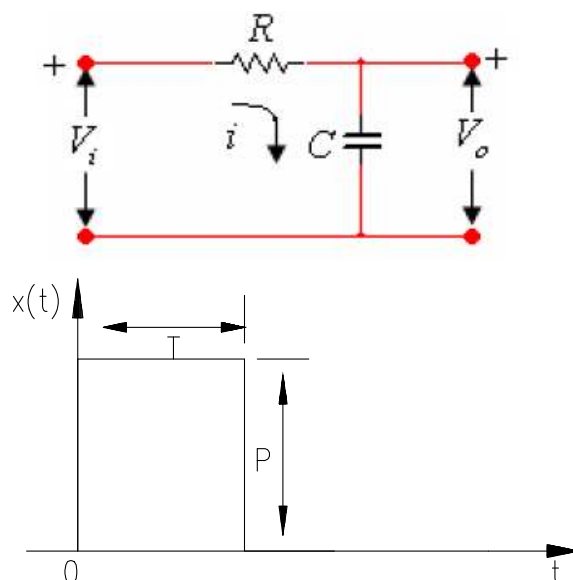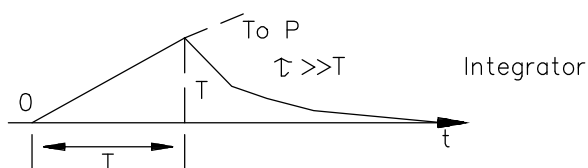

Fig.19 Input pulse to low pass RC

$$x(t) = p(1- e^{-t/\tau})$$

τ comparable to T

(HF Consideration)

$t_r = t_f \simeq 2.2\tau$

$\simeq 0.35/f_H$

$\tau <<T$

To P
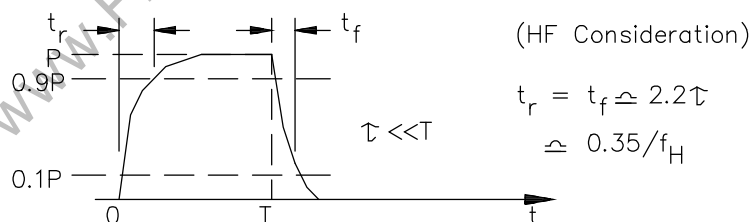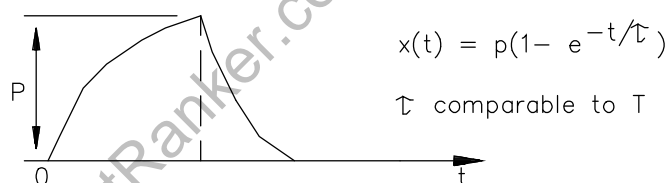
$\tau >>T$ Integrator

Fig.20 Response of low pass RC for pulse input under different conditions

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1.12 Response of low pass RC for square input:

The shape of the output waveform of an RC low-pass circuit depends upon the value of the circuit time constant T (as compared to pulse duration t_p). For a pulse waveform of the low-pass circuit may be short, long or medium as compared to t_p, the pulse duration of the input pulse wave. The output wave form for three different conditions for square wave input will be as follows .The conditions are $T << t_p$, $T = t_p$, $T >> t_p$.
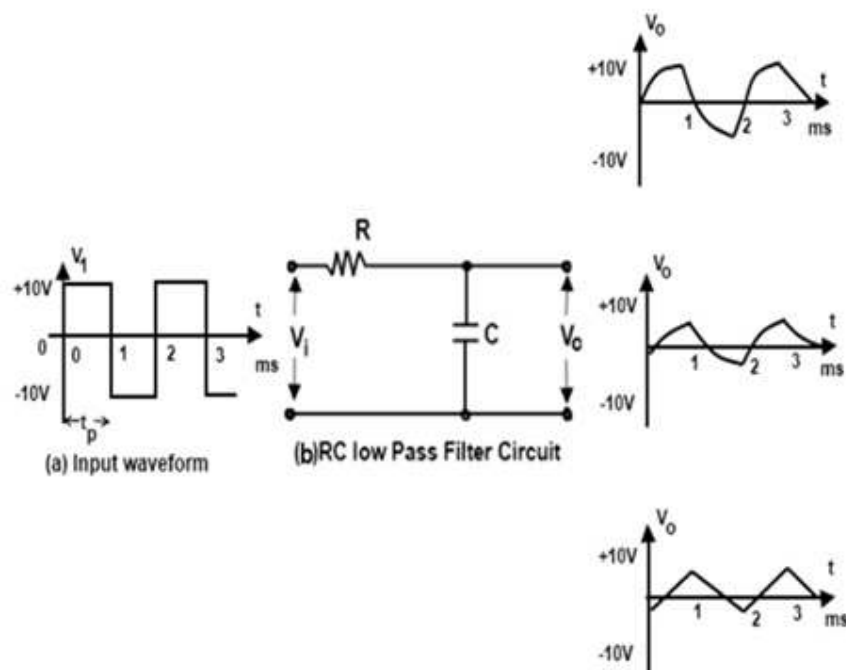

Fig.21 Response of low passes RC for square input

1.13 Response of Low pass circuit for ramp input:

When a ramp is applied as input to a lowpass circuit, the output deviates from the input which is defined as transmission error et. Mathematically it can be written as

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The input is a ramp
i.e. $V_i = \alpha t$

We have $V_i = \tau \dfrac{dV_0}{dt} + V_0$

$\therefore \alpha t = \tau \dfrac{dV_0}{dt} + V_0$

solving for output, we have

$V_o(t) = -\alpha\tau + \alpha t + \alpha\tau e^{-t/\tau}$

$V_o(t) = \alpha\left[t - \tau\left(1 - e^{-t/\tau}\right)\right]$

At $t = T$

$V_o(T) = \alpha\left[T - \tau\left(1 - e^{-T/\tau}\right)\right]$

Case 1 : If $\tau \ll T$, then the deviation of the output from the input is very small since

$e^{-T/\tau} \approx 0$
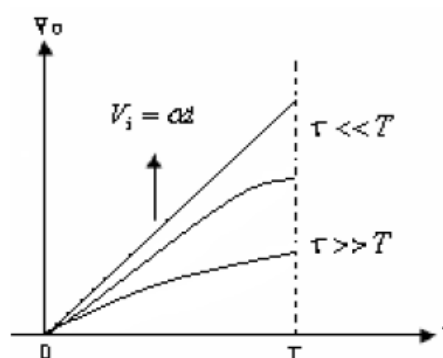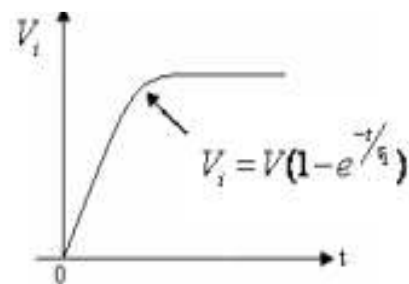
$V_o(t) = \alpha(T - \tau)$

Case 2: If $\tau \gg T$, then $e^{-T/\tau}$ can be expanded as series

$V_o(t) = \alpha\left[T - \tau\left(\dfrac{T}{\tau} - \dfrac{T^2}{2\tau^2}\right)\right]$

$= \alpha\left[T - T + \dfrac{T^2}{2\tau}\right] = \dfrac{\alpha T^2}{2\tau}$ $------$ 2.36

The response is plotted in fig. below

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$$e_t = \frac{V_i - V_0}{V_i}$$

$$= \frac{\alpha T - \alpha(T - \tau)}{\alpha T}$$

$$e_t = \frac{\tau}{T}$$

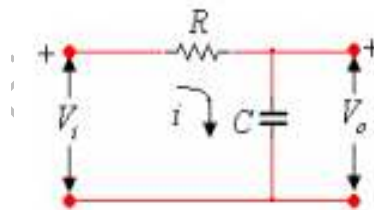$$f_2 = \frac{1}{2\pi\tau}$$

$$\tau = \frac{1}{2\pi f_2}$$

1.14 Low pass circuit as an integrator

For the low pass circuit to behave as an integrator $\tau >> T$ then the voltage Variation in C is very small

$$V_i = iR + \frac{1}{C}\int i\,dt$$

$$V_i \cong iR$$

Since, $\frac{1}{C}\int i\,dt << iR$
,

$$i = \frac{V_i}{R}$$

Therefore $V_o = \frac{1}{C}\int i\,dt = \frac{1}{RC}\int V_i\,dt = \frac{1}{\tau}\int V_i\,dt$

The output is proportional to the integral of the input signal.

Hence a low pass circuit with large time constant produces an output that is proportional to the integral of the input.

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1.15 Attenuators:

An attenuator is a circuit that reduces the amplitude of the signal by a finite amount. A simple resistance attenuator is as shown below.
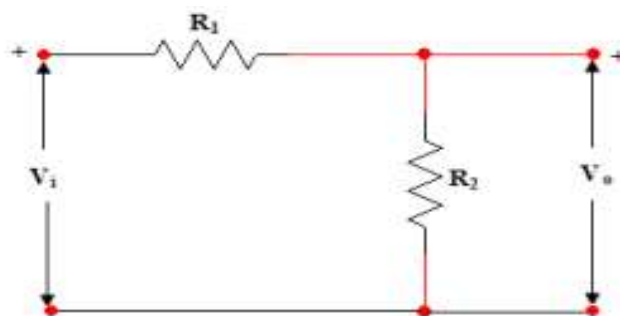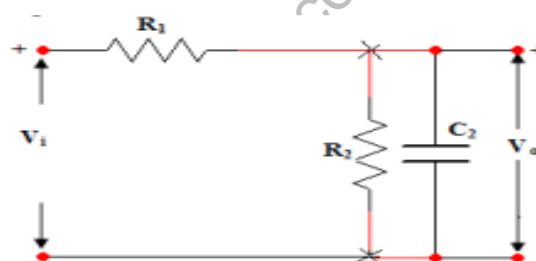

Fig.22 Resistive Attenuator

The output is reduced depending on the choice of R1 and R2. The output of this attenuator can be connected as input to an amplifier having a stray capacitance C2 and input resistance Ri.If Ri>>R2, then the effective value of resistance will be smaller than R2. The attenuator circuit will be now as

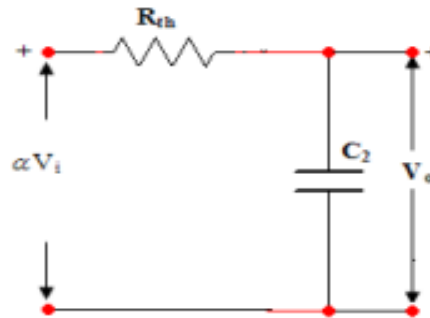Reducing the two loop network into a single loop network by Thevenizing

$$V_{Th} = V_i \times \frac{R_2}{R_1 + R_2} = \alpha V_i \quad where \ \alpha = \frac{R_2}{R_1 + R_2}$$

and

$$R_{th} = R_1 // R_2$$

Hence the above circuit reduces to

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When the input αV_i is applied to this low pass RC circuit, the output will not reach the steady-state value instantaneously. For e.g. in the above circuit, R1=R2=1M and C2 = 20nF.Then the rise time t_r = 2.2RthC2=$2.2 \times 0.5 \times 10^6 \times 20 \times 10^{-9}$,tr = 22msec. which says that approximately after a time interval of 22 msec. after the application of the input αV_i to the circuit, the output reaches the steady state value. Obviously this is an abnormally long time delay. An attenuator of this type is called an uncompensated attenuator and the response is depending on frequency. To make the response of the attenuator independent of frequency, capacitor C1 is shunted across R1. This attenuator now is called a compensated attenuator as shown in fig.a, and the same is redrawn as in fig.b
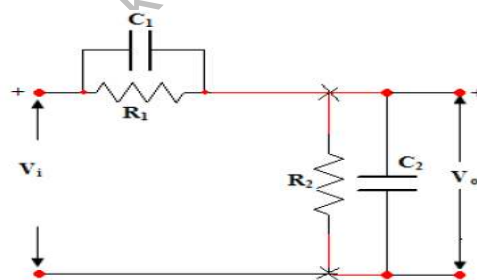
fig.a Compensated Attenuator
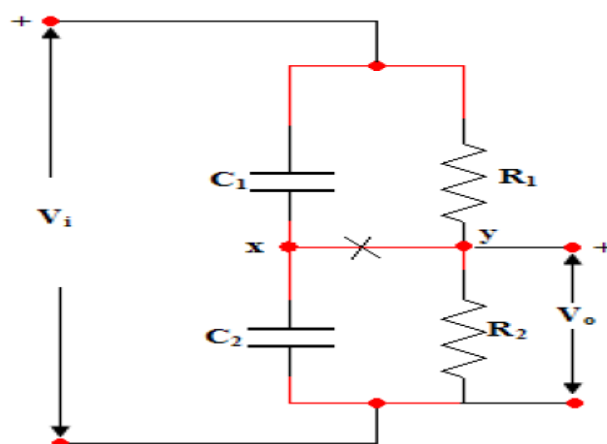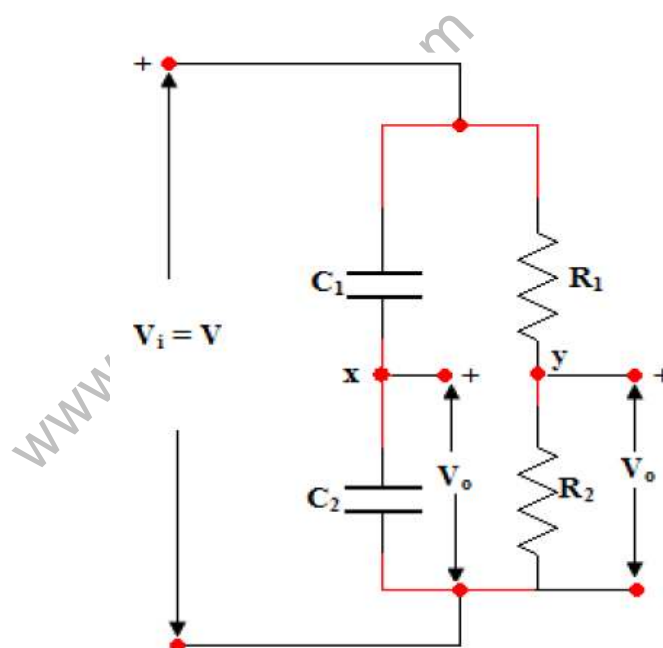
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fig.b Compensated attenuator

R1,R2,C1,C2 form four arms of the bridge. The bridge is said to be balanced when R1C1=R2C2.Then no current flows in the branch xy. Hence for the purpose of computing the output, branch xy is omitted. The resultant circuit is

When a step voltage Vi=V is applied as input, the output is calculated as follows:

At t=0+, as the capacitors will not allow any sudden changes in voltage, as the Input changes the output also should change abruptly, depending on the values of C1 and C2.

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$$V(0^+) = V\frac{C_1}{C_1 + C_2}$$

Thus, the initial output voltage is determined by C1 and C2.

As t→∞, the capacitors are fully charged and they behave as open circuits for dc.

Hence the resultant output is

$$V_0(\infty) = V\frac{R_2}{R_1 + R_2}$$

Perfect compensation is obtained if, Vo(0+)=Vo(∞)

$$\frac{C_1}{C_1 + C_2}V = V\frac{R_2}{R_1 + R_2}$$

2

From this we get

C1R1=C2R2,or C1=(R2/R1)C2=Cp
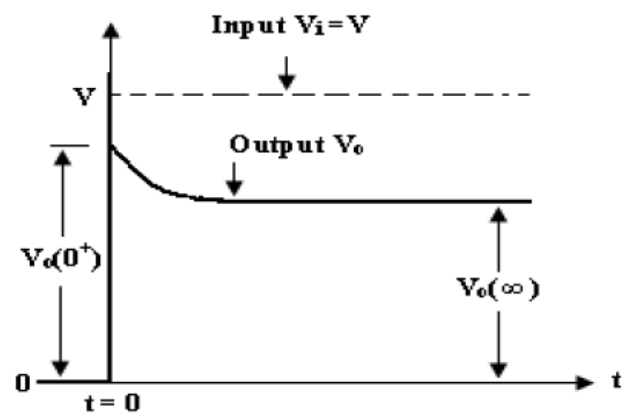
and the output is αVi

Hence following conditions(cases) arise.

(i) When C1=Cp, the attenuator is a perfectly compensated attenuator.

(ii) When C1>Cp , it is an over-compensated attenuator and

(iii) When C1<Cp , it is an under-compensated attenuator.

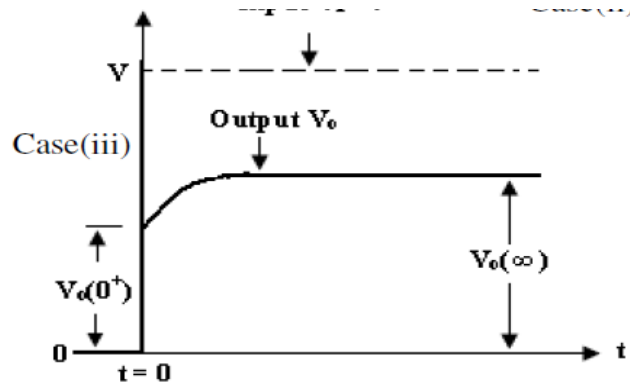The responses of the attenuator for step input are shown in the following fig.
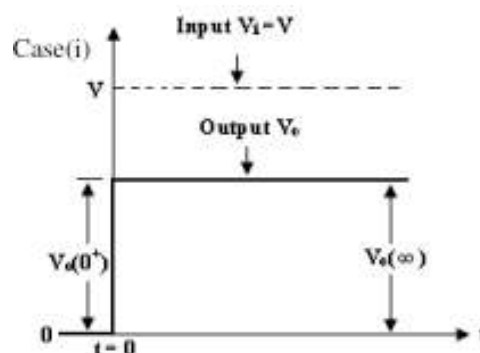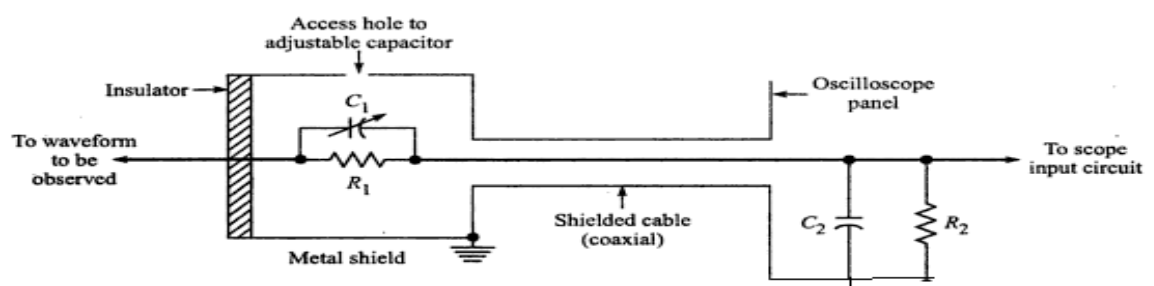
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Case(ii)

case(iii)

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1.16 Application of attenuator as a CRO probe:

To measure the signal at a point in the circuit, the input terminals of the oscilloscope are connected to the signal point. Normally the point at which the signal is available will be at some distance from the oscilloscope terminals and if the signal appears at a high impedance level, a shielded cable is used to connect the signal to the oscilloscope. The shielding is necessary in this case to isolate the input lead from stray fields such as those of the ever-present power line. The capacitance seen looking into several feet of cable may be as high as 100 to 150 pF. This combination of high input capacitance together with the high output impedence of the signal source will make it impossible to make faithful observations of waveforms. A *probe* assembly, which permits the use of shielded cable and still keeps the capacitance low, is indicated in Figure 1.64.

1.17 RL and RLC Circuits and their response for step input.
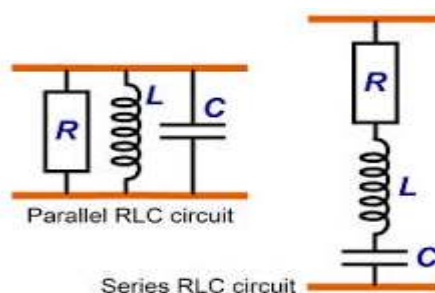
RL circuit:

RL circuit is similar to RC circuit the circuit diagram represents RL circuit will be as follows it can be acts as high pass RL and low pass RL also.
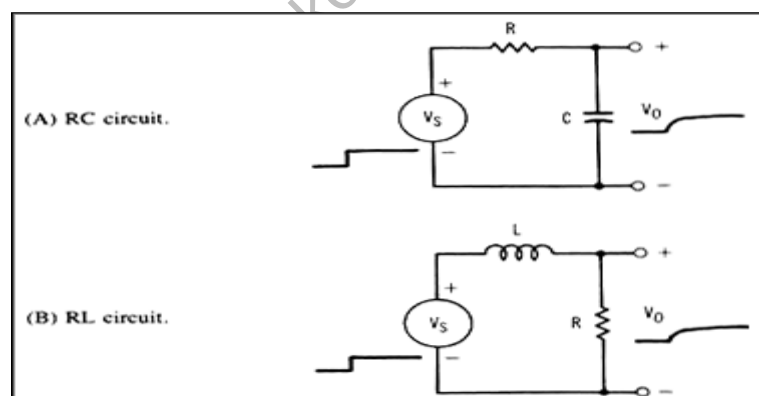
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RLC circuits:

There are two types of RLC circuits series RLC and parallel RLC will be as follows.

Parallel RLC circuit

Series RLC circuit

Step response of RL and RLC circuits:

$$T(s) = \frac{\tilde{V}_{out}(s)}{\tilde{V}_{in}(s)}\Bigg|_{ZERO\ IC} = \frac{\frac{1}{sC}}{sL + R + \frac{1}{sC}} = \frac{1}{LC} \cdot \frac{1}{s^2 + s \cdot \frac{R}{L} + \frac{1}{LC}}$$

poles of $s^2 + s \cdot \frac{R}{L} + \frac{1}{LC} = 0$ 	 $P_{1,2} = -\frac{R}{2L} \pm \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}}$

case1 	 $\frac{R^2}{4L^2} > \frac{1}{LC}$, i.e. $R > 2\sqrt{\frac{L}{C}}$ 	 poles are real and different

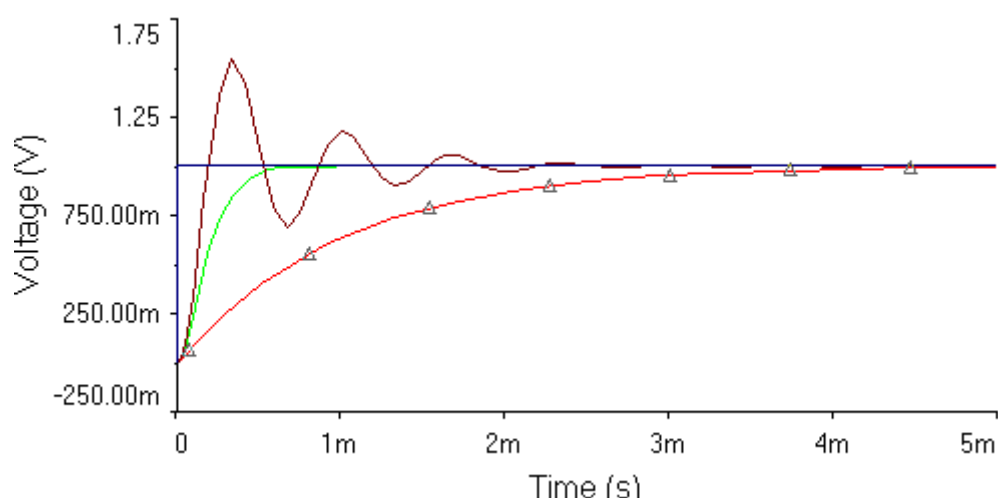case2 	 $\frac{R^2}{4L^2} = \frac{1}{LC}$, i.e. $P_1 = P_2 = -\frac{R}{2L}$ 	 poles are real and equal

case3 	 $\frac{R^2}{4L^2} < \frac{1}{LC}$, i.e. $R < 2\sqrt{\frac{L}{C}}$ 	 poles are imaginary

By solving above three cases we get the output as the waveforms which are under damped ,crictical damped and overdamped waveforms.

The output waveforms will be as follows.

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Fig. Response of RLC for step input.

1.18 Ringing circuit:

A circuit which provides un damped oscillations is called ringing circuit. If the damping is very small circuit rings for many cycles.for this circuit Q=π N.if Q=12,circuit will ring for 4 cycles

Important Questions:

1. What is linear wave shaping?

2. What are linear elements give suitable examples?

3. What are linear wave shaping circuits?

4. What is high pass RC? explain how it acts as differentiator?

5. What is low pass RC? explain how it acts as integrator?

6. What is the time constant of RC circuit?

7. Draw the responses of high pass RC for STEP,PULSE,SQUARE inputs?

8. Draw the responses of low pass RC for STEP,PULSE,SQUARE inputs?

9. What is transmission error? how it can be defined?

10.What is attenuator? give its applications?

# Pulse & Digital Circuits

2. <u>Non-Linear Wave Shaping</u>

<u>Syllabus:</u>

Diode clippers. Transistor Clippers. Clipping at two independent levels. Comparator – Applications of voltage Comparators – Diode Comparator. Clamping Operation. Clamping Circuits using Diode with Different Inputs. Clamping Circuit Theorem. Practical Clamping circuits. Effect of diodeCharacteristics on Clamping Voltage.

2.1 Diode clippers:

Basic Description

As you know, diodes can be used as switches depending on the biasing type, reverse of forward. The clipping circuit also referred to as clipper, clips off some of the portions of the input signal and uses the clipped signal as the output signal.
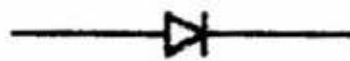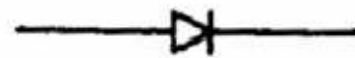
Forward turning-on   Reversely turning-off

Switch is closed   Switch is opened

Ideal Diode – Switch Terminology

2.1. a Clipper Circuits

There are two types of clipper circuits, the series and parallel diode clipping circuits.

2.1 a.1 Series Diode Clipping Circuit

In these types of circuits, the diode is connected between the input and output voltage terminals

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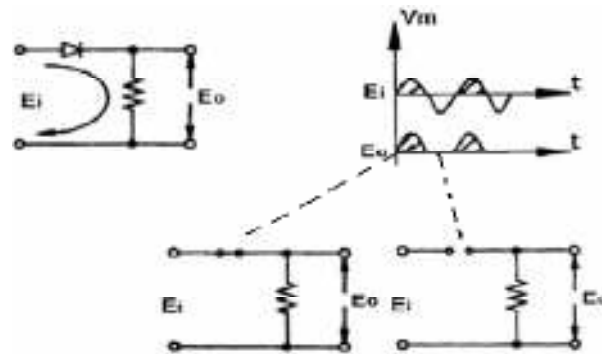
Fig: series negative clipper

As **Fig** reveals, the negative cycle of the input voltage can be clipped of by this type of series clippers. Reverse of the diode pins yields to a positive cycle clipping circuit as shown in **Fig.**
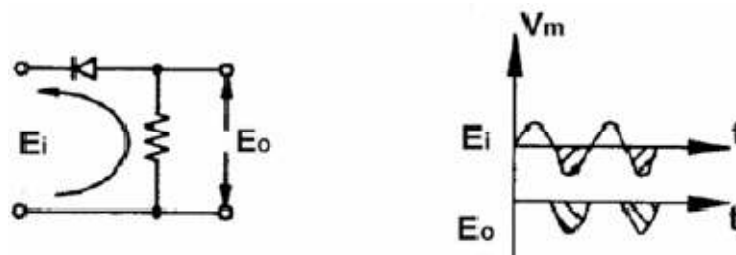
Fig. series positive clipper

Diode operation as short and open circuits

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Diode clippers using bias

Previous circuits clip the values larger or smaller than zero voltage. This voltage, technically called "threshold voltage" and can be changed to a desired value by inserting a D.C. voltage source. This is achieved in two different ways.
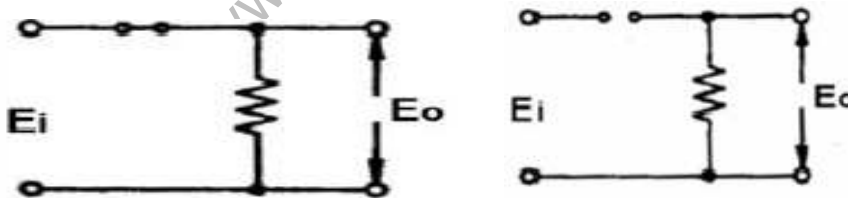
In the first type, the voltage source of **Em** (positive or negative) is connected through output terminals as in **Fig** Depending on the diode connection (normal12 or reverse), the values smaller **or** greater **than Em** is clipped and assigned as **Em.**
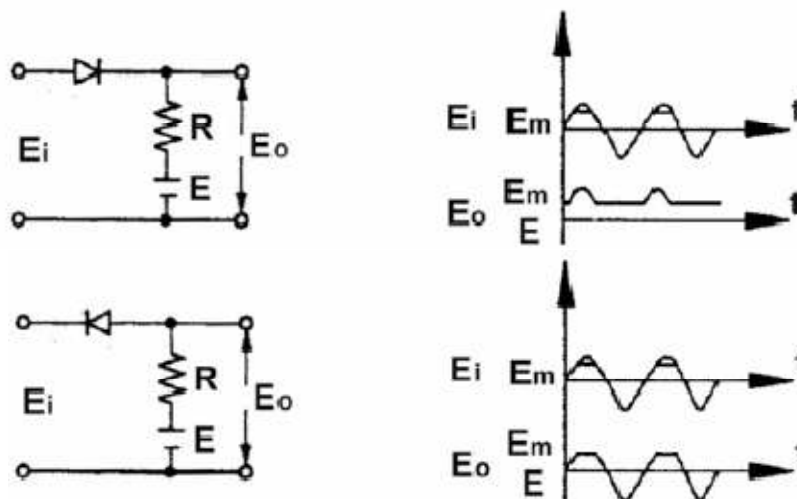
Note that if **Em** is negative, (where the voltage source is reversely connected) again the values smaller or larger than this negative value are clipped.

Parallel Diode Clipping Circuit

In this type of clippers, the diode is connected between output terminals. The on/off state of diode directly affects the output voltage. These types of clippers may also have a non-zero threshold voltage by addition of a voltage series with diode.

Following figures illustrate the clipping process
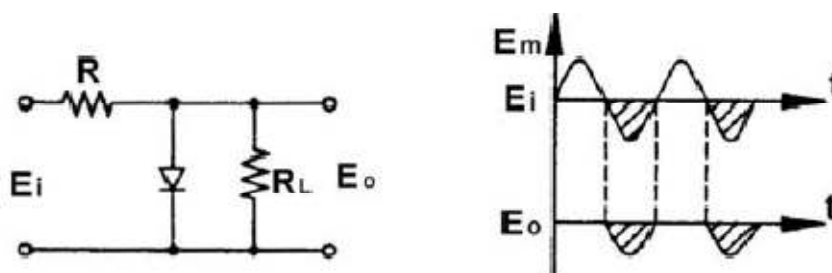
Pulse & Digital Circuits
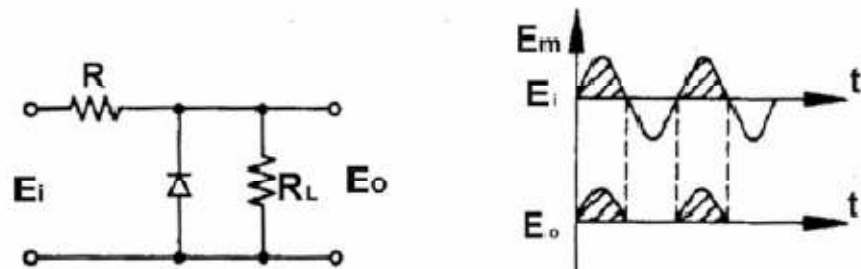
Fig. Zero Threshold Parallel Clippers
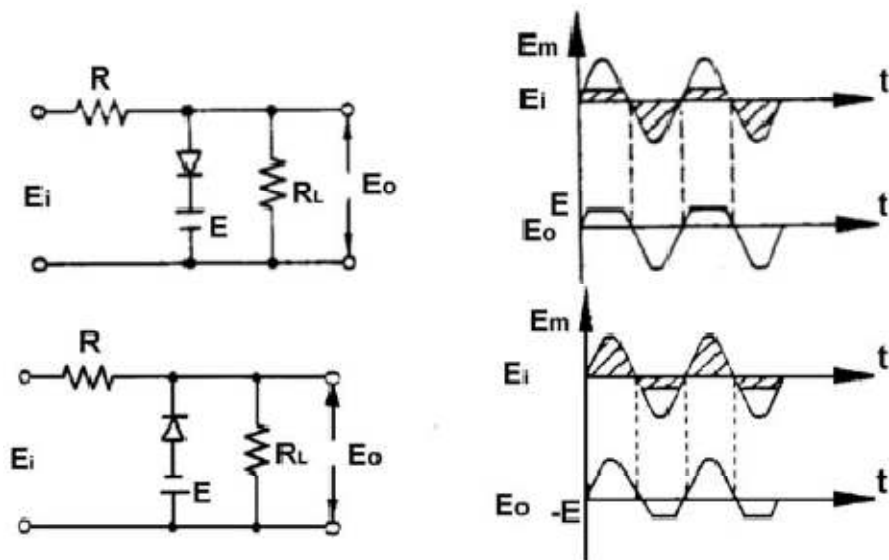
Fig .Threshold Parallel Clippers

2.2 Double Diode Clipping

In single diode clipping circuit, the wave form is selected either above or below (but not on both sides) reference level. Two diode clippers may be used in parallel, series, or series-parallel to limit the output at two independent levels.

Consider the circuit in Fig. side

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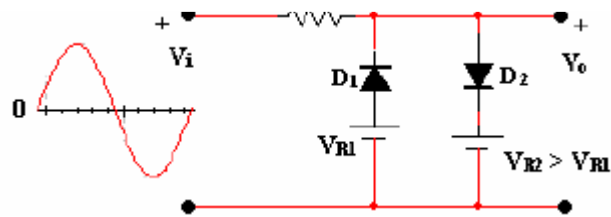
The transfer curve has two break points, one at Vo = Vi = VR1 and

a second at Vo = Vi =VR2 has the following characteristics Vo

Input voltage	Output voltage	Diode states
Vi >VR2,	Vo =VR1	D1 is OFF and D2 is ON,
Vi < VR1,	Vo =Vi	D1 is ON D2 is OFF,
VR1 < Vi < VR2,	Vo =VR2	D1 and D2 are OFF.

Transfer characteristic of the slicer with input and output
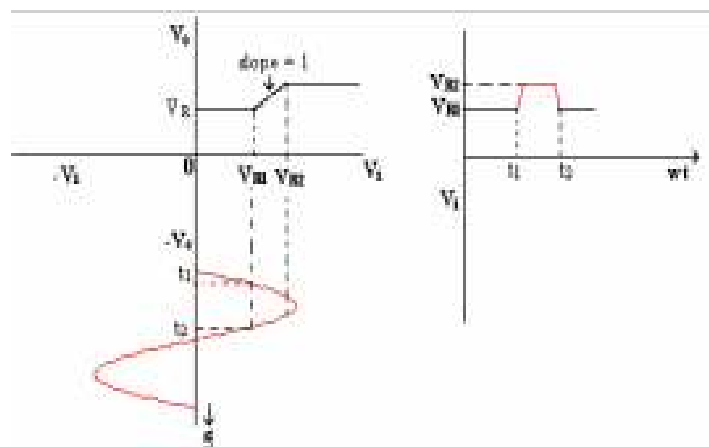
A combination of a positive peak clipper and a negative peak clipper, clipping the input symmetrically at the top and the bottom is called a limiter
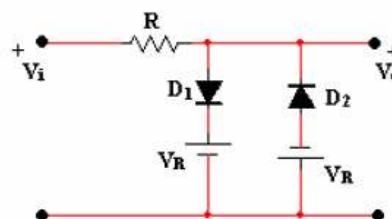
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The resultant transfer characteristic is as shown below.
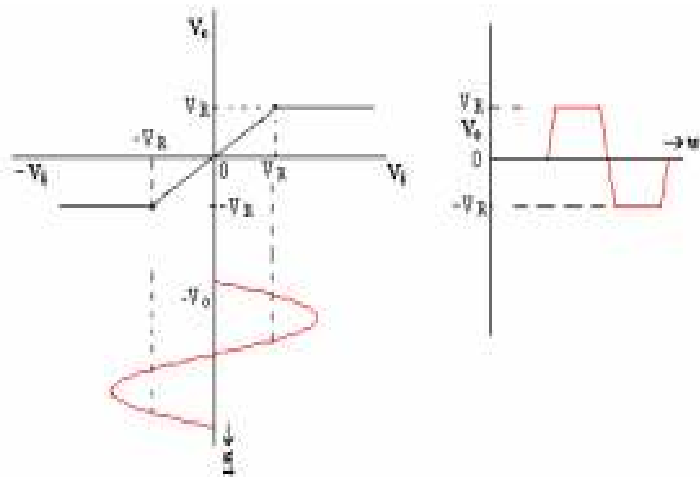
Fig.Transfer characteristic of a Limiter with input and output

Two avalanche diodes in series opposing, as indicated in fig below constitutes another form of double-ended clipper. If the diodes have identical characteristics then a symmetrical limiter is obtained.If the breakdown (zener) voltage is VZ and if the cut in voltage in the forward direction is Vy, then the transfer characteristic is as shown below. Transfer characteristic
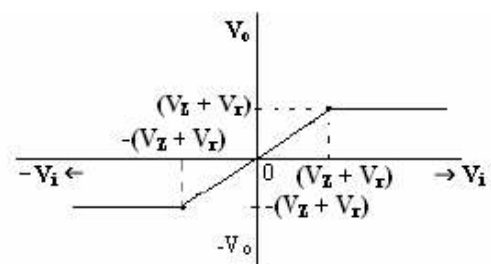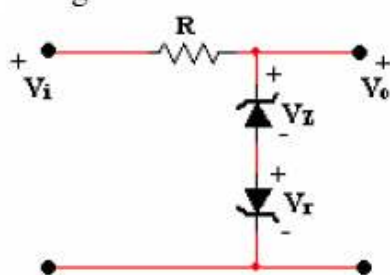
Transfer characteristic

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2.3 Transistor clippers:

Emitter-coupled transistor clipper:

Consider initially that the input voltage Vi is negative enough to ensure that Q1 is in cutoff .Then only Q2 is carrying current. Consider that VBB has been adjusted so that Q2is in its active region. As Vi increases Q1 will eventually come out off cutoff, both transistors will be carrying current and the input signal will appear at the output, amplified but not inverted. As Vi continues its excursion in the positive direction the common emitter will follow the base of Q1.The base of Q2 is fixed, a point will be reached when the rising emitter cuts off Q2 .Finally, the input signal is amplified but twice limited, once by the cutoff of Q1 and once by the onset of cutoff in Q2.
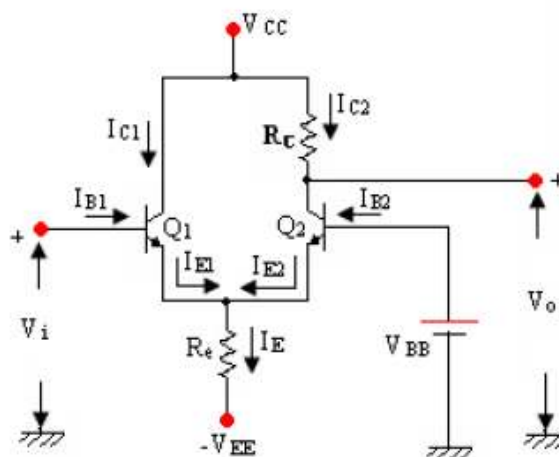
Fig.A two-level transistor clipper

The transfer characteristic is shown in fig below. Thus this circuit behaves as a two-level clipper. The region of linearity can be controlled by the choice of VBB.

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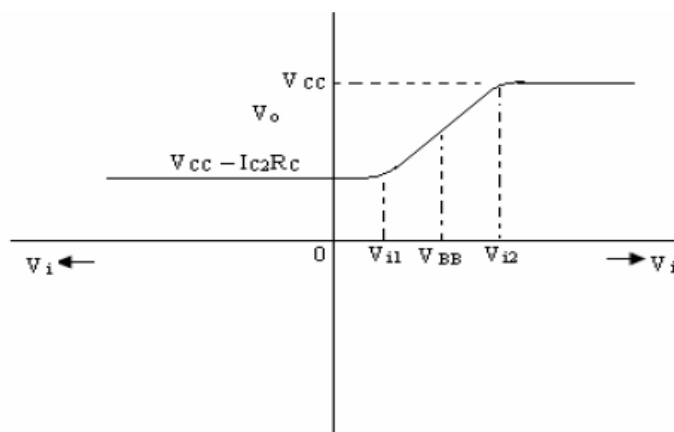
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2.4 COMPARATORS:

A comparator circuit is one which may be used to mark the instant when an Arbitrary waveform attains some reference level. Consider the simple clipping circuit for comparison operation.

For the sake of explanation let the input signal be a ramp as shown below.

This input crosses the voltage level vi = V_R at time t = t1.

The output remains quiescent at vo = V_R until t = t1 after which it rises with the input Signal

Fig Diode comparator
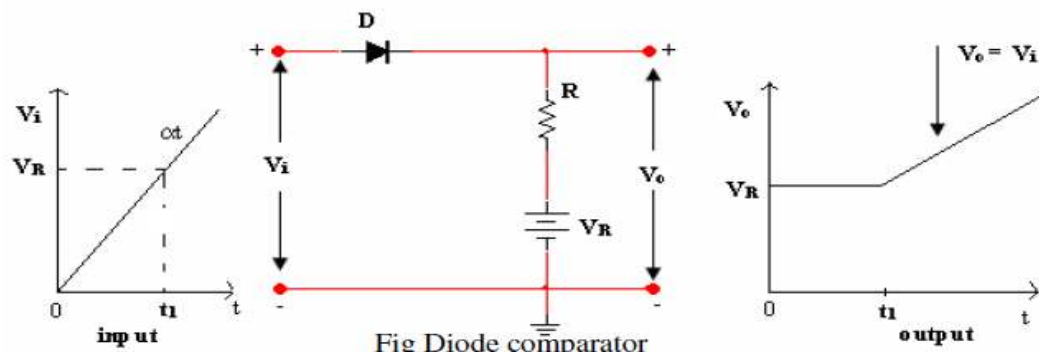
There is a sudden change in the slope of the output at the instant the input reaches V_R.

But due to ageing and due to temperature variations the diode, may not switch from

OFF to ON at exactly t = t1 .It may switch state at any instant after t1 and before t2.

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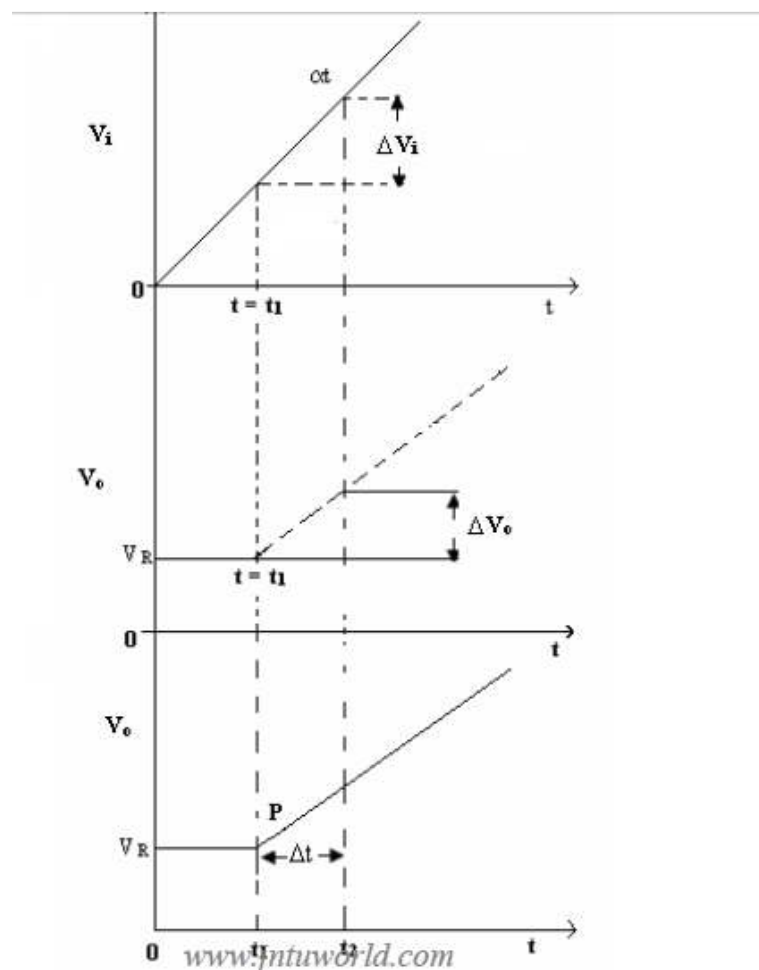
Input and output of the diode comparator

Hence, the break point (point at which device D changes state) may not exactly be at t1 but instead, there is a break region (t1 to t2).. Hence, there is a region of uncertainty which also, after the break point, the output follows the input i.e. has the same slope of the input. If this region of uncertainty is to be reduced, the response after the break point should be sharp. To achieve this amplifier may be placed before or after the comparator.

Consider the comparator circuit the response .To the left of the break point, the diode is OFF then the reverse incremental resistance of the diode, Rr is very much larger when compared to R. To the right of the break point the forward incremental resistance of the diode, R_f is very much smaller than R. If the break point is located at a point where r = R.

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$$\Delta V_o = \Delta V_i \frac{R}{r+R} \approx V_i \quad \text{if } R \gg r$$

$$\text{As } \Delta V_o = \Delta V_i \frac{R}{r+R}$$

$$\text{if } r = R$$

$$\therefore \quad \frac{\Delta V_o}{\Delta V_i} = \frac{R}{R+R} = \frac{1}{2}$$

So the improvement is only half.

If a device is connected at the output of the comparator, this is required to be activated when the diode current is say, I and has a drop across R as IR.

If now an amplifier is connected at the output of the comparator so that this amplifier output activates the device.

Let the amplifier have a gain A. During $\Delta t = t2 - t1$, the output changes by

$\Delta Vo = V_2 - V_R$, the delay in response is reduced to

$$\frac{\Delta t}{A} \quad or \quad \frac{(t_2 - t_1)}{A}$$
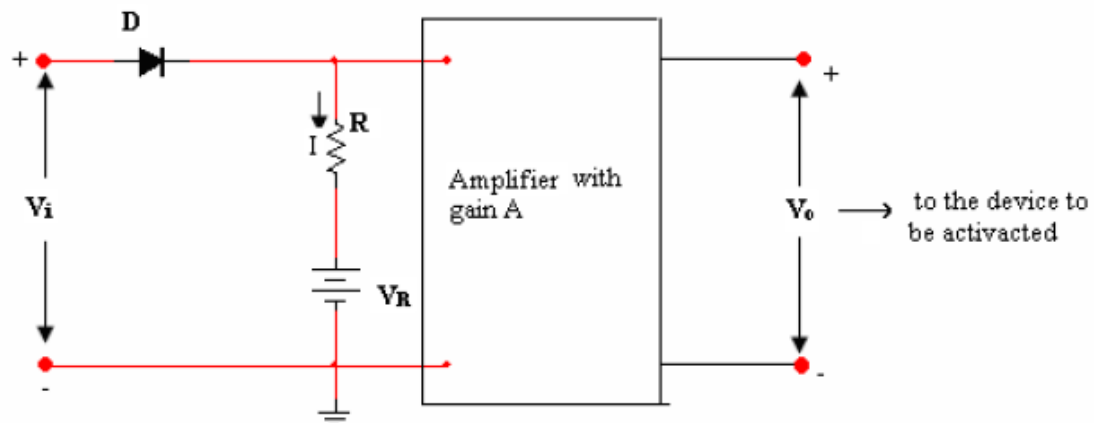
Output of the comparator connected to an amplifier

Let the amplifier only amplify the change in the comparator input but not the reference voltage. The device to be activated is activated only when the drop across R is IR But now I = I/A, Hence the device is activated when the drop across R is RI/A since the diode current is amplified by A and the diode resistance i.e the dynamic resistance which varies inversely with current. Therefore it is evident that, the device to be activated by the

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comparator will respond at a current such that r = RA

$$\therefore \frac{\Delta V_o}{\Delta V_i} = A \frac{R}{r+R} = \frac{AR}{R+RA} = \frac{A}{1+A}$$

$$\text{As } A \to \infty, \quad \frac{\Delta V_o}{\Delta V_i} \to 1$$

Without an amplifier $\frac{\Delta V_o}{\Delta V_i}$ the transmission gain) was ½ and with an amplifier connected,

$\frac{\Delta V_o}{\Delta V_i}$ is 1. Which says that there is no marked improvement in the response of the comparator arrangement.

2.5 Some applications of comparators:

(i)   **Measurement of time delays:**

In the comparator shown before, if V_{R1} is the reference level in the first comparator (double differentiator) then a pulse is generated with a peak at t = t1. If V_{R2} is the reference level set in a second comparator then the pulse is generated with peak at t = t2.

Then the time difference between the two pulses is simply

$$t2 - t1 = (V_{R2} - V_{R1})/\alpha$$

(ii)   **Timing markers generated from sine wave:**

If a sine wave is applied as input, when the input reaches VR output of the comparator is high till again the input reaches VR. Differentiate and clip negative spikes. We have positive spikes which can be implemented as timing markers.

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(iii) **Phase meter:** Let two sinusoidal inputs having a phase difference be applied to a comparator whose reference voltage is zero.

Fig.The output pulses are differentiated and the time difference between the outputs spikes is proportional to the phase difference.
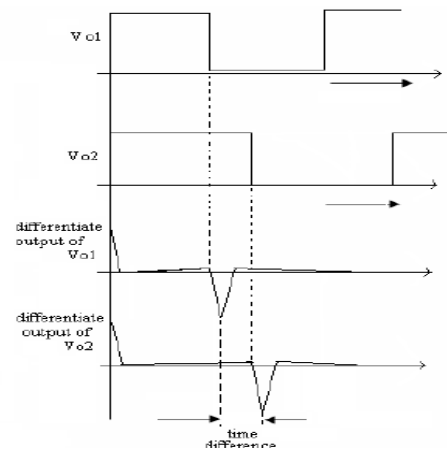
(iv) **Square waves from sine waves**: In regenerative comparator (Schmitt trigger) if the reference voltage is + Vref, the output goes to +V or –V

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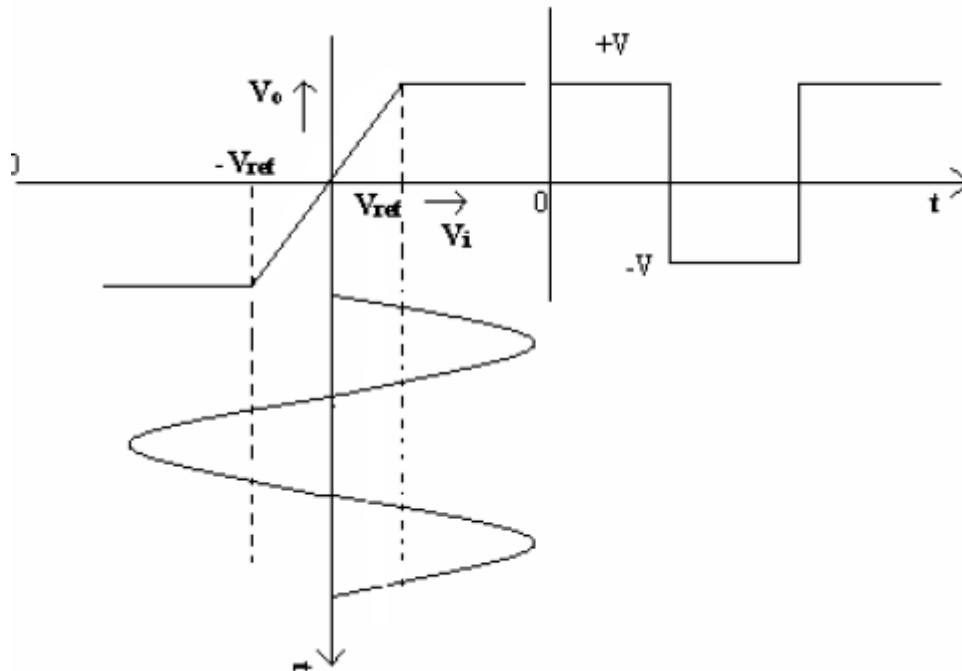
NON-LINEAR WAVESHAPING - CLAMPING CIRCUITS

2.6 clamping operation:

Introduction:

The establishment of extremity of positive or negative signal excursion at some reference level V_R is called Clamping. Clamping circuits introduce the dc component lost during transmission through a capacitive coupled network. Circuits that clamp the positive peak of the signal to zero level are called negative clampers and those that clamp the negative peak of the signal to zero level are called positive clampers. If a non-sinusoidal periodic signal is transmitted through a network having capacitive coupling, the dc component in the output is lost since the capacitor blocks the dc. If there arises the need once again that dc component is to be restored, this is done by a clamping circuit. A clamping circuit is, therefore, called a dc restorer or dc reinserted. As such, the output can be referenced to any arbitrarily chosen reference level.

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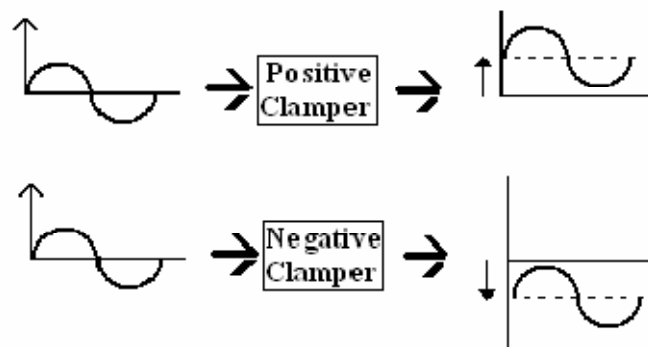
The clamping circuit:

The circuit in fig below is the basic clamping circuit.
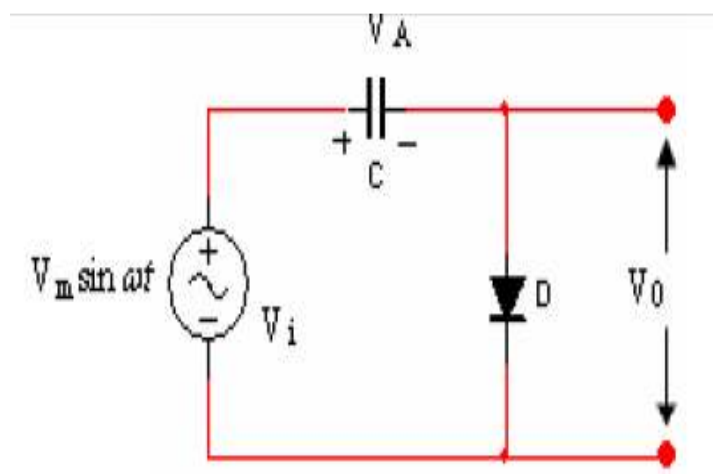
Fig. Negative Clamping circuit

As the input rises from 0 to Vm in the first quarter cycle fig.4.2a, C charges to Vm. During this period, V0 = 0. i.e. the output is zero for the first quarter cycle since D conducts. The input falls after the first quarter cycle. Vi<Vm, the charge on the capacitor. As a result the diode is reverse biased by a voltage (Vi -Vm). Hence D is OFF.

V0=Vi - Vm -------- 1

The voltage across C remains unchanged.

From equation .1----.If Vi = 0, V0 = -Vm

And if, Vi = -Vm , V0 = -Vm - Vm = -2Vm

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During the next cycle, the positive peak of the output just reaches the zero level. Hence in the output, the positive peak is clamped to zero level and this is repeated for succeeding cycles. The input, output waveforms are represented in fig.2
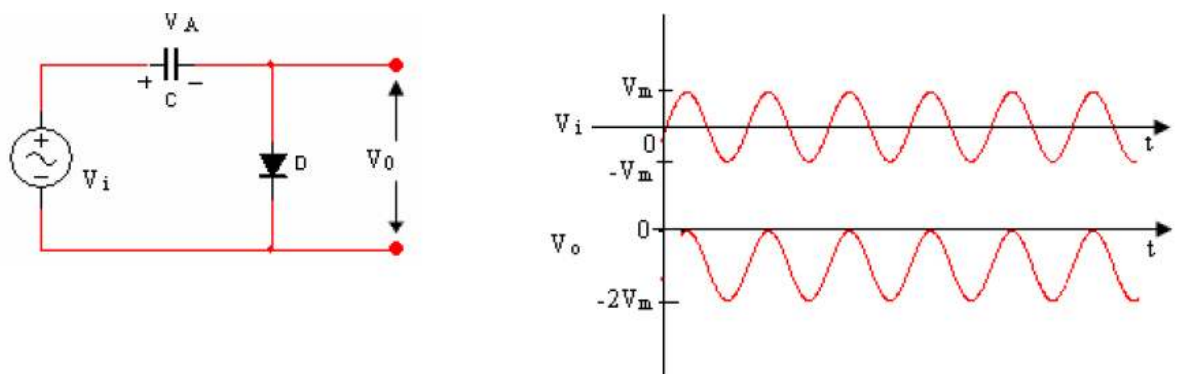
Fig.2 input – output waveforms of negative clamp

The input to this circuit is a sinusoidal with zero reference level. The output is referenced to – Vm and the positive peak is clamped to zero. When the input decreases, to clamp the positive peak to zero level, the voltage across the capacitor should change to the peak amplitude of the new input. But there is no discharge path for the capacitor to discharge. For this a resistance R is provided in shunt with the diode D fig.3
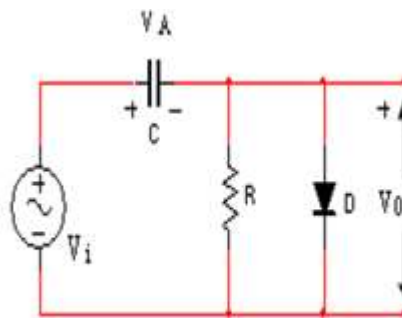
Fig. clamping circuit with R shunted across diode D

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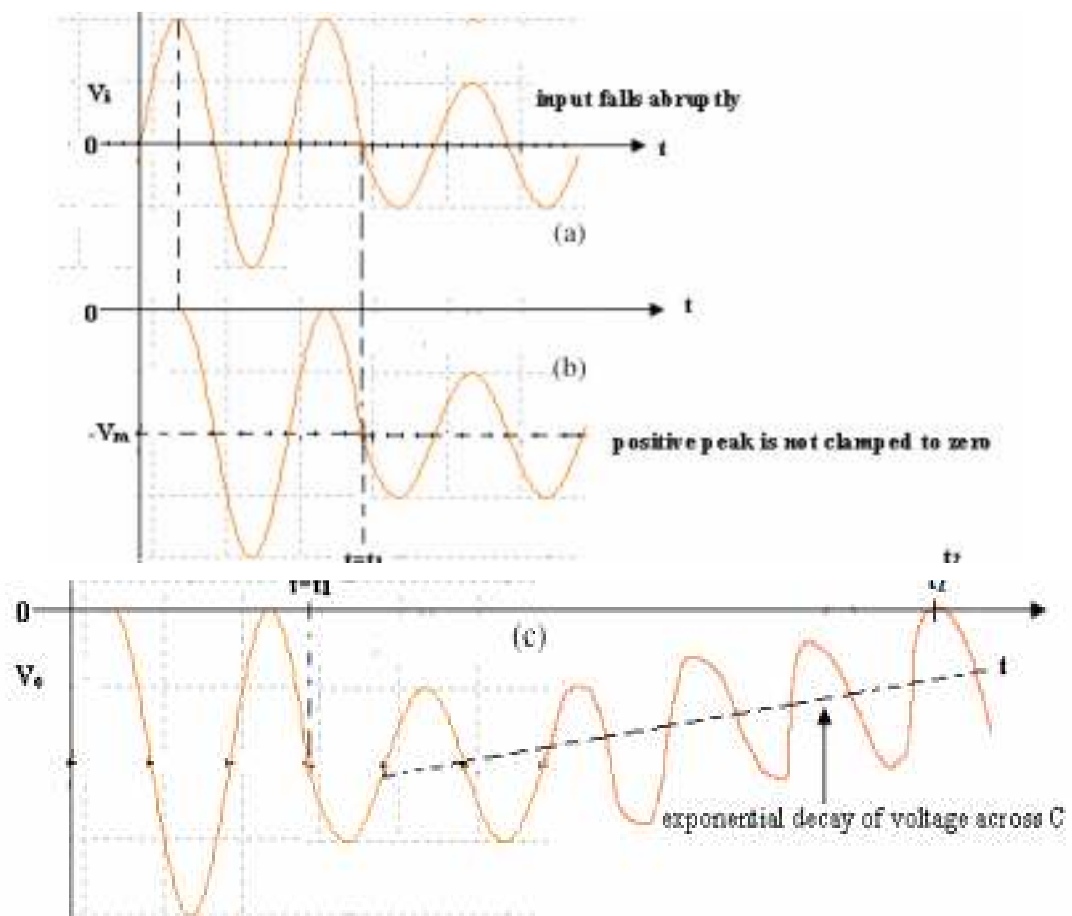
Fig. a) input b) Output when R = ∞ c) output with finite R

At t = t1, if the input amplitude is abruptly reduced, as the voltage across the capacitor cannot change instantaneously, the positive peaks will not reach zero level. But now as the charge on C is going to discharge, as the voltage across the capacitor varies exponentially with a time constant τ=RC, the output reaches zero level at t = t2, the positive peak is again clamped to zero, after few cycles
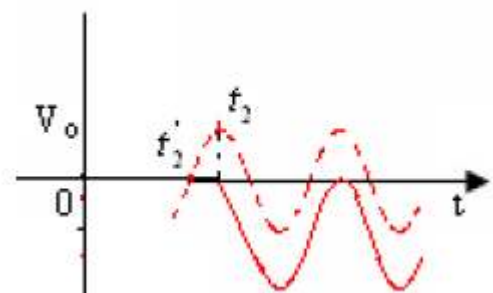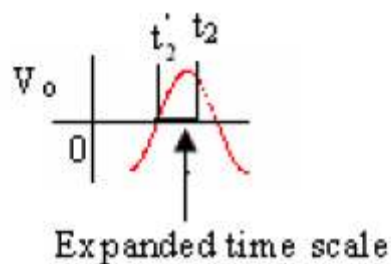
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Fig. Output with expanded time scale in the neighborhood of a positive peak

In the vicinity of a positive peak D conducts and at t = 't , V0=0. If there were to be no diode, the output should have followed the dashed line with the peak at t = t2. But because of the diode, the output in zero from 't_2' to t2 and in the subsequent cycles the positive peaks of the sinusoidal are clamped to zero.

2.7 Clamping circuit theorem:

Under steady state conditions the area under the forward biased condition and the area under the reverse biased condition are related as $A_f/A_r=R_f/R$

proof:

for forward biased condition charging of capacitor can be done and charge stored on capacitor is $Q1= A_{f/} R_f$.

for reverse biased condition discharging of capacitor can be done and CHARGE LOST BY capacitor is $Q2= A_r/R$.

under steady state conditions charge gained by the capacitor equal to charge lost hence we can get

$$A_f/A_r=R_f/R$$

2.8 Clamping circuit with diode and source resistances:

Consider now the internal resistance of the source, R_S.as shown in Fig.
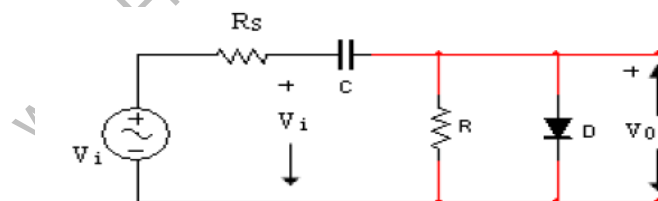
When the input is applied, the output reaches the steady-state value after a few cycles and the positive peaks are clamped to zero. Consider the equivalent circuits

    (i)   When the diode is ON,

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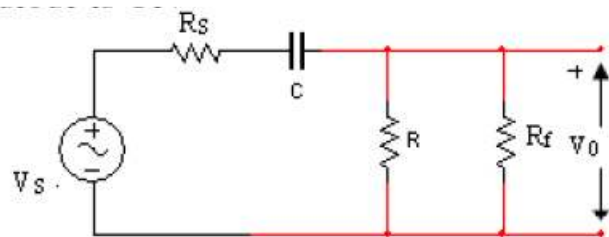
Fig.ii) Circuit when the diode is ON

(i) When the diode is ON

As R_f << R, this circuit reduces to
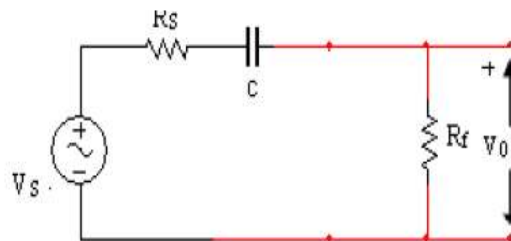
Fig.ii) Circuit when the diode is ON

This circuit, for the purpose of computing the output may be redrawn as fig.iv
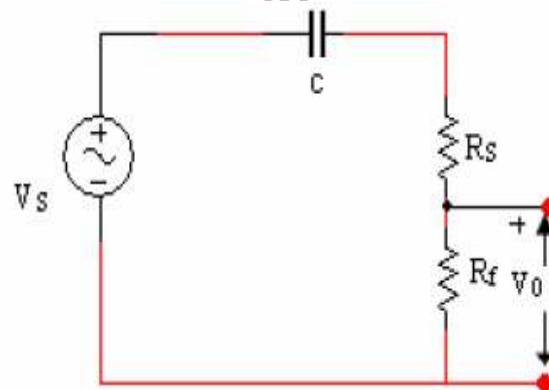
Fig.Circuit to calculate the output when the diode is ON

(ii)   when the diode is OFF

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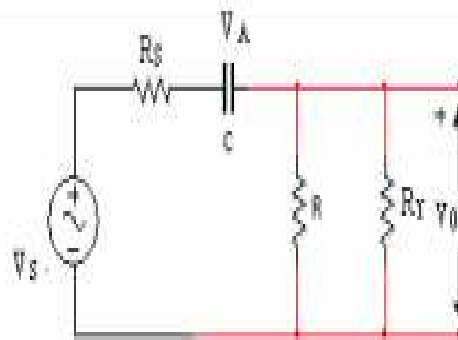
circuit when D is OFF

As Rr >> R, this circuit reduces to
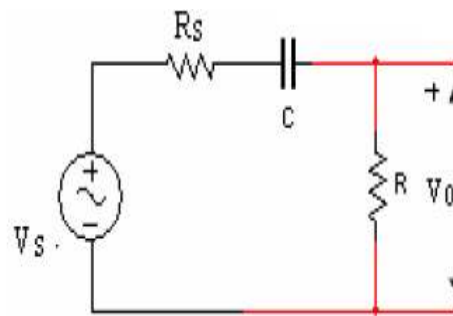
Again, for computing the output this circuit is redrawn as in Fig
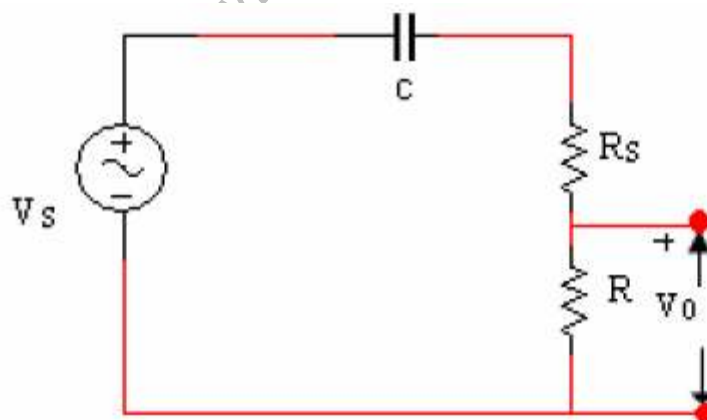
Fig.Circuit to calculate the output when the diode is OFF

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2.9 Practical clamping circuits

If a square wave is applied as input to a clamping circuit, the output reaches the steady state value after a few cycles.

Hence for the input in Fig.(a) the output of the clamping circuit is given in (b).
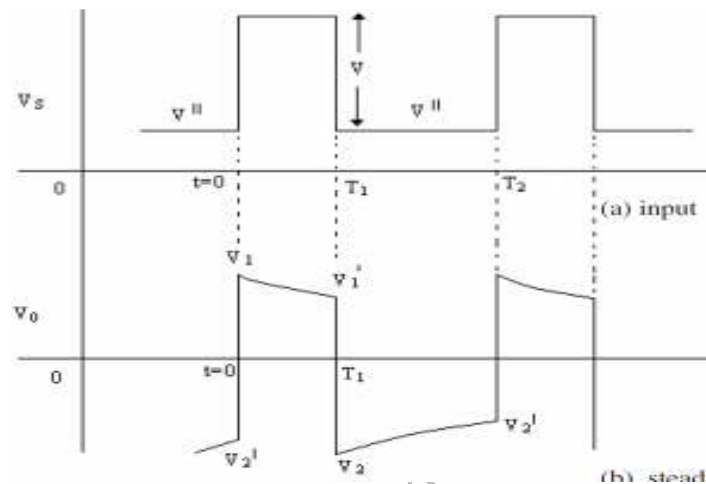
(a) input

(b) steady-state output

Input and steady-state output of the clamping circuit

The output at steady-state is as in figure above with voltage levels V^1, V^{11}, V_2 and
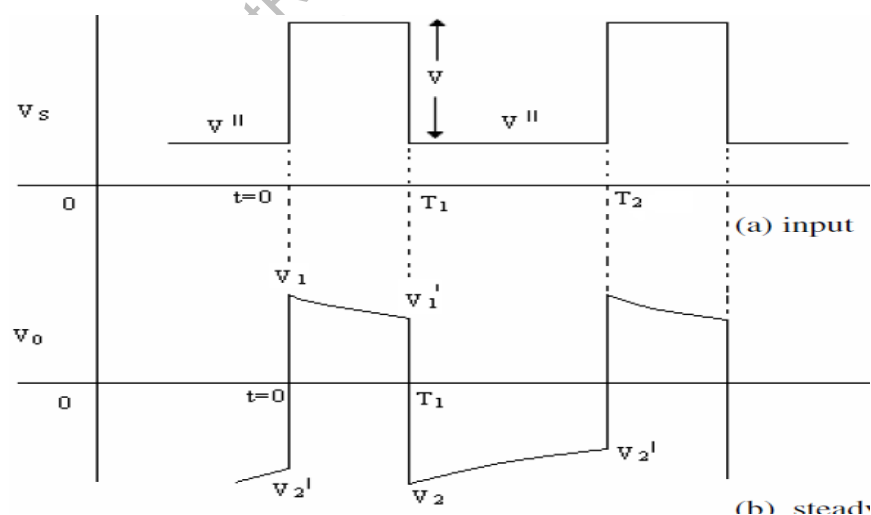
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Input and steady-state output of the clamping circuit

The output at steady-state is as in figure above with voltage levels V_1, V_1^1, V_2 and V_2^1. This output can be plotted to scale if the voltages V_1, V_1^1, V_2 and V_2^1 are calculated. To calculate these four unknowns, we need four equations and these four equations are obtained as follows.fig.

(a) consider the situation at t = 0-

At   t = 0- , $V_s = V^{11}$ and $V_0 = V_2^1$

The diode is reverse biased and the corresponding equivalent circuit is
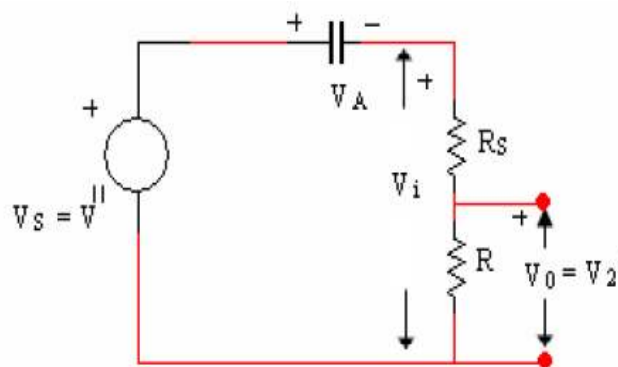
The voltage across the capacitor terminals at t=0- is

$$V_A(0-) = V_s - V_i \qquad \text{--------} \qquad 2$$

$$V_s = V^{11} \quad \text{and} \quad V_2^1 = V_i \frac{R}{R_s + R}$$

$$\therefore V_i = V_2^1 \frac{(R_s + R)}{R}$$

Substituting the values of V_s and V_i in equation 2

$$\therefore V_A(0-) = V^{11} - V_2^1 \frac{(R_s + R)}{R} \qquad \text{--------} \qquad 3$$

(b) Consider the situation at the instant t = 0+

At t= 0+, $V_s = V^1$ and $V_0 = V_1$. the diode is ON and the corresponding equivalent circuit is

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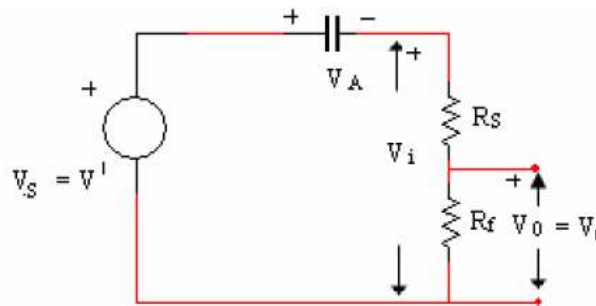
The voltage across the capacitor terminals at t = 0+ is

$$V_A(0+) = V_s - V_i$$
$$= V^1 - V_i$$

$$V_1 = V_i \frac{R_f}{R_s + R_f} ,$$

$$\therefore \quad V_i = \frac{(R_s + R_f)}{R_f} V_1$$

$$\therefore \quad V_A(0+) = V^1 - \frac{(R_s + R_f)}{R_f} V_1 \qquad -------- \qquad 4$$

Since the voltage across the capacitor cannot change instantaneously

$$V_A(0-) = V_A(0+)$$

Hence, from equations 3 and 4

$$V^{11} - \frac{R + R_s}{R} V_2{}^1 = V^1 - V_1 \frac{R_s + R_f}{R_f} \qquad -------- \qquad 5$$

The peak-to-peak amplitude of the input is V. Therefore

$$V = V^1 - V^{11}$$

From equation 5 ,$V = V^1 - V^{11} = V_1 \dfrac{R_s + R_f}{R_f} - \dfrac{R + R_s}{R} V_2{}^1$ -------- 6

Once again consider the situation at $t = T_1{}^-$, $V_s = V^1$ and $V_0 = V_1{}^1$ and the diode is ON

$$V_A(T_1-) = V_s - V_i$$
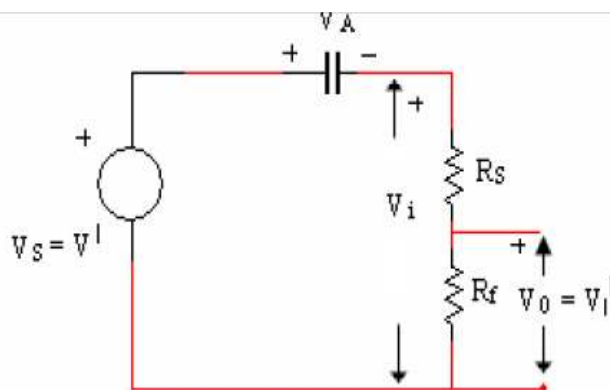
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$$= V^1 - \frac{R_f + R_s}{R_f} V_1^1 \qquad \text{------- } 7$$

Similarly, at $t = T_1+$ from the equivalent circuit, since D is OFF
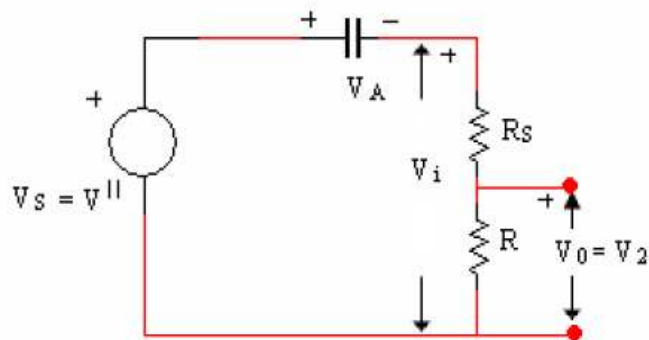
$$\therefore V_A(T_1+) = V_s - V_i$$

$$= V^{11} - \frac{R + R_s}{R} V_2 \qquad \text{------- } 8$$

Again as $V_A(T_1-) = V_A(T_1 +)$, from equations 7 and 8

$$V^1 - \frac{R_f + R_s}{R_f} V_1^1 = V^{11} - \frac{R + R_s}{R} V_2$$

$$V = V^1 - V^{11} = \frac{R_f + R_s}{R_f} V_1^1 - \frac{R + R_s}{R} V_2 \qquad \text{------- } 9$$

Further at $t = 0+$, $V_0 = V_1$ and in the interval 0 to T_1, V_0 decays with a time constant $(R_f+R_s)C$

Hence, $V_1^1 = V_1 e^{\frac{-T_1}{(R_f+R_s)C}}$ $\qquad$ --------- 10

Similarly in the interval T_1 to T_2, the diode is reverse biased and the circuit time constant is $(R_s+R)C$

The voltage V_2 decays to V_2^1

$$V_2^1 = V_2 \, e^{\frac{-(T_2-T_1)}{(R_s+R)C}} \qquad \text{--------- } 11$$

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Equations 6, 9, 10 and 11 will enable us to determine the voltage V_1, V_1^1, V_2 and V_2^1. If in the above circuit $R_s = 0$.

Equations 6 and 9 reduce to

$$V = V_1 - V_2^1 = V_1^1 - V_2 \qquad \text{-------- } 12$$

It is evident from the above discussion that the output is independent of the levels V^1 and V^{11} associated with the input and is only determined by the amplitude V.

Subtracting equation 9 from equation 6

$$\frac{R_f + R_s}{R_f}(V_1 - V_1^1) - \frac{R + R_s}{R}(V_2^1 - V_2) = 0 \qquad \text{------- } 13$$

If $V_1 - V_1^1 = \Delta_f$ and $V_2^1 - V_2 = \Delta_r$

From Equation 13

$$\frac{R_f + R_s}{R_f}\Delta_f = \frac{R + R_s}{R}\Delta_r$$

$$\Delta_f = \frac{R_f}{R_s + R_f} \cdot \frac{R + R_s}{R}\Delta_r$$

If $R_s \ll R$

$$\Delta_f = \frac{R_f}{R_s + R_f}\Delta_r \quad,$$

where Δ_f is the tilt in the forward direction and Δ_r is the tilt in the reverse direction

Let $R_s \ll R_f$

Then $\Delta_f \approx \Delta_r$

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A clamping circuit that clamps the output to a reference voltage V_R:

The following clamping circuit similar to that we have studied earlier, except for the fact that a reference voltage V_R is included.
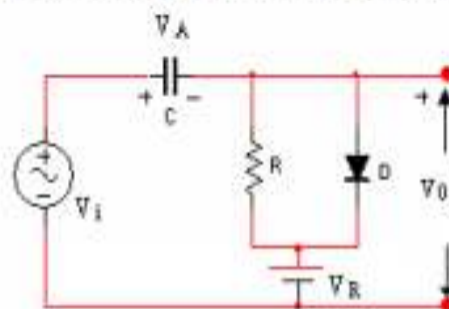
Fig.1 Circuit that clamps the positive peak of the input to V_R

To obtain the steady-state response of the circuit, first assume that V_R is zero. Then this circuit is clamping circuit that clamps the positive peak of the input signal to V_γ. Now the steady-state response for the input of an unsymmetrical square wave, will be as follows.
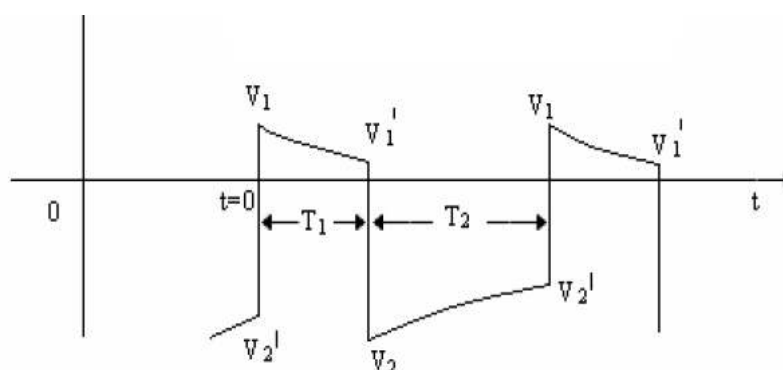
Solving four equations (we have discussed earlier) the values of V_1, V_1^1, V_2 and V_2^1 can be evaluated. To each of these values calculated add V_R. With the result, the positive peak in the output is clamped to V_R.
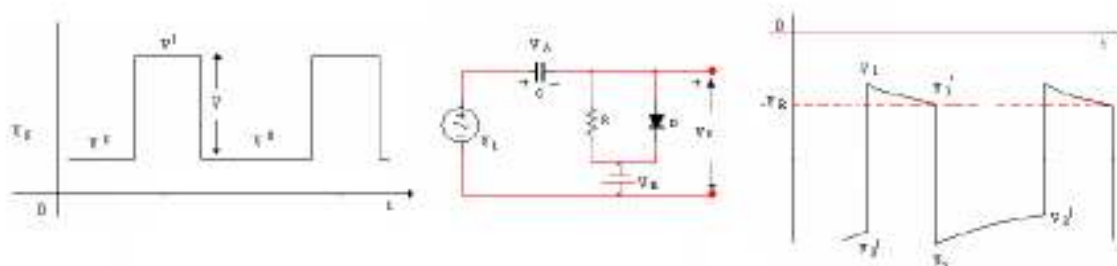
The positive peak of the input clamped to $-V_R$

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2.10 Effect of diode charecterestics on clamping voltage:

The diode characteristics will also effect the voltage as diode voltage is the clamping voltage,

$$I_{cl} = I_o e^{V_{cl}/\eta V_T}$$

will be the diode current. For charging of capacitor resistor voltage is equal to

$$R = V_A - V'' = V - V_{cl}$$
$$V_{cl} << V. \text{ Hence } V - V_{cl} = V$$

Charging current=discharging current

$$I_{cl} = \frac{V}{R} = I_o e^{(V_{cl}/\eta V_T)}$$

$$\frac{V}{I_o R} = e^{(V_{cl}/\eta V_T)}$$

$$V_{cl} = \eta V_T \ln \frac{V}{RI_o}$$

$$dV_{cl} = \eta V_T \frac{dV}{V}$$

From the above equation we can say that the diode will effect the voltage as diode voltage is the clamping voltage,

Important Questions:

1.what is clipping?what are the types of clippers?

2.what is non linear wave shaping?

3.what is clamping ?what are the types of clamping?

4.explain the effect of diode charecterestics on clamping voltage?

5.state clamping circuit theorem?

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3. SWITCHING CHARECTERESTICS OF DEVICES

SYLLABUS:

Transistor and diode as a Switch - Switching times of a transistor. Transistor acts as a switch, Breakdown voltage consideration of transistor, saturation parameters of transistor and their variation with temperature, design of transistor switch, transistor switching times.
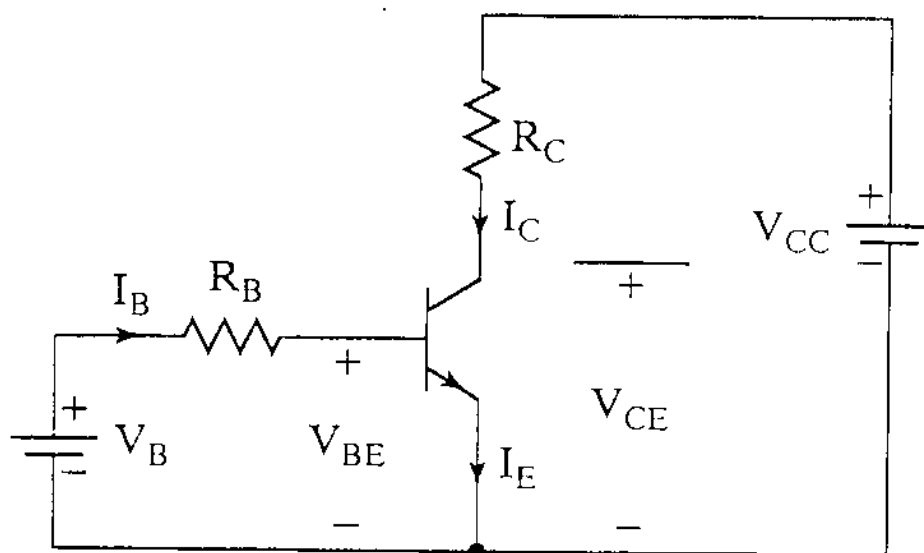
Fig. Transistor as a switch

Above diagram represents the operation of transistor as a switch.

The transistor operates as a switch in two regions mainly

1. Saturation region: In this region transistor acts as closed switch.

2. Cut-off region: In this region transistor acts as closed switch

By applying KCL to above circuit,

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$$I_B = \frac{V_B - V_{BE}}{R_B}$$
$$V_{CE} = V_{CC} - I_C R_C$$
$$V_{CE} = V_{CB} + V_{BE}$$
$$V_{CB} = V_{CE} - V_{BE}$$

3.2 Switching characteristics of devices

Diode as a switch:

A PN junction diode can be used as a switch. When diode is forward biased, the switch is said to be in the ON state and in reverse-bias, the switch is in the OFF state. The V-I Characteristic of a PN junction diode is shown here.

c
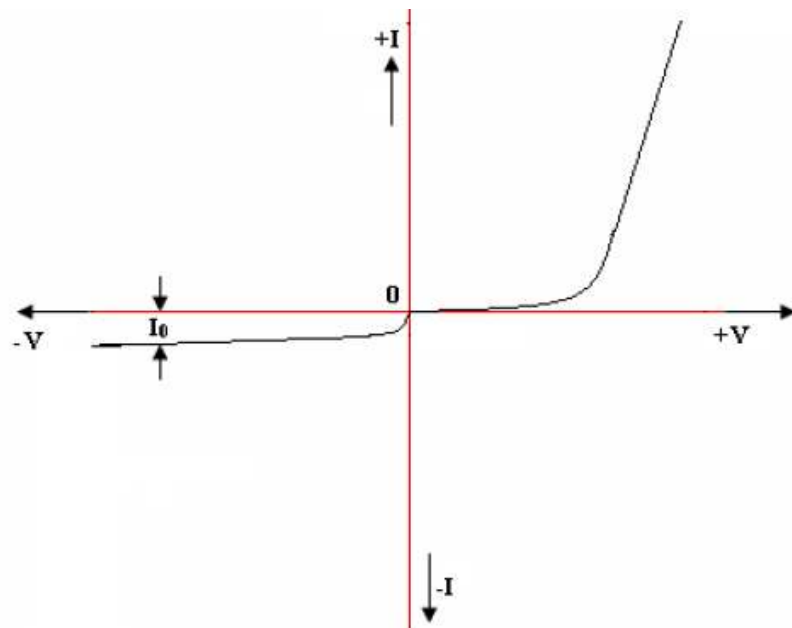
V-I characteristic of a PN diode

The diode current is given by the relation

$$I = I_0 (e^{\frac{V}{\eta V_T}} - 1)$$

Where V is the bias voltage, η= 1 or 2 depending on whether the diode is Ge or Si and VT is the Volt-equivalent for temperature and at room temperature VT = 26mV.

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If $e^{\frac{V}{\eta V_T}} \gg 1,$

equation 5.1 reduces to

$$I = I_0 \, e^{\frac{V}{\eta V_T}}$$

When the diode is forward biased V is positive and I is a positive current which varies exponentially with the variation of V. When the diode is reverse-biased V is a negative voltage and the current I now flows in the opposite direction. I = -I0, the reverse saturation current gets doubled for every 100C rise in temperature.

When a diode is used as a switch, the device should be ON or OFF depending on the polarity of the signal applied to change state.

Junction diode switching times:

Reverse recovery time of the diode:

Let the diode be ON for some time, as a result there is a large current due to injected hole or electron density.
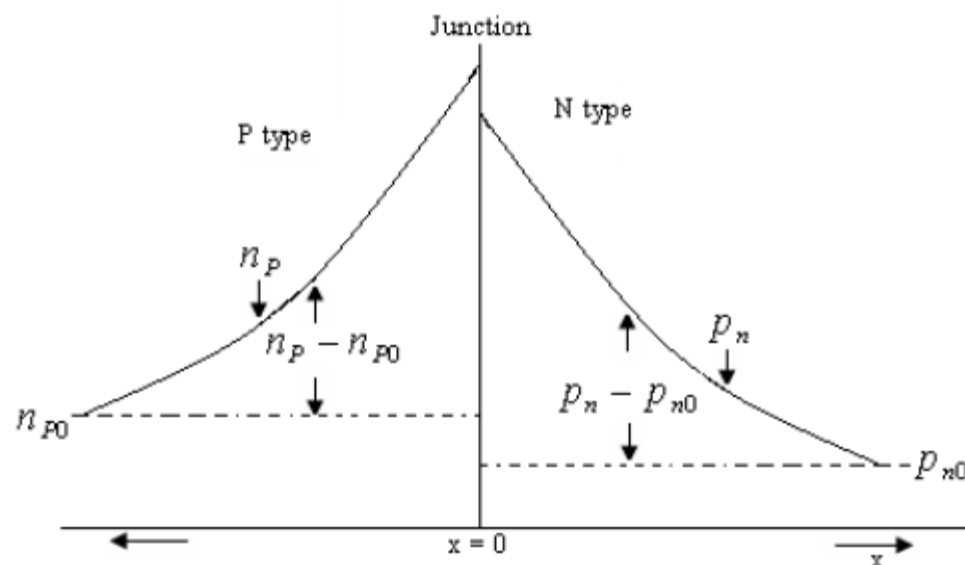
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Fig.a Minority carrier density distribution as a function of x, the distance from the junction when the diode is ON

p_{n0} = density of holes on the n-side at equilibrium

n_{P0} = density of electrons on the P-side at equilibrium

n_P = density of electrons on the P-side when forward biased

p_n = density of holes on the n-side when forward biased

$p_n - p_{n0}$ = injected or excess hole density on the n-side

$n_P - n_{P0}$ = injected or excess electron density on the P-side
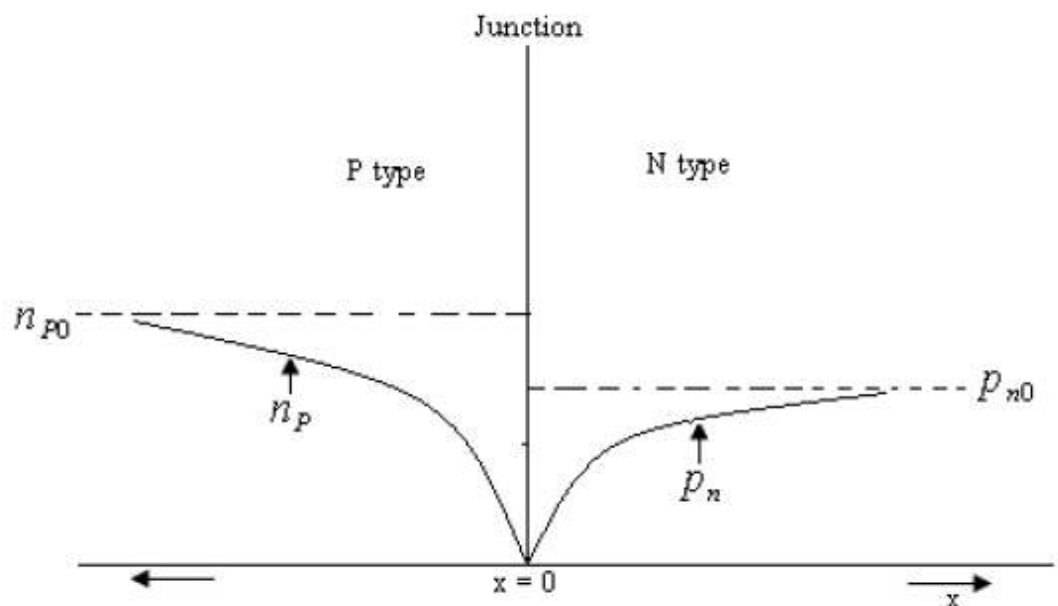
Fig.b Minority carrier density distribution as a function of x, the distance from the junction when the diode is OFF

When the diode is ON the number of minority carriers is large fig (a). When the polarity of the external voltage is suddenly reversed, the diode forward current when ON being large is to be reduced to reverse current which is very small. But this is not happened as it takes a finite time delay for the minority carrier density distribution to take the form shown in fig. During this period the injected minority carrier density will drop to zero and the minority carrier density reaches the equilibrium value.

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(b) Voltage applied to diode

(c) injected carrier density at the junction

(d) diode current

storage time t_s

Transition time t_t
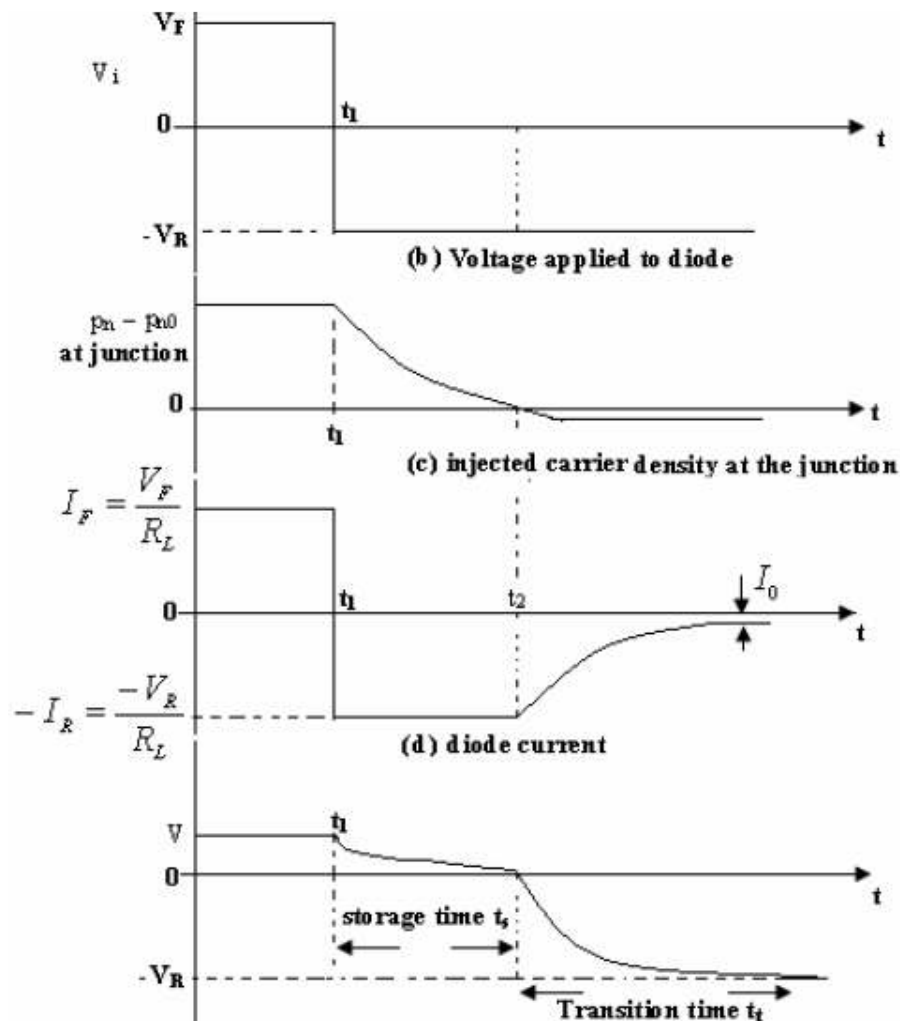
As long as the voltage Vi = VF till t1, the diode is ON. The forward resistance of the diode being negligible when compared to RL, therefore

$$I_F = \frac{V_F}{R_L}.$$

At t = t1, the polarity of Vi is abruptly reversed, i.e.Vi = -VR and $-I_R = \frac{-V_R}{R_L}$ until t = t2 at which time minority carrier density pn at x = 0 has reached the equilibrium value pn0.

At t = t2 the charge carriers have been swept, the polarity of the diode voltage reverses, the diode current starts to decrease. The time duration, t1 to t2, during which period the stored minority charge becomes zero is called the **storage time ts**.

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The time interval from t2 to the instant that the diode has recovered (V = -VR) is called the **transition time,t_T**.

The sum total of the storage time,ts and the transition time,tt is called the reverse recovery time of the diode, trr.

$$\therefore \ t_{rr} = t_s + t_t$$

Transistor switching times

Let the input to the transistor switch be a pulse of duration T.

When a pulse is applied, because of stray capacitances, collector current will not reach the steady state value instantaneously. To know exactly when the device switches into the ON state and also into the OFF state we define the following switching times of the transistor.
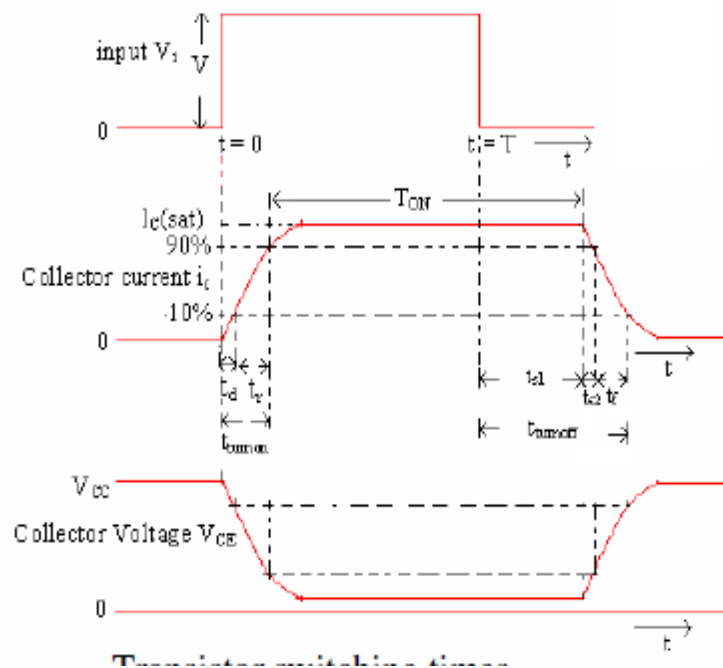
Fig. **Transistor switching times**

Delay Time, td: It is the time taken for the collector current to reach from its initial value to 10% of its final value, If the rise of the collector current is linear, the time required to rise to 10%IC(sat) is 1/8 the time required for the current to rise from 10% to 90% IC(sat).

It is given as

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$$t_d = \frac{1}{8}t_r$$

where tr is the rise time

Rise Time,tr : It is the time taken for the collector current to reach from 10% of its final value to 90% of its final value.

However, because of the stored charges, the current remains unaltered for sometime interval ts1 and then begin to fall. The time taken for this current to fall from its initial value at ts1 to 90% of its initial value is ts2. The sum of these ts1 and ts2 is approximately ts1 and is called the storage time.

Storage time, ts: It is the time taken for the collector current to fall from its initial value to 90% of its initial value. Storage time

$$: t_s \cong \tau_s \ln \frac{I_{B1} - I_{B2}}{I_{B\min} - I_{B2}}$$

I_{B1} is the base current when the pulse amplitude is V(=12 V) and I_{B2} is the base current when the pulse amplitude is zero.

Fall time, t_f : It is the time taken for the collector current to fall from 90% of its initial value to 10% of its initial value.

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Let initially Q1 be OFF and Q2 be in ON. Then the voltage at the first collector is V_{CC} and the voltage at the second collector is V_{CE}(sat) . If a negative trigger is applied at the base of the ON device (Q2), Q2 goes into the OFF i.e. its collector voltage rises to V_{CC} .Consequently Q1 goes into the ON state and its collector voltage falls to VCE(sat).

Design of a fixed bias binary:

Design a fixed bias binary with supply voltages +12V, NPN silicon devices having VCE(sat)= 0.2V , VBE(sat)= 0.7V and h_{FEmin}=50 are used.

Assume I_C = 5mA.

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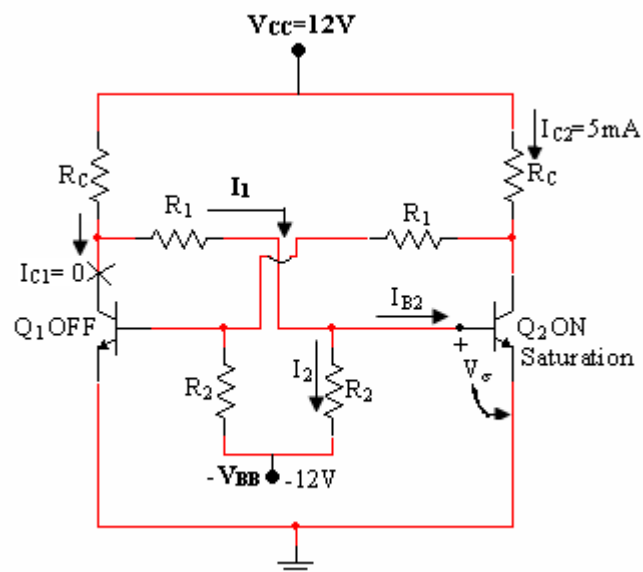
$$R_c = \left| \frac{V_{CC} - V_{CE(sat)}}{I_{C2}} \right| = \frac{12 - 0.2V}{5mA} = \frac{11.8V}{5mA}$$

$$= 2.36 K\Omega$$
$$\approx 2.2K \text{ (standard resistance)}$$

$$R_2 = \frac{V_\sigma - (-V_{BB})}{I_2}$$

$$Choose \quad I_2 \approx \frac{1}{10} I_{C2}$$

$$= 0.5mA$$

$$\therefore R_2 = \frac{0.7 + 12}{0.5} = \frac{12.7V}{0.5mA} = 25.4 K\Omega$$

$$\approx 22 K\Omega$$

If Q2 is in saturation

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$$I_{B2} = 1.5 I_{B2\,min}$$
$$= 0.15\,mA$$

$$I_1 = I_2 + I_{B2}$$
$$= 0.5\,mA + 0.15\,mA = 0.65\,mA$$

$$R_C + R_1 = \frac{V_{CC} - V_\sigma}{I_1} = \frac{12 - 0.7}{0.65\,mA} = \frac{11.3V}{0.65\,mA} = 17.38\,K\Omega$$

$$R_1 = (R_C + R_1) - R_C$$
$$= 17.38 - 2.36 = 15.02\,K\Omega$$

The circuit, so designed, with component values indicated is shown below:
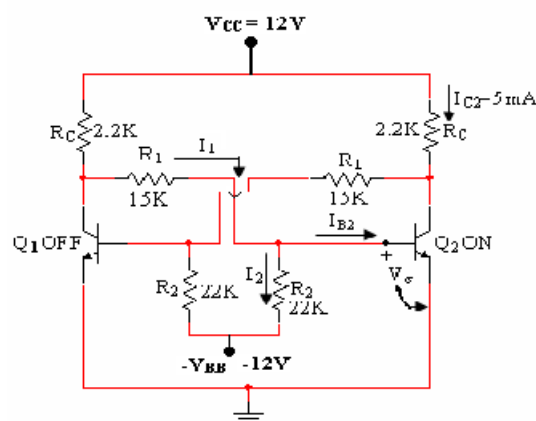
$$= 0.94 mA$$
$$I_{B2} = I_1 - I_2$$
$$= 0.94 mA - 0.58 mA$$
$$= 0.36 mA$$
$$I_{B2} \geq I_{B2\,min}$$
Hence Q_2 is in saturation

$$V_{B1} = V_{CE}(sat)\frac{R_2}{R_1 + R_2} - V_{BB}\frac{R_1}{R_1 + R_2}$$
$$= 0.2 \times \frac{22}{10 + 22} - 12 \times \frac{10}{10 + 22}$$
$$= 0.137 - 3.75$$
$$= -3.613V$$
Hence Q_1 is OFF

3.4 Resolution time of a binary:

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It is the sum of settling time and transition time of a   binary is called resolution time.

3.5 Methods of improving resolution time:

1. By reducing stray capacitances.

2. By not allowing transistors to go into saturation.

3.6 Methods of triggering a binary:

To change the binary from one stable state to the other, a pulse of short duration with sufficient amplitude (called trigger) of proper polarity should be applied at the input(output) of an active device the circuit. The trigger can be a dc trigger or it can be a pulse trigger. There are two triggering methods to change the state of multivibrator.

1. Unsymmetrical triggering

2. Symmetrical triggering.

Unsymmetrical triggering:

In unsymmetrical triggering, one trigger pulse, taken from a source, is applied at

one point in the circuit. The next trigger pulse taken from a different source is applied at

a different point in the circuit as shown below.
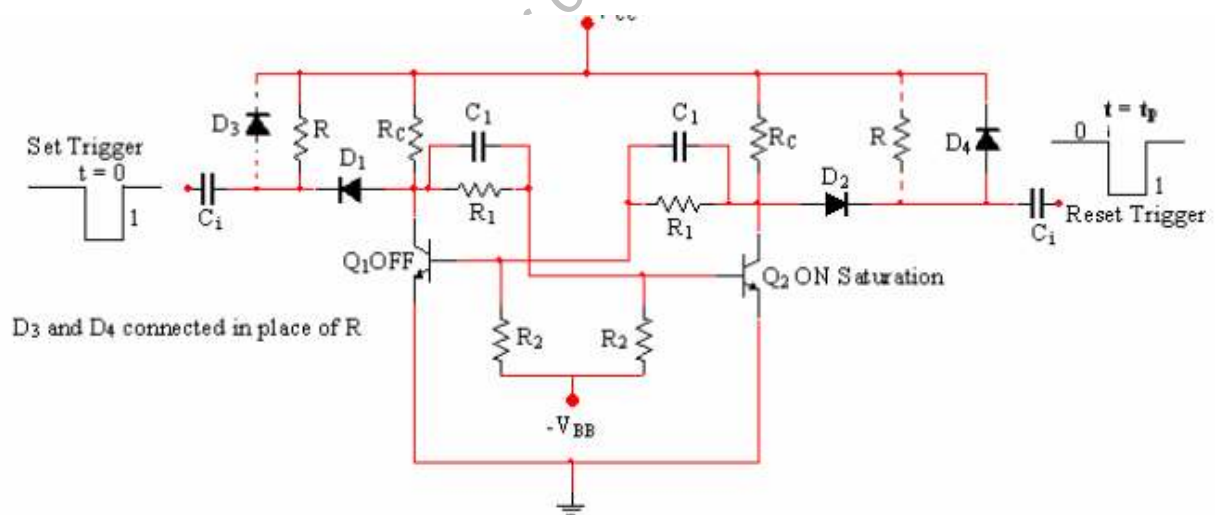
Unsymmetrical triggering of a binary

Let the trigger be applied to the collector C1 of the circuit at t=0. If Q1 is OFF, D1 is ON and this negative pulse appears at the base of Q2 as the first collector and second base are connected. Q2 goes into the OFF state and Q1 into the ON state. The next through C1 trigger pulse, i.e. the Reset pulse, is applied through D2 at the second collector C2 which is coupled

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to the first base through C1. Q1 now goes into the OFF state and Q2 into the ON state. Unsymmetrical triggering is used to generate a gated output, the width of this gate must be at least equal to the spacing between two successive triggers. To prevent the loading down problem from the trigger source , R should be large. But when a trigger is applied, a charge is built up on the condenser Ci. If the charge is to be quickly removed before the application of the next trigger signal at this terminal, R should be small. So while choosing the value of resistance R a compromise is necessary single resistance cannot simultaneously satisfy these two requirements. Hence in place of R, diodes D3 and D4 are used. When a pulse appears, the diode is OFF (D3 or D4), a large reverse resistance of the diode appears in place of R. Otherwise the diode is ON offering negligible resistance so that the charge on the capacitance can be quickly removed.

Symmetrical triggering:

In symmetrical triggering, one triggering pulse generator is taken to change from one stable state to the other in one direction. The same is used to change the state in reverse direction also. This method of triggering is normally used in counters.
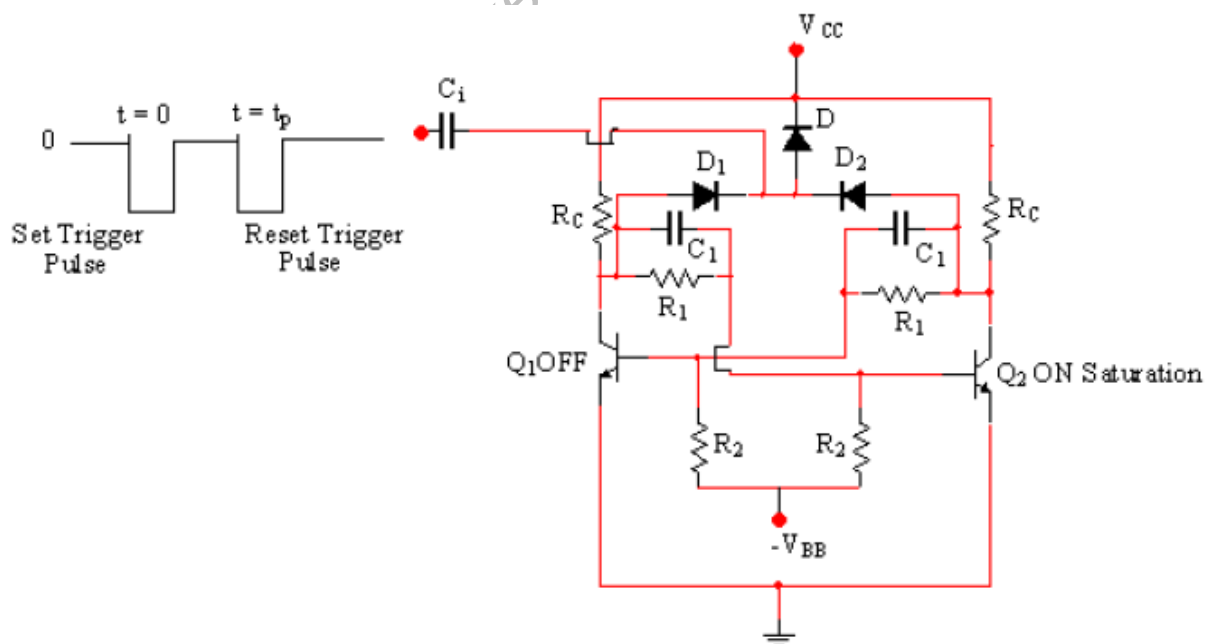
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Fig. Symmetric triggering of binary

The purpose of D is similar to the diodes D3 and D4 used earlier. The first trigger pulse makes D1 conduct and this pulse is coupled to the base of Q2 and drives Q2 into the OFF state and Q1 into the ON state. The next trigger pulse applied at t = t_p is coupled to the base of Q1 as D2 is now ON. Hence Q1 again goes into the OFF state and Q2 into the ON state. D1 and D2 are called steering diodes as these diodes steer the trigger pulse train.

Self-bias binary :

In a fixed bias binary there are two separate sources, VCC and VBB. Instead two we can design a binary with one power supply using self-bias method.
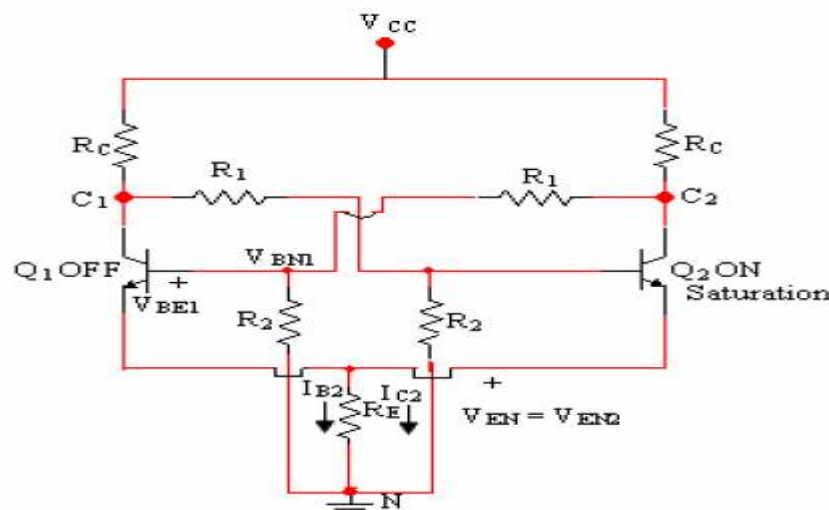
Self-bias Binary

Let Q_2 be ON and in saturation, in the initial stable state. As a result I_{B2} and I_{C2} flow through R_E developing a voltage V_{EN}. The voltage between the base emitter terminals of Q1 is V_{BE1} and it is $V_{BE1} = V_{BN1} - V_{EN}$

If this voltage reverse biases the emitter diode of Q1, then Q1 is indeed in the OFF state.To calculate the stable state currents and voltages consider a practical circuit.

In npn silicon transistors are used. $V_{BE(sat)} = 0.7V$, $V_{CE(sat)} = 0.4V$ and $h_{FEmin} = 50$,

$V_{CC} = 20V$, $R_C = 6.7K$, R1 = 30K and R2 = 15K, $R_E = 400\Omega$

Let Q1 be OFF and Q2 be ON. As Q1 is OFF, $I_{E1} = 0$. To verify whether Q2 is in Saturation or not , draw the collector loop and base loop of the circuit by thevenising at the collector and base terminals.

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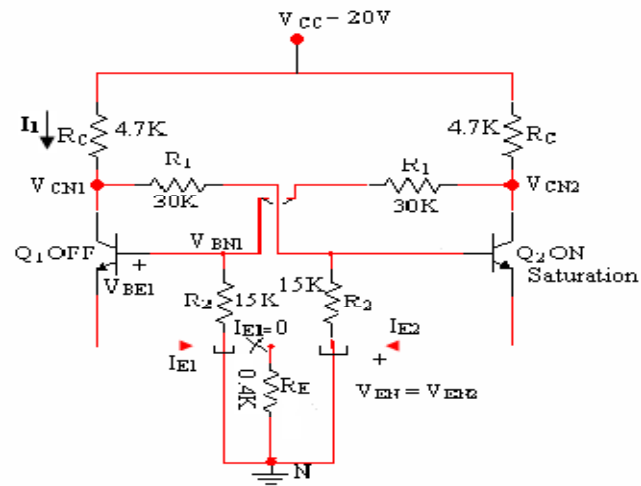
$$V_{thb} = V_{CC} \times \frac{R_2}{R_C + R_1 + R_2}$$

$$= 20 \times \frac{15}{4.7 + 30 + 15}$$

$$= 6.03V$$

and

$$R_{thb} = R_2 // (R_C + R_1) = \frac{R_2 (R_C + R_1)}{R_2 + R_C + R_1}$$

$$= \frac{(15)(30 + 4.7)}{4.7 + 30 + 15}$$

$$= 10.47K$$

$$V_{thc} = V_{CC} \times \frac{(R_1 + R_2)}{R_C + R_1 + R_2}$$

$$= \frac{20 \times (30 + 15)}{4.7 + 30 + 15}$$

$$= 18.10V$$

$$R_{thc} = (R_1 + R_2) // R_C$$

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$$= \frac{(30+15)(4.7)}{30+15+4.7}$$
$$= 4.25K$$
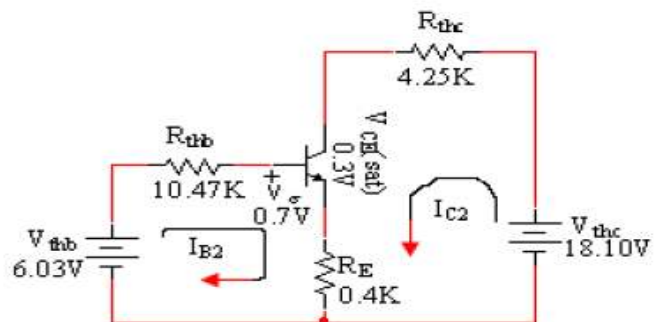
Using KVL at the input and output loops

$6.03-0.7 = (10.47+0.4) I_{B2} + 0.4 I_{C2}$ ---------- (1)
$18.10-0.3 = 0.4 I_{B2} + (6.25+0.4) I_{C2}$ ---------- (2)
i.e.
$5.33V = 10.87 I_{B2} + 0.4 I_{C2}$

$17.80V = 0.4 I_{B2} + 6.65 I_{C2}$
From which

$I_{B2} = 0.35mA$
$I_{C2} = 3.79mA$

$$I_{B2min} = \frac{I_{C2}}{h_{FE}} = \frac{3.79mA}{50}$$
$$= 0.076mA$$

$I_{B2} \gg I_{B2min}$
Hence Q_2 is saturation
$$\therefore V_{EN} = V_{EN2} = (I_{B2} + I_{C2})R_E$$
$$V_{CN2} = V_{EN2} + V_{CE(sat)}$$
$$= (1.66V + 0.4V) = 2.06V$$
$$V_{BN2} = V_{EN2} + V_\sigma$$
$$= (1.66V + 0.7V) = 2.36V$$
$$V_{BN1} = V_{CN2} \times \frac{R_2}{R_1 + R_2}$$
$$= \frac{2.06 \times 15}{15 + 30}$$
$$= 0.69V$$
$$V_{BE1} = V_{BN1} - V_{EN2}$$
$$= (0.69V - 1.66) = -0.97V$$
As this voltage reverse biases the emitter diode, Q_1 is OFF.

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$$I_1 = \frac{V_{CC} - V_{BN2}}{R_C + R_1}$$

$$= \frac{20 - 2.36}{4.7 + 30}$$

$$= 0.51mA$$

$$V_{CN1} = V_{CC} - I_1 R_C$$

$$= 20 - (0.51)(4.7)$$

$$= 17.6V$$

The stable state voltages are

$V_{CN1}=17.6V$,	$V_{BN1}=0.69V$
$V_{CN2}=2.06V$	$V_{BN2}=2.36V$
$V_{EN}=1.66V$	

3.7 Schmitt trigger:

It is an emitter coupled binary it is also called inventor.The following circuit represents Schmitt trigger.
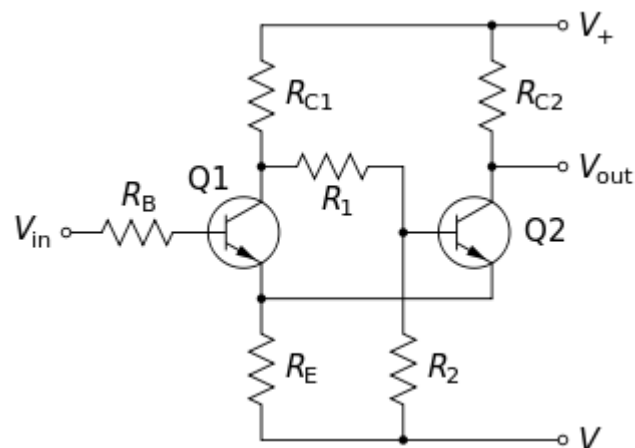
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Fig 1 .schmitt trigger

Schmitt trigger belongs to a class of bistable multivibrator circuits. In a bistable, there exist two D.C. couplings from each output to input of the other. But in Schmitt trigger circuit, there exists only one coupling. It can be recalled that if in the emitter coupled bistable the feedback network from the collector of transistor Q_2 to the base of transistor Q_1 is removed, it becomes a Schmitt trigger circuit.

The Schmitt trigger is used for wave shaping circuits. It can be used for generation of a square wave from a sine wave input. Basically, the circuit has two opposite operating states like in all other multivibrator circuits. However, the trigger signal is not, typically, a pulse waveform but a slowly varying A.C. Voltage. The Schmitt trigger is level sensitive and switches the output state at two distinct trigger levels. One of the triggering levels is called a lower trigger level (abbreviated as L.T.L) and the other as upper trigger level (abbreviated as U.T.L).

Above Figure1 shows the circuit of a Schmitt trigger, the circuit of Schmitt trigger contains of two identical transistors Q_1 and Q_2 coupled through an emitter R_E. The resistors R_1 and R_2 form a voltage divider across the V_{CC} supply and ground. These resistors provide a small forward bias on the base of transistor Q_2.

Let us suppose that initially there is no signal at the input. Then as soon as the power supply V_{CC} is switched on, the transistor Q_2 starts conducting. The flow of its current through resistor R_E produces a voltage drop across it. This voltage drop acts as a reverse bias across the emitter junction of transistor Q_1 due to which it cuts-off. As a result of this, the voltage at its collector rises to V_{CC}. This rising voltage is coupled to the base of transistor Q_2 through the resistor R_1. It increases the forward bias at the base of transistor Q_2 and therefore drives it into saturation and holds it there. At this instant, the collector voltage, level are $V_{C1} = V_{CC}$ and $V_{C2} = V_{CE(sat)}$ as shown in Figure 2.

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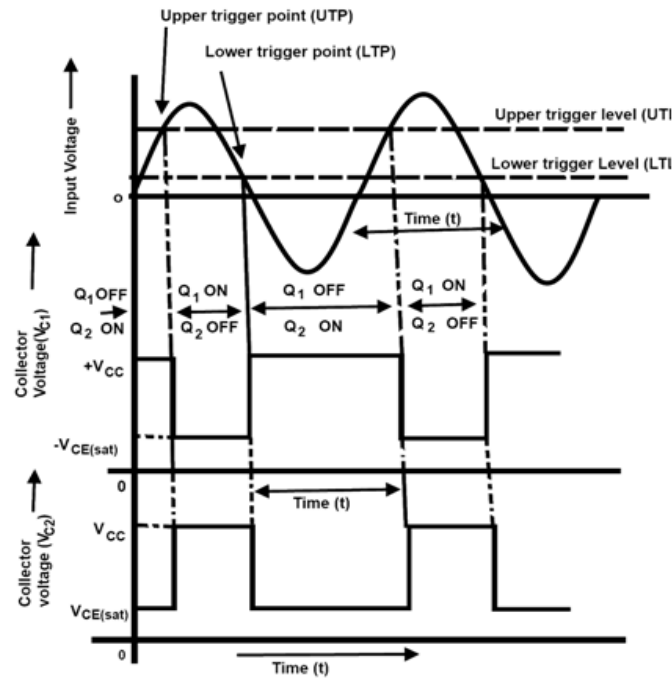
Figure 2: Waveforms at the input and collector of transistor Q1 and Q2

suppose an A.C. signal is applied at the input of the Schmitt trigger (i.e. at the base of the transistor Q_1). As the input voltage increases above zero, nothing will happen till it crosses the upper trigger level (U.L.T). As the input voltage increases, above the upper trigger level, the transistor Q_1 conducts. The point, at which it starts conducting, is known as upper trigger point (U.T.P). As the transistor Q_1 conducts, its collector voltage falls below V_{CC}. This fall is coupled through resistor R_1 to the base of transistor Q_2 which reduces its forward bias. This in turn reduces the current of transistor Q_2 and hence the voltage drop across the resistor R_E. As a result of this, the reverse bias of transistor Q_1 is reduced and it conducts more. As the transistor Q_1 conducts more heavily, its collector further reduces due to which the transistor Q_1 conducts near cut-off. This process continues till the transistor Q_1 is driven into saturation and Q_2 into cut-off. At this instant, the collector voltage levels are $V_{C1} = V_{CE(sat)}$ and $V_{C2} = V_{CC}$ as shown in the figure.

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The transistor Q_1 will continue to conduct till the input voltage falls below the lower trigger level (L.T.L). It will be interesting to know that when the input voltage becomes equal to the lower trigger level, the emitter base junction of transistor Q_1 becomes reverse biased. As a result of this, its collector voltage starts rising toward V_{CC}. This rising voltage increases the forward bias across transistor Q_2 due to which it conducts. The point, at which transistor Q_2 starts conducting, is called lower trigger point (L.T.P). Soon the transistor Q_2 is driven into saturation and Q_1 to cur-off. This completes one cycle. The collector voltage levels at this instant are $V_{C1} = V_{CC}$ and $V_{C2} = V_{CE(sat)}$. No change in state will occur during the negative half cycle of the input voltage.

3.8 Monostable Multivibrator

Introduction:

This circuit consists of two active devices Q1 and Q2, one is in the OFF state, say (Q1) and the other, Q2 in the ON state. These devices remain in the same state forever. Only on the application of a trigger, the multi goes into the quasi stable state (Q1 ON and Q2 OFF) and after a time interval T, will return to the stable state (Q1 OFF and Q2 ON). Thus this circuit generates a gate pulse of duration Tether output of this circuit is high for a time duration T called the pulse duration, pulse width or gate width.

Collector-Coupled monostable multivibrator:

The collector coupled monostable multivibratoris shown below.

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Fig. Collector-coupled monostable multivibrator.

In the stable state Q1 is OFF and Q2 is ON . Therefore

$V_{C1} = V_{CC}$

$V_{C2} = V_{CE(sat)}$

$V_{B2} = V_{BE(sat)} = V_{\sigma}$

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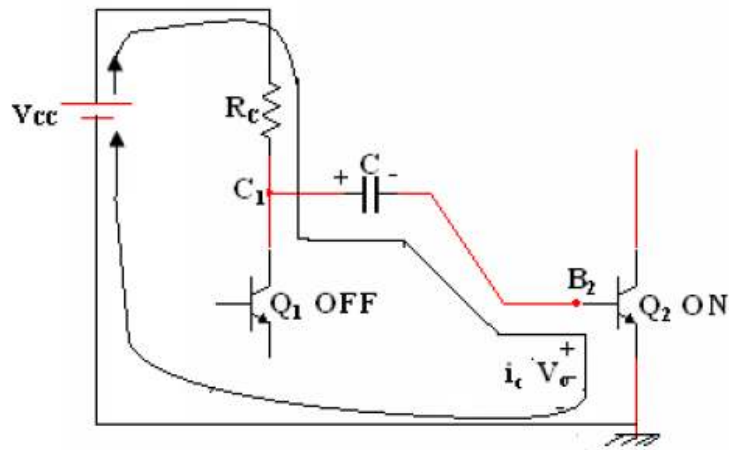
Fig. Charging of C

C now tries to charge to V_{CC} through R_C of Q1 and small input resistance of Q2.As t $\rightarrow\infty$, this voltage reaches V_{CC}. On the application of a trigger at t=0, (a negative pulse at B2), Q2 goes into the OFF state and Q1 is driven into the ON state and preferably into saturation. Hence there is a current I_1 in Q1. V_{C1} is $V_{CE(sat)}$, if $I_1 = I_{C(sat)}$.
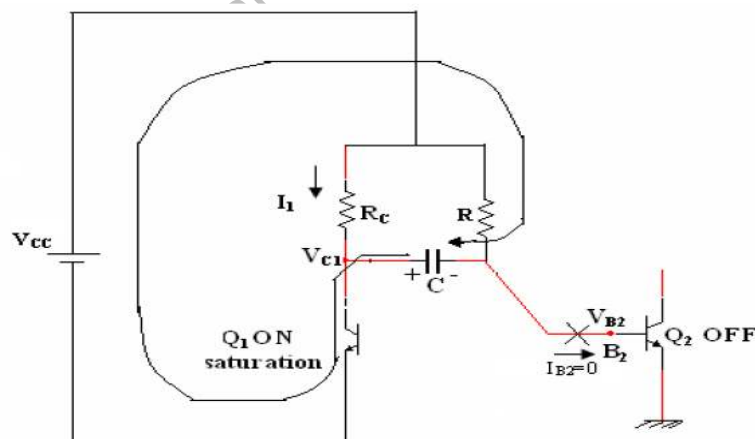
Fig. discharging of c

Pulse & Digital Circuits
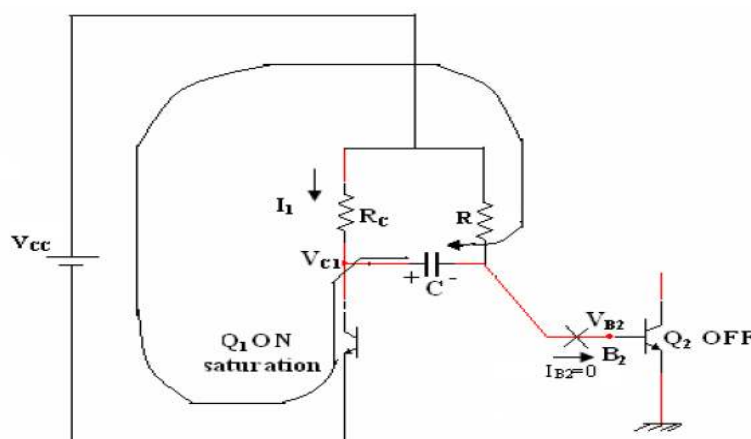
The charge on C now discharges with a time constant $\tau = RC$. As a result the voltage at B_2 changes as a function of time. When this voltage V_{B2} at B_2 reaches V_γ after a time interval T, Q2 is switched ON and Q1 is switched OFF due to regeneration, thus ending the quasi stable state.

The voltage variation at B_2 of Q2
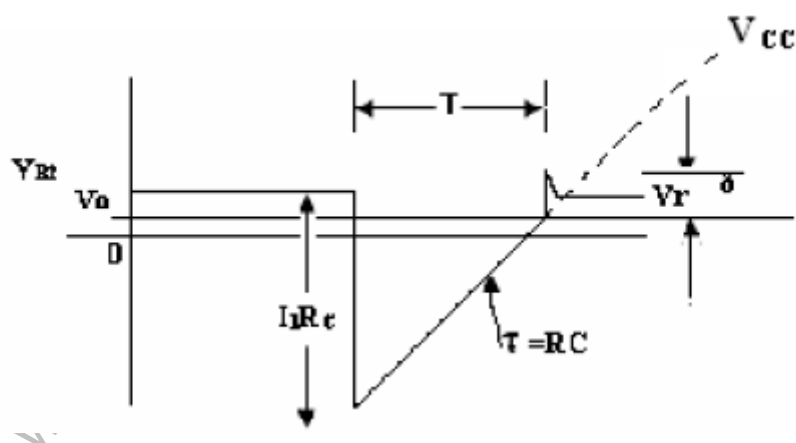
Fig. Voltage variation at the base of Q2 in the quasi stable state.

The time period T can be calculated as T= 0.69RC, if Q1 in the quasi stable state is in saturation, since $I_1RC = V_{CC} - V_{CE(sat)}$

Gate width of a collector coupled mono stable:

A mono stable multi can be used as a voltage to time converter as shown in Fig

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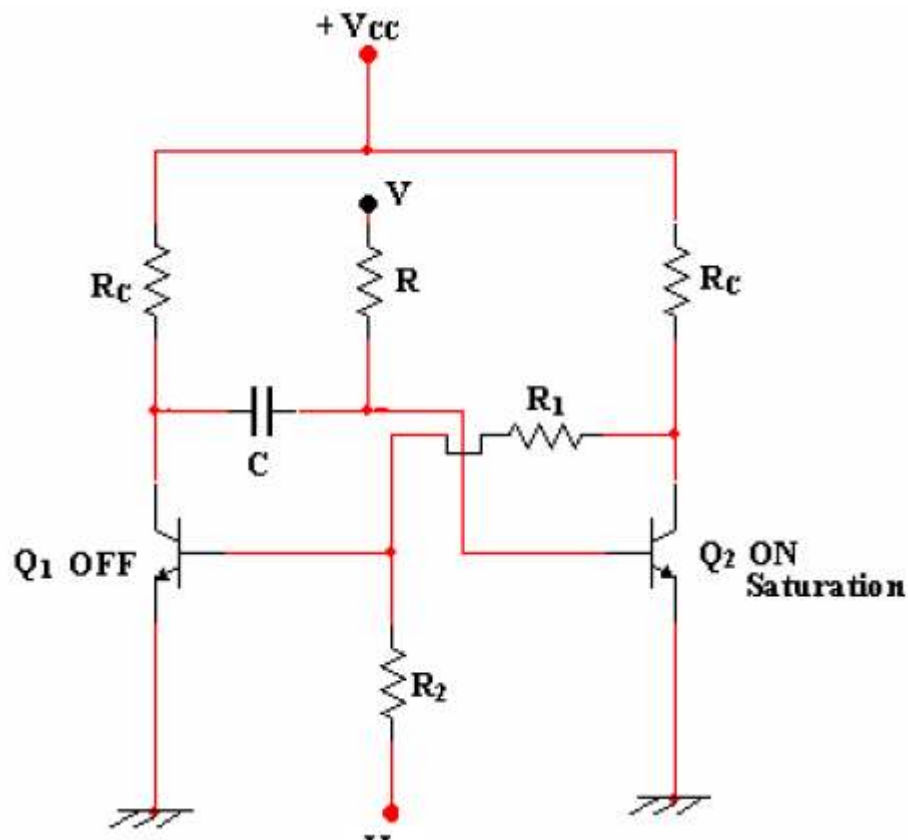
Fig. . Monostable as a voltage to time converter

The time T for which Q1, in the quasi stable state, is ON and Q2 is OFF is calculated.

Consider the voltage variations at B2, fig.7.17

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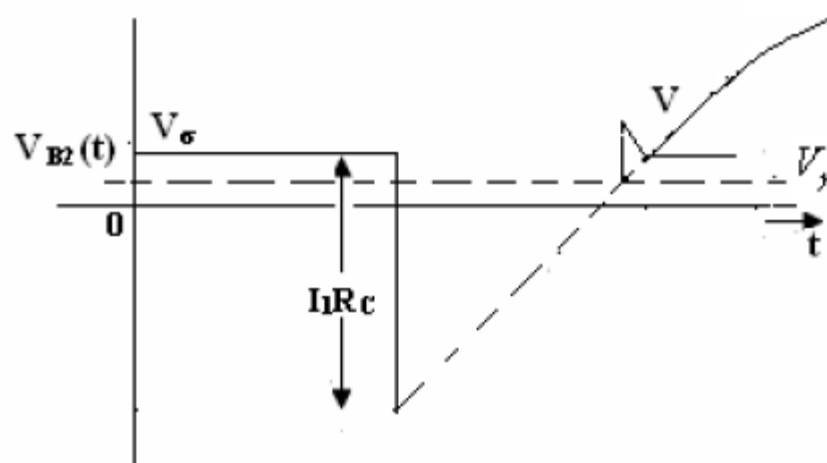
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$$V_{B2}(t) = V_f - (V_f - V_i)e^{\frac{-t}{\tau}}$$

$V_f = V$

$V_i = V_\sigma - I_1 R_C$

If Q_1 is in saturation

$I_1 R_C = V_{CC} - V_{CE}(sat)$

$V_i = V_\sigma - V_{CC} + V_{CE}(sat)$

$$V_{B2}(t) = V - (V - V_\sigma + V_{CC} - V_{CE}(sat))e^{\frac{-t}{\tau}}$$

At $t = T$

$V_{B2}(t) = V_\gamma$

$$V_\gamma = V - (V - V_\sigma + V_{CC} - V_{CE}(sat)e^{\frac{-T}{\tau}}$$

As V_γ, V_σ and $V_{CE}(sat)$ are small when compared to V and V_{CC}

$$\therefore \quad 0 = V - (V + V_{CC})e^{-\frac{T}{\tau}}$$

$$T = \tau \ln \frac{(V + V_{CC})}{V}$$

$$T = \tau \ln(1 + \frac{V_{CC}}{V})$$

Thus, to change T, V can be varied.

3.9 Astable multivibrator

Introduction:

Two cross-coupled switching circuits are connected in this arrangement. The devices in this Multivibrator will not remain in one state (either ON or OFF) forever. Change of state in the devices occurs continuously after a finite time interval depending on the circuit components used. Hence this circuit has two quasi stable states.

Let Q1 and Q2 be two transistors used. If Q1 is ON, then Q2 is OFF. These will remain in this state only for a fixed time duration after which Q1 switches into the OFF state and Q2 into the ON state without applying triggering pulse and this process is repeated. Therefore it

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is also called Free running multivibrator. The output of the circuit is a squarewave, having two time periods, T1 and T2. If T1 = T2=T/2 , then the circuit is a symmetric astable multivibrator. If T1≠T2, then it is called an unsymmetrical astable multi-vibrator. The astable multivibrator is essentially a square wave generator

.

Collector Coupled astable multi:

Collector coupled astable multi is shown below.
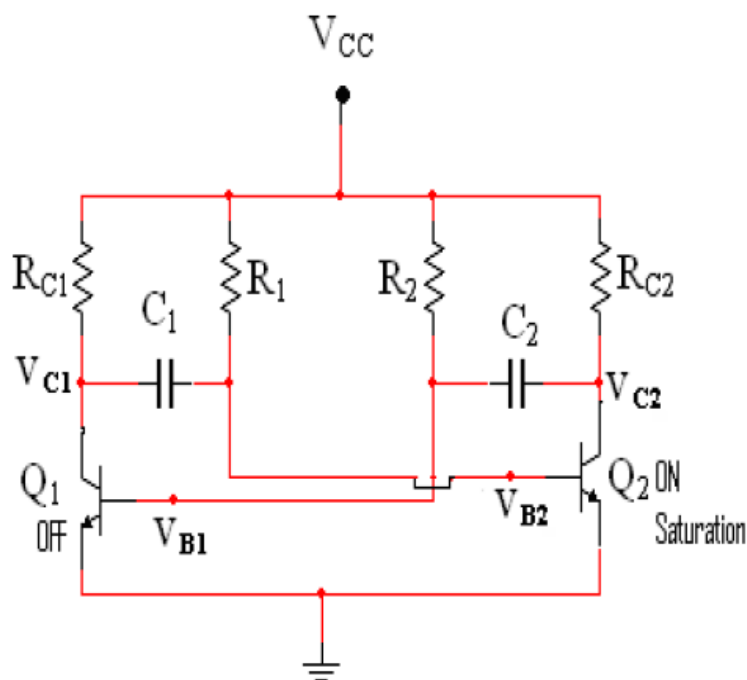
Fig.   astable multi vibrator

Assume that transistor Q1 is OFF and Q2 is ON initially. Then $V_{B2} = V_\sigma$, $V_{C2} = V_{CE(sat)}$ and $V_{C1}=V_{CC}$. With Q1 OFF and Q2 ON, C1 will try to charge to the supply voltage through the collector resistance R_{C1} and through the base and emitter terminals of Q2 .

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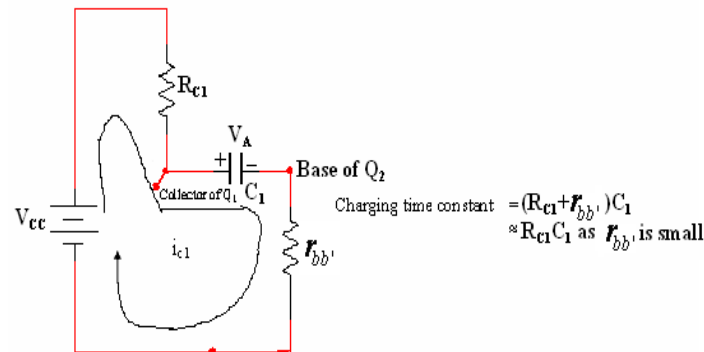
Fig. Charging of capacitor C1

Prior to this condition, Q2 must have been in the OFF state and Q1 must have been in the ON state. As a result C2 must have been charged through R_{C2} . Between the base and emitter terminals of Q1,
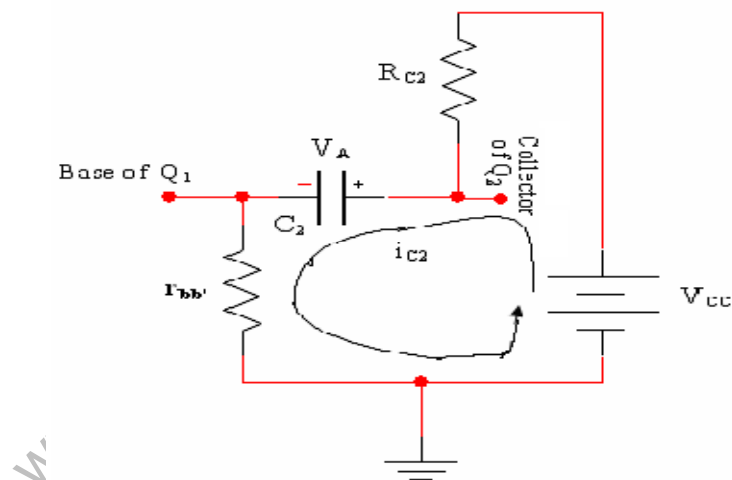
Fig.charging of capacitor C2

When Q2 suddenly changes from the OFF state to ON state, the voltage between its collector and emitter terminals is V_{CE}. Hence the collector of Q2 is at ground potential i.e. the positive end of the capacitor C2 is at the ground potential and its negative terminal is connected to base of Q1. As a large negative voltage is now coupled to base ofQ1, Q1 is indeed in the OFF state.

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But Q1 is not going to remain in the OFF state forever. Now, with Q2 ON, the charge on the capacitor C2 discharges with a time constant $\tau_2 = R2C2$.
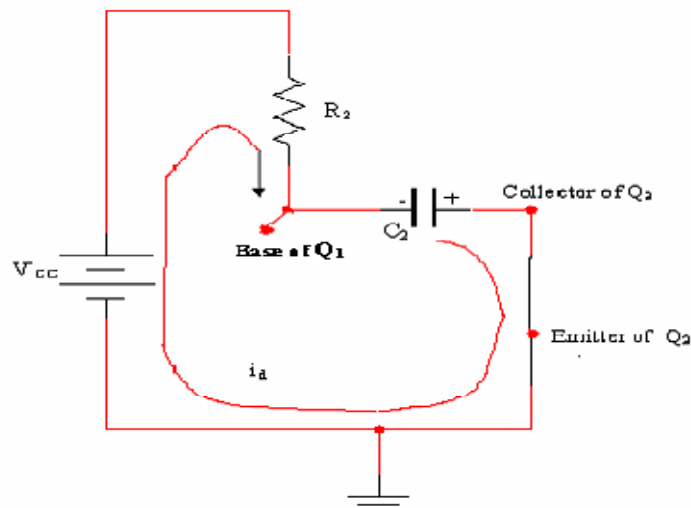
Fig. discharge of C2 through R2

As a result, the voltage at the base of Q1 goes on changing as a function of time .Once this voltage is V_γ, Q1 draws base current. Hence there is a collector current; there is a voltage drop across R_{C1} and the voltage at the collector of Q1 falls. Earlier this voltage was V_{CC} and now it is smaller than V_{CC}. Therefore, the negative step at this collector is coupled to the base of Q2 through C_1. As the collector of Q1 and the base of Q2 are connected through C_1 and as a capacitor will not allow any sudden changes in voltage, whatever is the change that has taken place at the first collector an identical change takes place at the base of Q2. As a result the base current of Q2 is reduced, its collector current is reduced and the voltage at its collector rises. This positive step change is coupled to the base of Q1. Its base current further increases. The collector current increases, the voltage at the collector of Q1 further falls and this change is coupled to the base Q2 and this process is repeated. Thus a regenerative action takes place and Q2 switches into the OFF state and Q1 goes into the ON state.

The waveforms at the base and collectors of Q1 and Q2 are shown below.

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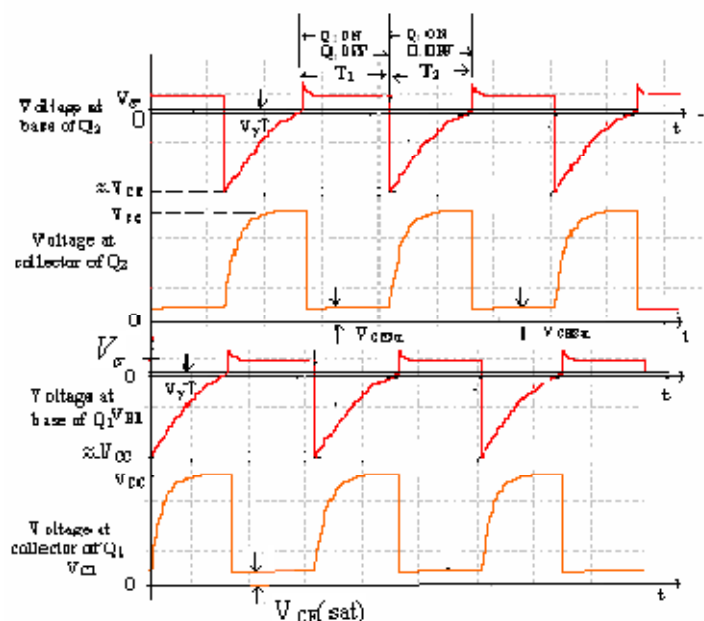
Fig. Waveforms of collector–coupled astable multi

When suddenly the transistor changes from the OFF state to the ON state there could be a small overshoot at this base and at the collector of the other transistor. Further, it is seen that when a transistor changes from the ON state into OFF state, say Q1, its collector voltage is required to abruptly rise to V_{CC}. But when Q1 is OFF and Q2 is ON, there is a charging current of capacitor C1. As a result the voltage V_{C1} will not suddenly rise to V_{CC}. Only when this charging current is zero, the collector voltage reaches V_{CC} . Hence, there is rounding off of the rising edge of the pulse.

Important Questions:

1.What is a multivibrator?what are the types of it?

2.What are types of triggering?

3.What is the resolution time ?how it can be improved?

4.Explain operation of bistable multivibrator? calculate pulse width?

5.Explain operation of Monostable multivibrator? calculate pulse width?

6. Explain operation of astable multivibrator? calculate pulse width?

7. Explain operation of Schmitt trigger?

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UNIT-V
TimeBase Generators

4.1 Voltage Sweep Generators

Introduction:

A linear time-base generator is one that provides an output waveform a portion of which Exhibits a linear variation of voltage or current with time. Earlier, this waveform is used to sweep the electron beam horizontally across the screen. Because of this reason it is called **sweep voltage**.

4.2 Errors that define deviation from linearity

Quality of a sweep is specified by three errors that define deviation from linearity.

Errors that define deviation from linearity are three types.

i)The slope error or speed error e_s

ii)Displacement error e_d

iii)Transmission error e_t

(a)Slope or sweep speed error ,e_s
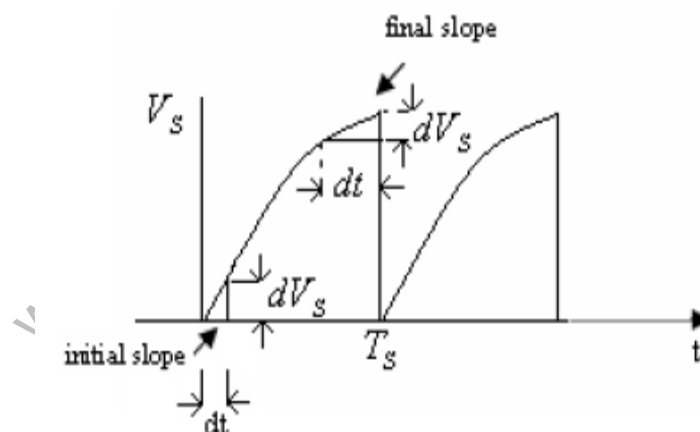
$$e_s = \frac{\text{initial slope - final slope}}{\text{initial slope}}$$

$$= \frac{\left.\dfrac{dV_S}{dt}\right|_{t=0} - \left.\dfrac{dV_S}{dt}\right|_{t=T}}{\left.\dfrac{dV_S}{dt}\right|_{t=0}}$$

(b) Displacement error, e_d :

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It is the maximum difference between the actual sweep voltage and the linear sweep which posses through the beginning and end points of the a sweep.

$$e_d = \frac{(V_s - V_s')_{max}}{V_s}$$
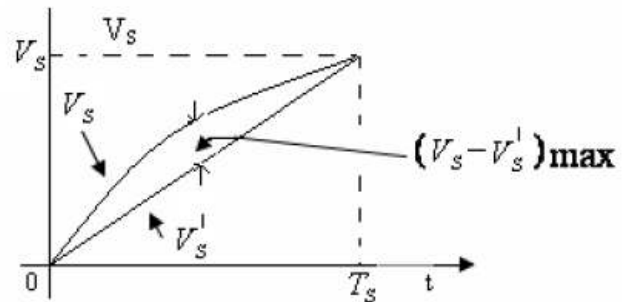
(c)Transmission error, e_t:

If a ramp voltage is transmitted through a highpass RC circuit, the output falls away from the input.

$$e_t = \frac{(V_s' - V_s)}{V_s'}$$

V_s is the actual output
V_s' is the input
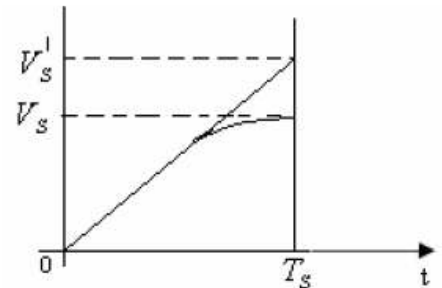
4.3 Exponential sweep generator:

A simple exponential sweep generator and its output are shown in Figs. a) and b) respectively If initially the capacitor is uncharged and t = 0 the switch S is open, the capacitor charges to the supply voltage V.

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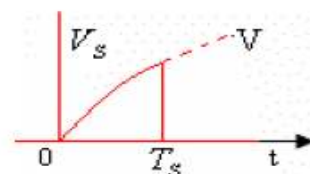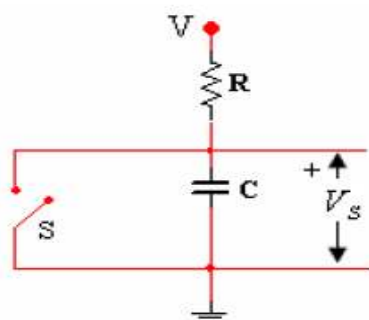
Fig.a) A simple exponential sweep generator   **Fig.b) Output of the sweep**
generator

If the resistance offered by the switch is ideally not zero there is a finite time delay before the
signal reaches its initial value. This time delay is called fly back time, restoration time or
retrace tie.

Normally Tr << Ts , so T= Ts
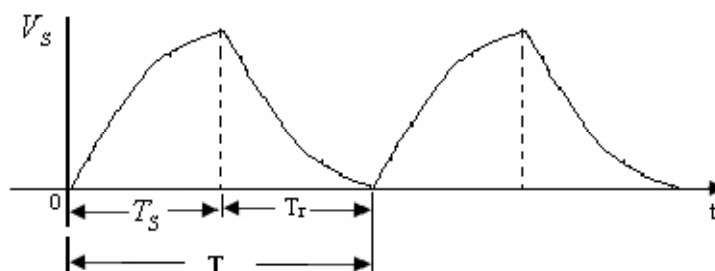
Fig. output waveform of exponential sweep

The voltage variation in the capacitor C is

$$v_c(t) = V_f - (V_f - V_i)e^{-t/\tau}$$
$$= V - (V - 0)e^{-t/\tau}$$
$$v_c(t) = v_s = V(1 - e^{-t/\tau})$$

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Assume that after an interval Ts when v_s = Vs, the switch closes. The charge on the capacitor discharges with a negligible time constant and the voltage abruptly falls to zero at t = TS.

$$v_s = V(1 - e^{-t/\tau})$$

$$\frac{dv_s}{dt} = -Ve^{-t/\tau}\left(-\frac{1}{\tau}\right) = \frac{V}{\tau}e^{-t/\tau}$$

$$\frac{dv_s}{dt}\bigg|t = 0 \quad = \quad \frac{V}{\tau}$$

$$\frac{dv_s}{dt}\bigg|t = T_S \quad = \quad \frac{V}{\tau}e^{\frac{-T_s}{\tau}}$$

$$\therefore e_s = \frac{\dfrac{V}{\tau} - \dfrac{V}{\tau}e^{\frac{-T_s}{\tau}}}{\dfrac{V}{\tau}} = \left[1 - e^{\frac{-T_s}{\tau}}\right]$$

at $t = T_S, v_s = V_s$

Hence $$V_s = V\left(1 - e^{\frac{-T_s}{\tau}}\right)$$

$$\therefore 1 - e^{-T_S/\tau} = \frac{V_s}{V}$$

Substituting, we have

$$e_s = \frac{V_s}{V}$$

From above equation it is evident that e_s is small when V >> V_s. i.e. the linearity improves if V is large when compared to V_s. Therefore, a simple exponential sweep suffers from the disadvantage that a linear sweep is generated only when the sweep amplitude is very much small when compared to the applied d.c. voltage, V

If

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$$\frac{t}{\tau} << 1$$

$$e^{-t/\tau} = 1 - \frac{t}{\tau} + \frac{t^2}{2\tau^2} - \frac{t^3}{6\tau^3} + \Lambda$$

$$v_s = V\left(1 - e^{-t/\tau}\right)$$

$$= V\left[1 - 1 + \frac{t}{\tau} - \frac{t^2}{2\tau^2} + \frac{t^3}{6\tau^3}\Lambda\right]$$

$$= \frac{Vt}{\tau}\left[1 - \frac{t}{2\tau} + \frac{t^2}{6\tau^2}\right]$$

Since $v = V_s$ at $t = T_s$

To first approximation

As this is a linear sweep

$$V_s' = \frac{VT_s}{\tau}$$

Hence, for e_s to be small $\tau >> T_S$

If the actual sweep is non-linear, consider the first two terms

$$v_s = \frac{Vt}{\tau}\left(1 - \frac{t}{2\tau}\right)$$

$$\therefore V_s = \frac{VT_s}{\tau}\left(1 - \frac{T_s}{2\tau}\right)$$

This is a non-linear sweep

Therefore the transmission error e_t is

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'

$$e_t = \frac{V_s' - V_s}{V_s'}$$

$$= \frac{\dfrac{VT_s}{\tau} - \dfrac{VT_s}{\tau}\left(1 - \dfrac{T_s}{2\tau}\right)}{\dfrac{VT_s}{\tau}}$$

$$e_t = \frac{T_s}{2\tau}$$

Now,

$$e_s = \frac{T_s}{\tau}$$

If we relate

e_s and e_t

$$e_t = \frac{T_s}{2\tau} = \frac{e_s}{2}$$

Displacement error, e_d is

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$$e_d = \frac{(v_s - v_s')\,max}{V_s}$$

From equation 6.12

$$v_s = \frac{Vt}{\tau}\left(1 - \frac{t}{2\tau}\right)$$

$$v_s^1 = \frac{Vt}{\tau}$$

$$(v_s - v_s^1) = \frac{Vt}{\tau} \times \frac{t}{2\tau}$$

The deviation is maximum at $t = \dfrac{T_s}{2}$

$$(v_s - v_s^1)_{max} = \frac{VT_s}{2\tau} \times \frac{T_s}{4\tau}$$

$$v_s = \frac{Vt}{\tau}$$

At $t = T_s \quad v_s = V_s$

$$\therefore V_s = \frac{VT_s}{\tau}$$

$$\therefore e_d = \frac{(v_s - v_s^1)_{max}}{V_s} = \frac{\dfrac{VT_s}{2\tau} \times \dfrac{T_s}{4\tau}}{\dfrac{VT_s}{\tau}}$$

$$= \frac{T_s}{8\tau} = \frac{T_s}{8\tau}$$

$$e_d = \frac{1}{8}e_s$$
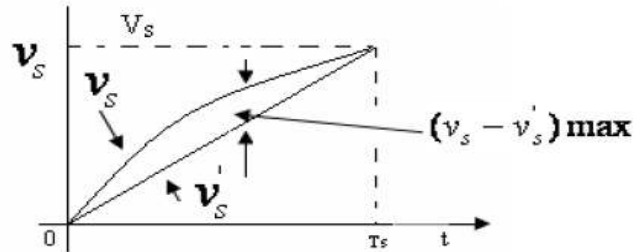
The interrelationship between the three types of errors is given below

$$e_d = \frac{1}{8}e_s = \frac{1}{4}e_t$$

If we know one type of error, we can calculate the other types of errors

$$C = \frac{I}{C}t.$$

If the capacitor is charged with a constant current I then the voltage across *t.*hence, the rate of change of voltage with time is called sweep speed.

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Sweep speed

$$= \frac{I}{C}$$

4.4 UJT sweep generator:

In the exponential sweep generator, a UJT can be used as switch S. The UJT and its d.c circuit are shown in figs. below. A UJT consists of an N-type semiconductor bar with leads B_1 and B_2 drawn. Emitter is a P-type material and it is heavily doped. Let the bias voltage V_{BB} be applied.

Fig.(b) d.c.circuit
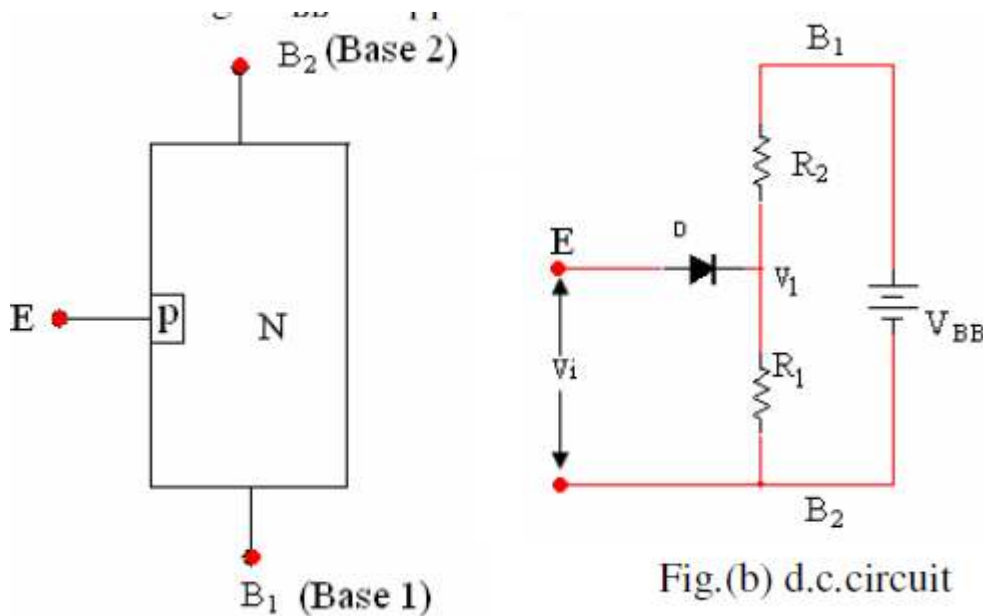
We have, $V_1 = V_{BB} \dfrac{R_1}{R_1 + R_2}$

$$= V_{BB} \frac{R_1}{R_{BB}} = \eta V_{BB}$$

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Where η= Intrinsic stand-of-ratio (lies around 0.7)

As long as $V_i \ll \eta V_{BB}$ D is OFF.

When $V_i > \eta V_{BB}$ D is ON and a large number of charge carriers exist on the N-side, reducing the resistance and the device conducts heavily, switch S is closed. The V-I characteristic of a UJT is shown in fig.c
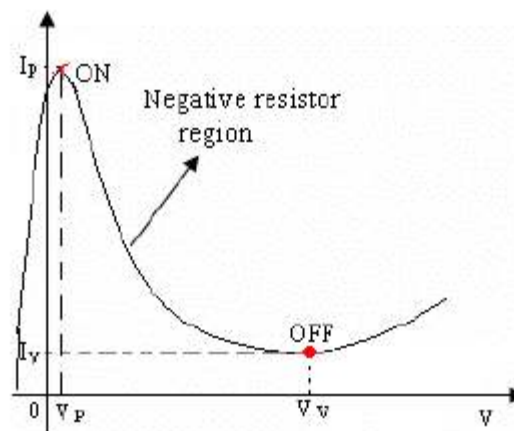
Fig.c. V-I characteristic of UJT

An exponential sweep generator using UJT is shown in fig below
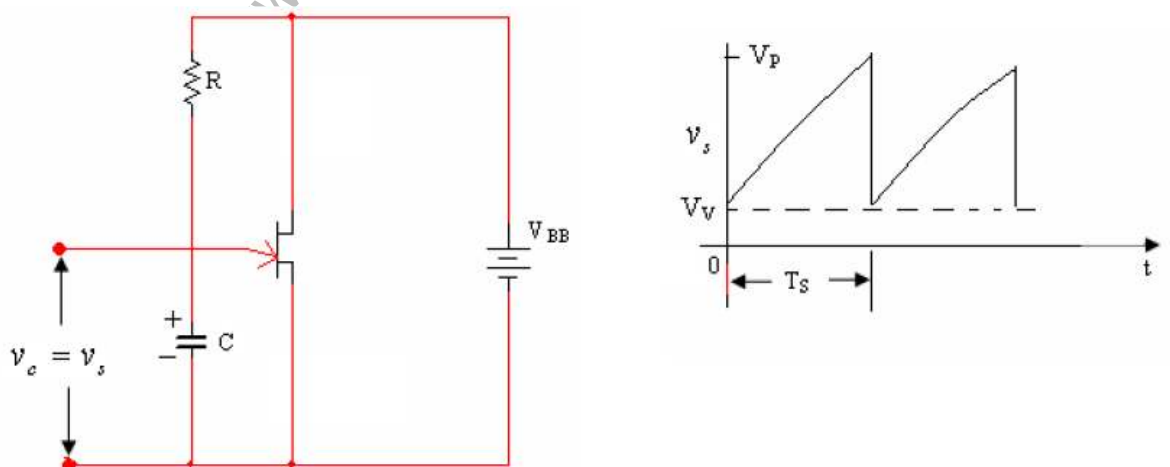
Fig.c A practical UJT sweep generator and its output

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$$v_s = V_{BB}\left(1 - e^{-t/\tau}\right)$$

At $t = T_s, v_s = \eta V_{BB}$

$$\eta V_{BB} = V_{BB}\left(1 - e^{-t/\tau}\right)$$

$$V_{BB}e^{-T_s/\tau} = V_{BB}(1-n)$$

$$V_{BB}e^{-T_s/\tau} = V_{BB}(1-n)$$

$$T_s = \tau \ln \frac{1}{(1-n)}$$

Alternately

$$v_s = V_f - (V_f - V_i)e^{-t/\tau}$$

$$= V_{BB} - (V_{BB} - V_v)e^{-t/\tau}$$

At $t = T_s, v_s = V_s = V_p$

$$V_p = V_{BB} - (V_{BB} - V_v)e^{-T_s/\tau}$$

$$T_s = \tau \ln \frac{(V_{BB} - V_V)}{(V_{BB} - V_P)}$$

4.5 Time-base generators-general considerations:

A simple exponential sweep generator essentially produces a nonlinear sweep voltage. Consider an auxiliary generator v . If V always kept equal to the volt across C Then net voltage in the loop is V. Then

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$$i = \frac{V}{R}$$

i.e. the capacitor charging current is constant and perfect linearity is achieved. Let us identify three nodes X, Y and Z. In a circuit one terminal is chosen as a reference terminal or ground terminal. Ground in a circuit is an arbitrarily chosen reference terminal.
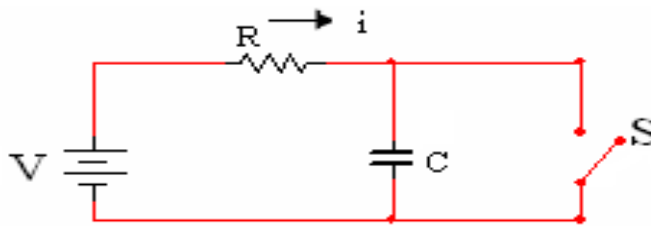
Fig. Method to linearize a non-linear sweep

Miller Sweep:

Now let Z be the ground terminal, and redrawing the above circuit
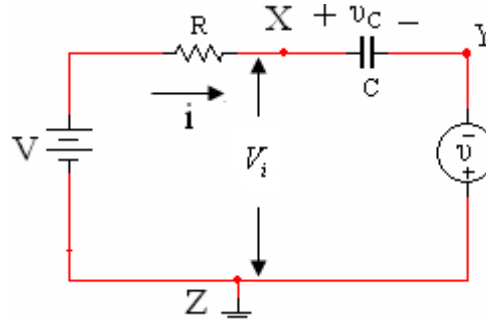
Fig. The sweep generator with Z as the ground terminal

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Since $v_{C=}$ *v and v_i=0* .Hence if the auxiliary generator is replaced by an amplifier with X and Z as input terminals and Y and Z as output terminals, then the gain of the amplifier A should be infinity. The above circuit reduces to that shown in fig. below which is called Miller Sweep.
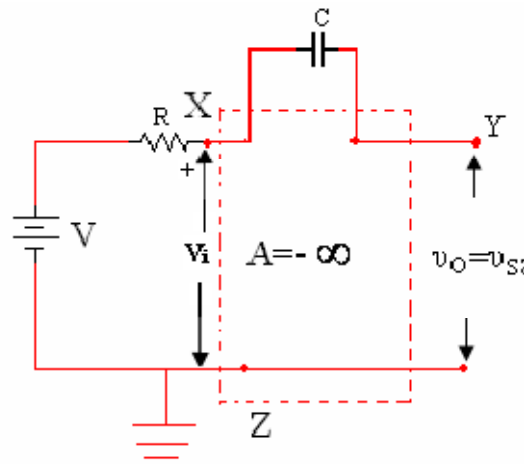
Fig. equivalent circuit.

Bootstrap Sweep: Let Y be the ground terminal redrawing the above circuit and replacing the auxiliary generator by an amplifier with X and Y as input terminals the amplifier should have again of unity as $v=V_c$

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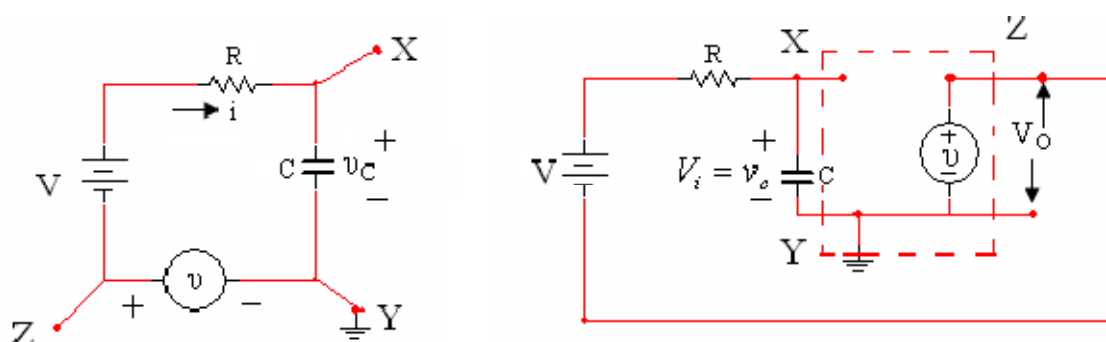
Fig. the sweep generator, with Y as the ground terminal

Replacing the generator by amplifier, the circuit is redrawn as in fig. below
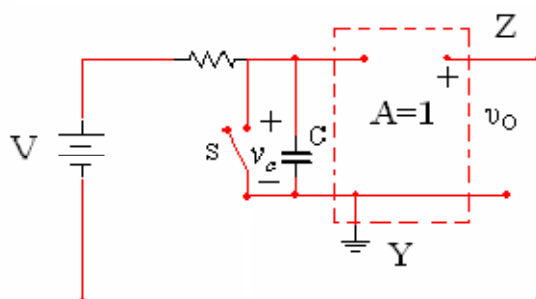
fig. Bootstrap sweep generator

This type of sweep generator is called a Bootstrap sweep generator

Slope error of a Miller's sweep:
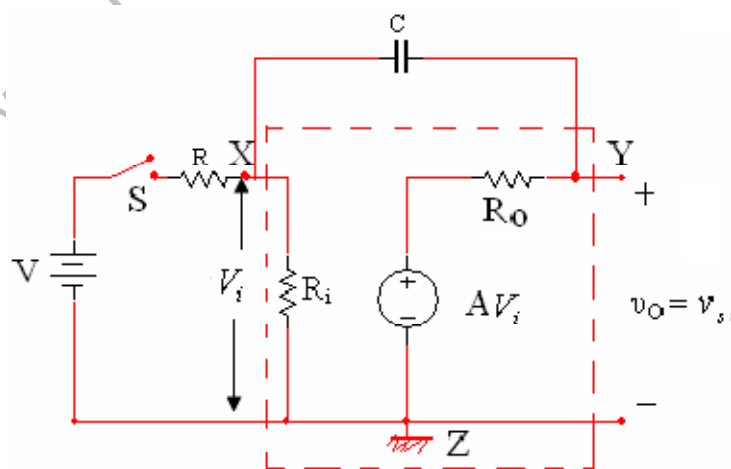
Fig. equivalent circuit

R_i = Input resistance of the amplifier

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R_o = Output resistance of the amplifier
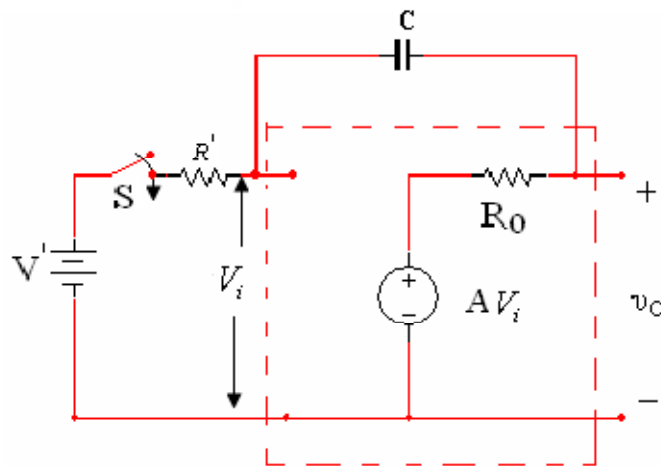
Fig. Thevinens equivalent circuit

Thevenising the circuit at the input

$$V' = V \frac{R_i}{R + R_i} = V \frac{1}{1 + \dfrac{R}{R_i}}$$

$$R' = \frac{R \times R_i}{R + R_i}$$

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Let $R_0 = 0$

At $t = 0$ the voltage across the capacitor is zero

$$\therefore v_i - Av_i = 0, \qquad v_i(1-A) = 0, \quad v_i = 0$$

$$v_i = AV_i = V_o = 0$$

As $t \to \infty$, the capacitor is fully charged no current flows in it and hence can be replaced by an open circuit for

the purpose of finding out the output voltage. The resultant circuit is

At $t = \infty$, $V_i = V'$

Hence $V_0 = AV'$

We know that $e_s = \dfrac{V_s}{V}$

where V_s = sweep amplitude

V = total peak to peak excursion of the exponential
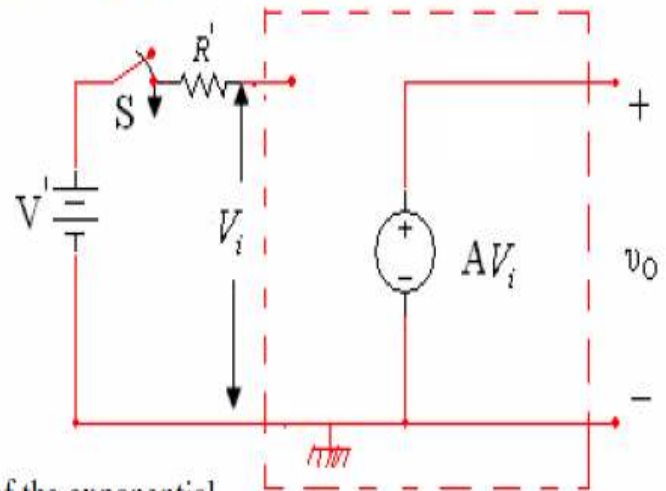
Hence, $e_{s_{Miller}} = \dfrac{V_s}{V_0} = \dfrac{V_s}{/A/V'} = \dfrac{V_s}{/A/} \times \dfrac{1}{V'}$

Substituting , $e_{S_{Miller}} = \dfrac{V_s}{/A/} \times \dfrac{1+R/R_i}{V}$

$$= \dfrac{V_s}{V} \times \dfrac{1+R/R_i}{/A/} \text{ ,where } \dfrac{V_s}{V} \text{ is the slope error of the exponential sweep.}$$

$\therefore e_{s_{Miller}} = e_s \times \dfrac{1+R/R_i}{|A|}$ .Even if R_i is small, as A is large, the slope error of a Miller's

sweep is very small. Hence, for all practical purposes this sweep generator produces a near linear sweep.

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Slope error of Bootstrap sweep generator:
Consider the Bootstrap sweep generator in fig I)
If initially the capacitor is uncharged and if S is closed at t = 0

$V_o = -V \times \dfrac{R_o}{R + R_o}$ from fig.ii)

And as R_o of emitter follower is very small.

$V_0 \approx 0$

Fig.i) Bootstrap sweepgenerator
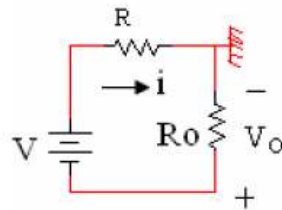
Fig ii) Circuit to calculate the output at t = 0
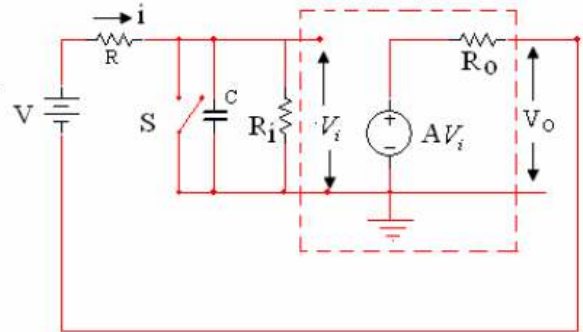
As t $\longrightarrow \infty$, C is fully charged and is open circuited, fig.6.20

$V_0(t \to \infty) = \dfrac{V(AR_i - R_0)}{R_0 + R + R_i(1 - A)}$

Dividing by R_i

$V_0(t \to \infty) = \dfrac{V(A - R_0 / R_i)}{(1 - A) + \dfrac{R}{R_i} + \dfrac{R_0}{R_i}}$
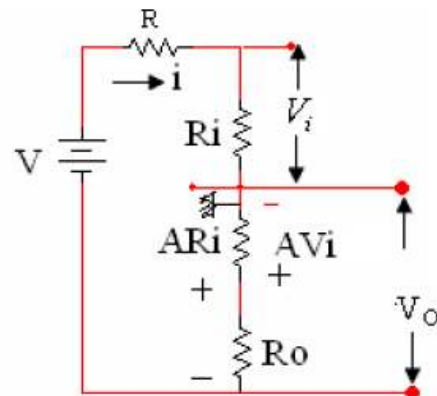
Fig 6.20 circuit to calculate the output as $t \to \infty$

$V_0(t \to \infty) \approx \dfrac{V}{(1 - A) + R / R_i}$

R_o is the output resistance which is small and R_i is its input resistance which is large.

$\therefore \dfrac{R_0}{R_i}$ is negligible and $A \approx 1$

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Equation reduces to

$$\therefore e_{sBootstrap} = \frac{V_s}{V}\left(1 - A + R/R_i\right)$$

$$\cong e_s \frac{R}{R_i}$$

If R=R$_i$, $e_{sBootstrap} = e_s$ .That is the Bootstrap circuit will not provide any improvement in linearity. For this sweep to be linear Ri >>R

Transistor Miller Sweep: Consider the working of the triggered transistor Miller's sweep generator as shown below.
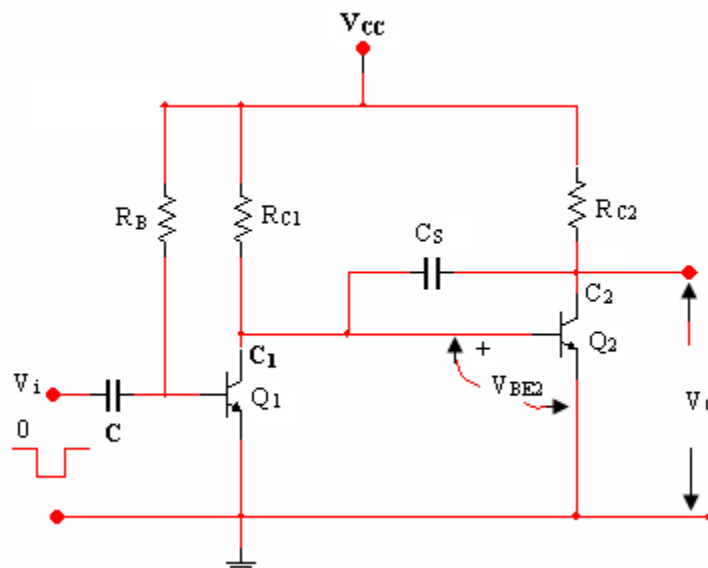
Fig. Transistor Miller sweep

The circuit conditions are adjusted such that when the input is zero *Q1* is ON and is in saturation. Therefore the voltage at C_1 (collector of Q1) is *V* (*sat*) *CE*=0. Transistor 2*Q2* is OFF since v_{be2}= 0 The voltage at C_2 (collector of Q2) is V_{cc} .The voltage across the capacitor *C* is V_{cc} When the input signal goes negative, 1 *Q* is OFF and the voltage at *C1* rises and *Q2* goes ON. The charge on the capacitor *C2* discharges. Hence the output is a negative going ramp. Again at the end of the input
pulse,Q1 goes ON,Q2 goes OFF and the output again reaches VCC . The waveforms are shown in fig

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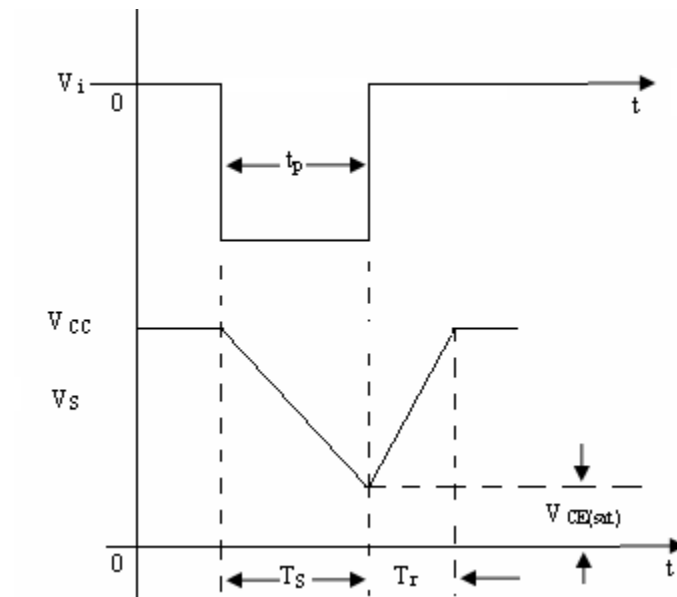
Fig Waveforms of a transistor Miller sweep

Bootstrap circuit: The circuit of a Bootstrap sweep generator is shown in fig.below.
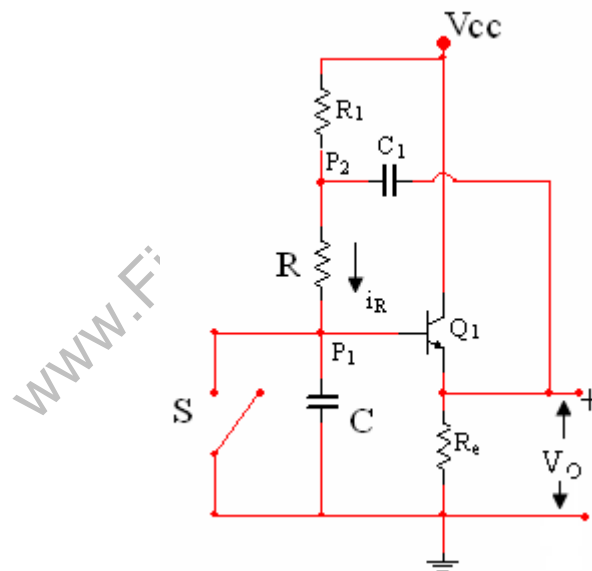
Fig. Bootstrap sweep generator

At t = 0, the switch S is open and the capacitor charges. C_1 is very large. Therefore, it is assumed that the voltage across C_1 remains unaltered during the sweep period. Let the

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voltage gain of the emitter follower remain constant. Then the voltage at P_2 (**output** of the emitter follower) follows P_1 (input of the emitter follower). The voltage between P_2 and P_1 will remain invariant and the current R_I through R is constant .As the capacitor charges with a constant current, the resultant sweep is linear.

The circuit of a practical Bootstrap ramp generator is shown.
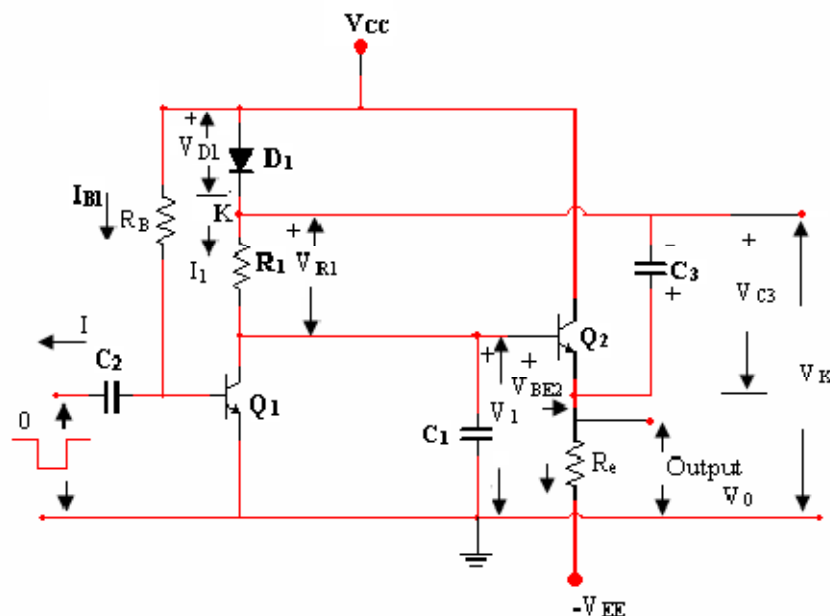
Fig. A practical Bootstrap sweep generator

The ramp is generated across capacitor C_1 which is charged from the current through R $_1$. The discharge transistor Q_1 when ON keeps the V_1 at V $_{(sat)\ CE}$ until a negative input pulse is applied. Q_2 is an emitter follower with low output resistance. Emitter resistance R_e is connected to a negative supply Vee instead of referencing to ground to ensure that Q_2 remains conducting even when its base voltage 1 V is close to ground. Capacitor C_3, called bootstrapping capacitance, has a much higher capacitance than C_1 . C_3 is meant to maintain a constant voltage across R_1 and thus maintain the charging current constant.

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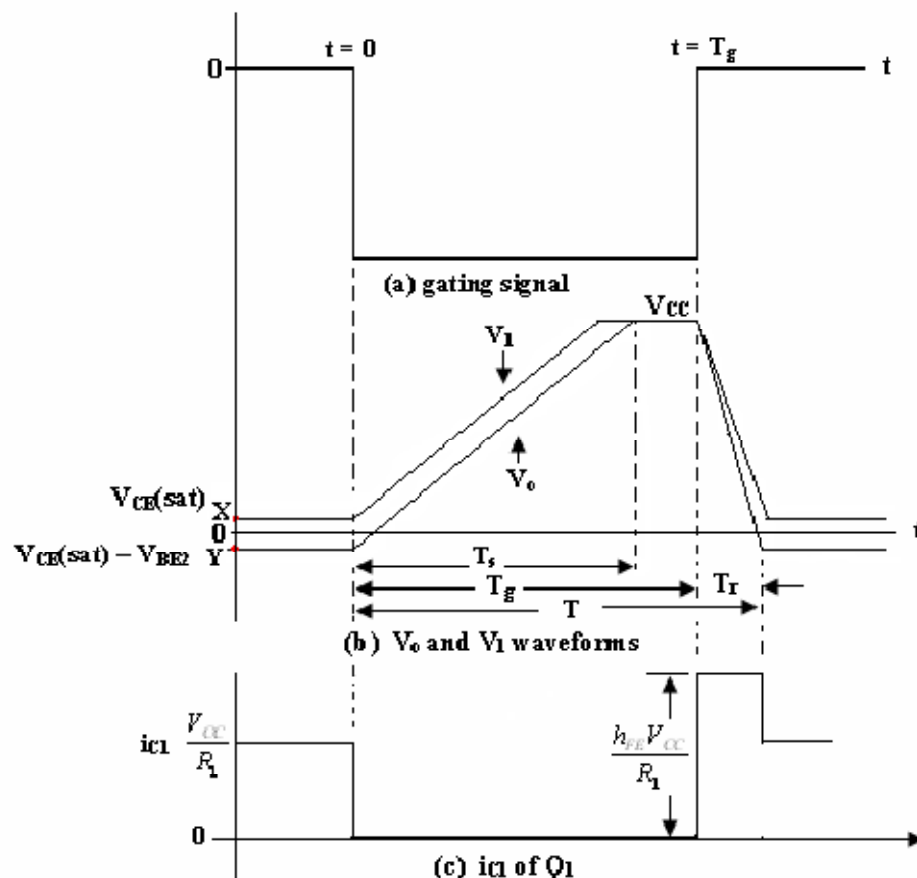
Fig.6.27 waveforms of the bootstrap circuit

Circuit operation:

Quiescent conditions:

As long as the input trigger signal is zero, Q1 has sufficient base current . So Q2 goes into saturation. Therefore the voltage V_1 across the capacitor C_1 is $V_{CE(sat)}$. $V_1 = V_{CE(sat)}$

Q2 is an emitter follower for which input is V_1 and its output Vo is $V_0 = V_1 - V_{BE2}$ which is very less

For all practical purposes both V_1 and Vo are zero. The voltage across R_1 is

$V_{R1} = V_{CC} - V_{D1} - V_{CE(sat)} \_ V_{CC}$

Also, the voltage across C_3 is $V_{C3} = V_{CC}$.

Hence the current I_1 in R_1 is

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$$I_1 = \frac{V_{CC}}{R_1}$$

As the base current of Q2 is smaller than the collector current of Q1

$$i_{C1} \approx I_1 = \frac{V_{CC}}{R_1} \quad \text{and} \quad I_{B1} = \frac{V_{CC}}{R_B}$$

For Q1 to be in saturation, $i_{B1(sat)} > i_{B1(active)}$

$$\therefore \frac{V_{CC}}{R_B} > \frac{V_{CC}}{h_{FE} R_1}, \qquad \text{or } R_B < h_{FE}R_1$$

Sweep generation:

At t=0, when voltage at the base of Q1 goes negative, Q1 is OFF. There is no current into the collector lead of Q1 and instead this current flows through C_1 charging it. As the voltage across the capacitor C_1 varies as t

$$\frac{i}{C} t$$

and so does the output.

$$V_0 = \frac{V_{CC}}{R_1} \cdot \frac{t}{C_1}$$

When the sweep starts, D1 is reverse biased and is an open circuit. The changing current I_1 to C_1 through R_1 is supplied by C_3 which is charged to V_{CC}.

It is known that the output V_O varies linearly only when the duration of the gate signal (Tg) is small so that in this period V_O does not reach V_{CC}. However, if Tg is large, the output V_0 may reach V_{CC} even before Tg. When $V_0 = V_{CC}$, the voltage V_{CE2} of Q_2 is practically zero

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(saturation). Q2 no longer behaves as an emitter follower. V_0 and V_1 therefore remain at V_{CC}. The current $V_{CC}/R_1.V_{CC}$ now flows through C_3, R_1 and through the base emitter diode of Q2.therby changing voltage across C_3 by a small amount .

If Ts < Tg ,Then at t = Ts, Vs = V_{CC}

Hence

$$V_{CC} = \frac{V_{CC}\,T_s}{RC}, \text{ or } T_s = RC$$

On the other hand if Vs < V_{CC}, the maximum ramp voltage is

$$V_s = \frac{V_{CC}\,T_g}{RC}$$

4.6 Current Sweep Generators

Introduction:

Application of electromagnetic deflection is used in these current sweep generators.

When a voltage is applied to a coil of inductance L, the current in L increases linearly with time. Usually a coil or set of coils called yoke is mounted external to the gun structure of the tube and the current in yoke produces a magnetic field that causes deflection of the electron beam.

If at a time t = 0, a voltage V is applied to a coil of inductance L in which the current is initially zero, then the inductor current L

$$i_L = \frac{V}{L}t$$

A time base circuit using this principle is shown in fig.a

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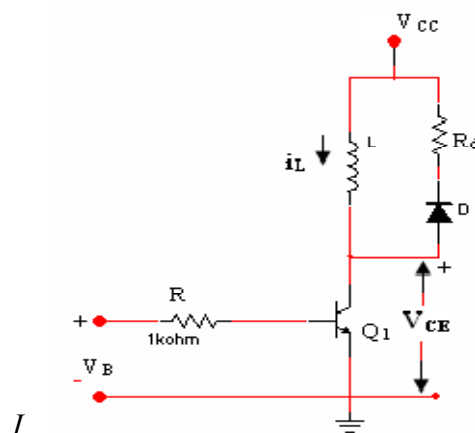
Fig.a Current sweep generator

The gating waveform V_b operates between two levels. The lower level keeps the transistor in cut off while the upper level drives the transistor into saturation. As long as the input is negative Q1 is biased OFF and the inductor current is zero. At t=0+ as the input goes positive Q1 is driven into saturation. The current i_L increases linearly with time. During the sweep period the diode D does not conduct since it is reverse-biased. The sweep terminates at t=T_s when the trigger signal drives the transistor to cut off. The inductor current then continues to flow through the diode D and the resistance R_d till it decays to zero. This decay is exponential with a time constant

$$\tau = \frac{L}{R_d}$$

Where R_d is the sum of the damping resistance and the diode forward resistance.

The inductor current attains a maximum value of $I_{\underline{l}}$ in fig b.

Before the transistor is turned ON, and sometime after it has been turned OFF, *CE*

$$V_{CE} = V_{CC}.$$ When the transistor is ON,

$$V_{CE} = V_{CE}(sat),$$

Is very low. At t=Ts Q1 is turned OFF.A spike of amplitude *I R* appears across the inductance L. This peak voltage must be limited to make sure that it would not exceed the

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break down voltage of the collector base junction. I_l is normally chosen on deflection requirements, and a spike of magnitude $I\,R$ is generated. Thus there is an upper limit to the size of R. The spike decays with the same time constant as the inductor current. Thus we see that the spike duration depends on L, whereas the spike amplitude does not. So far we have neglected the resistance of the inductor RL and the collector saturation resistance of the transistor, R_{CS}.

Taking R_L and R_{CS} into account

$$i_L = \frac{V_{CC}}{R_L + R_{CS}}(1 - e^{\frac{-(R_L+R_{CS})t}{L}})$$

Expanding it in to series

$$i_L \approx \frac{V_{CC}}{R_L + R_{CS}}\left[1 - 1\frac{+(R_L+R_{CS})t}{L} - \frac{(R_L+R_{CS})^2 t^2}{2L^2}\right]$$

$$i_L = \frac{V_{CC}}{L}t\left[1 - \frac{1}{2}\frac{(R_L+R_{CS})t}{L}\right]$$

The slope error e_s is $\quad e_s = \dfrac{I_L}{V_{CC}/(R_L+R_{CS})} = \dfrac{(R_L+R_{CS})I_L}{V_{CC}}$

The current sweep is linear if the slope error is small. Therefore, to ensure linearity the Voltage must be small when compared with the supply voltage V_{cc}.

$$(R_L + R_{CS})I_L$$

As this simple current sweep may not produce a linear output, we may think of methods that help in linearising the sweep. One simple method to produce a linear current sweep is by adjusting the driving waveform.

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4.7 Linearity correction through adjustment of the driving waveform:

The non-linearity encountered in this circuit results from the fact that as the yoke current increases the current in the series resistance also increases. Consequently the voltage across the yoke decreases and the rate of change of current decreases. We may compensate for the voltage developed across the resistance as shown in fig.c
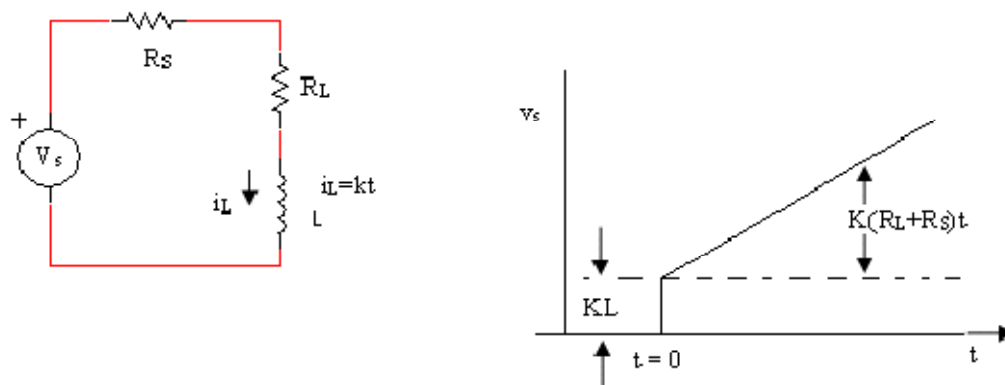
Fig.c Driving waveform for generating a linear current sweep

Let R_s be the internal resistance of the source V_s. The total circuit resistance $(R_S + R_L)$ .we want the inductor current to vary linearly

i.e. $i_L = Kt$, where K is the constant of proportionality.

If $i_L = Kt$,then the source voltage V_S is

$$V_S = L\frac{di_L}{dt} + (R_s + R_L)i_L$$

If $i_L = Kt$, $\frac{di_L}{dt} = K$

$$\therefore V_S = LK + (R_s + R_L)Kt$$

This waveform consists of a step by followed by a ramp $(R_s + R_L)Kt$. Such a waveform is called a trapezoidal waveform.

The Norton representation of the driving source, using above equation

$$i_s = \frac{V_S}{R_S} = \frac{LK}{R_S} + (1 + \frac{R_L}{R_S})Kt$$

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This waveform consists of a step by followed by a ramp
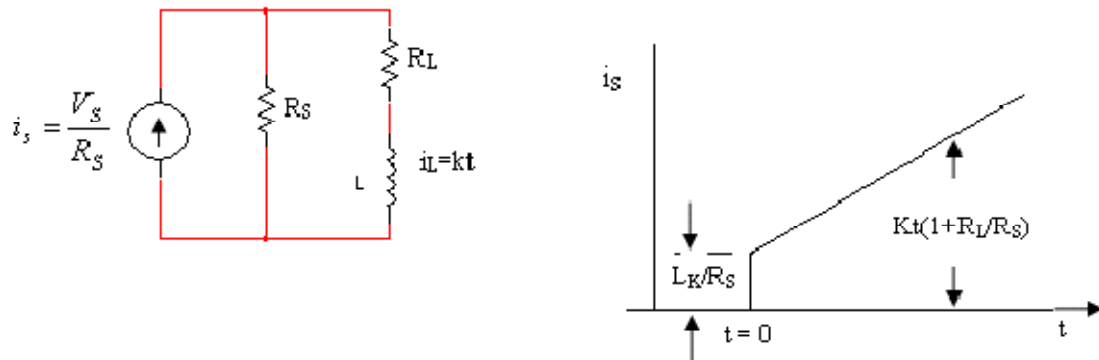
Fig.d Trapezoidal current source and the wave form

Thus a trapezoidal driving waveform generates a linear current sweep. At the end of the sweep the current once again will return to zero exponentially with a time constant

$$\tau = \frac{L}{R_S + R_L}.$$

Generally,

$$R_S \gg R_L \text{ hence } \tau \approx \frac{L}{R_S}$$

If R_s is small the current will decay slowly and a long period will have to elapse before another sweep is possible. But the advantage is that, the peak voltage developed across the current source (transistor) will be small. Alternately, if R_s is large, the current will decay rapidly, but a large peak voltage will appear across the source.

Generally, one has to strike a compromise such that the spike amplitude is not appreciably large and at the time the inductor current decays in a smaller time interval. To achieve this normally a damping resistance.R_d is connected across the yoke to limit the peak voltage.Let R be the parallel combination of R_s and R_d . Then the retrace time constant is

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$$\tau_r = L/R.$$

Now, how to generate this trapezoidal waveform which when applied as a driving source will result in the linearity of the current sweep.

The trapezoidal waveform required is generated using the circuit in fig below.
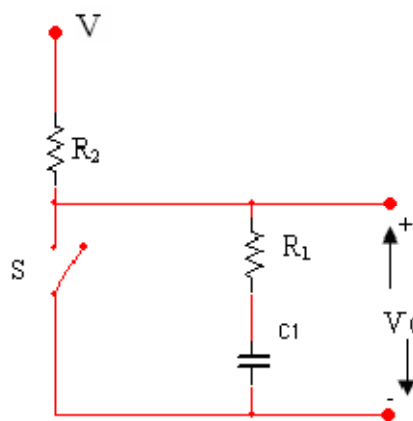
Fig . Generation of trapezoidal waveform

$$v_o = V - \frac{R_2}{R_1 + R_2} V e^{-t/(R_1+R_2)C_1}$$

Generally

$$R_2 >> R_1$$

$$v_o = \frac{V(R_1 + R_2) - R_2 V e^{-t/(R_1+R_2)C_1}}{R_1 + R_2}$$

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Dividing by R_2

$$v_o = \frac{V(1+\frac{R_1}{R_2}) - Ve^{-t/(R_1+R_2)C_1}}{R_1/R_2+1}$$

$$\approx \frac{VR_1}{R_2} + V - Ve^{-t/R_2C_1}$$

$$= \frac{VR_1}{R_2} + V(1 - Ve^{-t/R_2C_1})$$

$$v_0 = V\frac{R_1}{R_2} + \frac{Vt}{R_2C_1}(1 - \frac{t}{2R_2C_1})$$

If $\frac{t}{2R_2C_1} \ll 1$

$$v_0 = V\frac{R_1}{R_2} + \frac{Vt}{R_2C_1}$$

Thus v_0 is a step followed by ramp.

Important Questions:

1.Explain the operation of UJT Sweep Generator?

2.What is a Sweep waveform and what are three types of errors that define deviation from linearity?

3.Explain miller Sweep circuit?

4. Explain Bootstrap Sweep circuit?

5. Explain simple exponential Sweep generator circuit?

Pulse & Digital Circuits

UNIT - VI
Logic Families & Sampling Gates

Logic circuits:

Introduction :

In large scale digital systems such as in a digital computer, data processing, control or digital communication system a few basic operations are needed. These are four circuits known as OR, AND, NOT and flip-flop. These are called logic gates or circuits because their operations uses logic algebra or Boolean algebra.

Logic System :

In a de-or level-logic system a bit is implemented as one of two voltage levels as shown below.
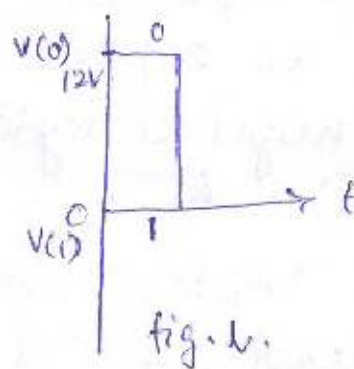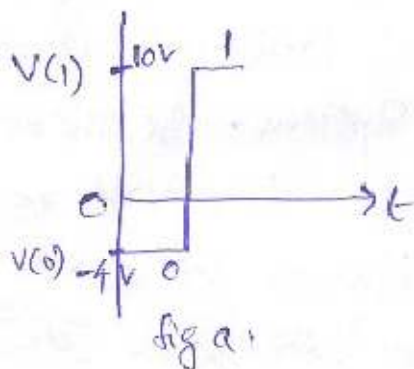
In fig (a) more positive voltage is the level 1 and the other is the level 1 and the other is the level 0. this is called as de-positive logic. In fig(b) more negative voltage state is represented with 1 and more positive with 0, which is known as negative logic.

In a dynamic or pulse logic system of bit is recognized by the presence or absence of a pulse. In a dynamic positive logic system, positive pulse indicates 1 and its absence or no pulse signifies 0.Similarly a negative pulse indicates 1 in a dynamic negative system and no pulse or absence specifies 0.

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OR gate :

The output of an OR assumes 1 state if any one of the inputs assumes 1 state. The N input logic circuit with output y is represented as shown below. Truth table for 2 input circuit is mentioned to understand simply.
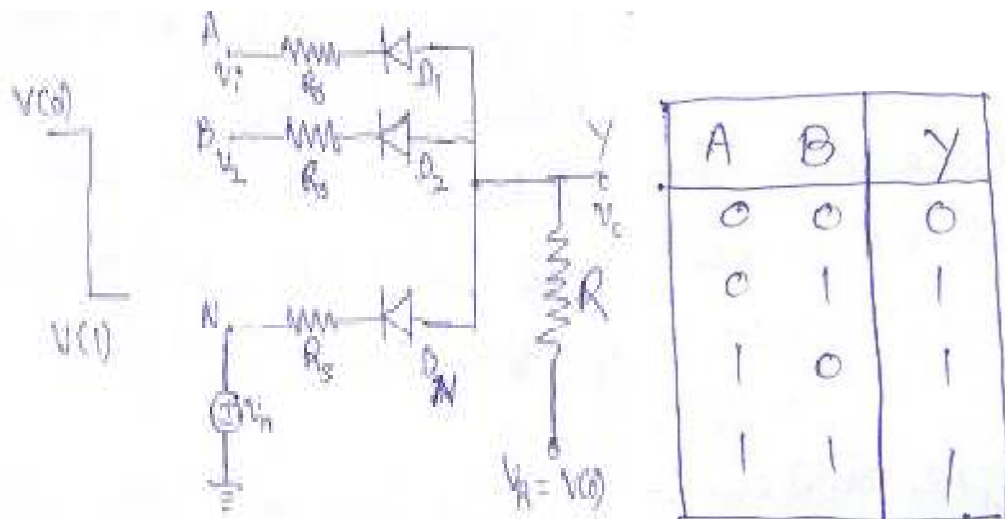
In the circuit, since the diodes only are used, it is called diode logic (DL) system. Here upper and lower voltages are represented with $V(0)$ and $V(1)$ respectively, it is a negative logic system. If all inputs are applied by $V(0)$, the the voltage across each diode is $V(0)-V(0)=0$. Hence no diode is forward biased by at least the cut voltage V_γ and none of the diode conducts. Therefore the output voltage is $V_0 = V(0)$ and so the gate is said to be in the 0 state. If one of the inputs, say A, is changed to 1 state and for negative logic system, the level $V(1)$ makes that diode forward bias. So diode D_1 conducts and hence current flows in the resistance R. Therefore the output is given by

$$V_0 = V(0)[V(0) - V(1) - V_\gamma] \frac{R}{R + R_s + R_f}$$

Where R_f is the forward resistance and $S R$ is the source resistance.

As R_f and R_s are smaller than R,

The above expression can be reduced to

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$$V_0 = V(1) + V_\gamma$$

So the output voltage exceeds the more negative level $V(1)$By V_γ that means output voltage is smaller by V_γ than the change in input voltage. If for any reason the level $V(1)$ is not identical for all inputs then the most negative value of $V(1)$(for negative logic) appears at the output. A positive logic OR gate can also be designed but this is same as above circuit except all diodes must be reversed.

AND gate :

Definition :

The output an AND assumes the 1 state if and only if all the inputs assume the 1state. A diode (DL) configuration for a negative AND gate is shown below with truth table for 2 inputs.
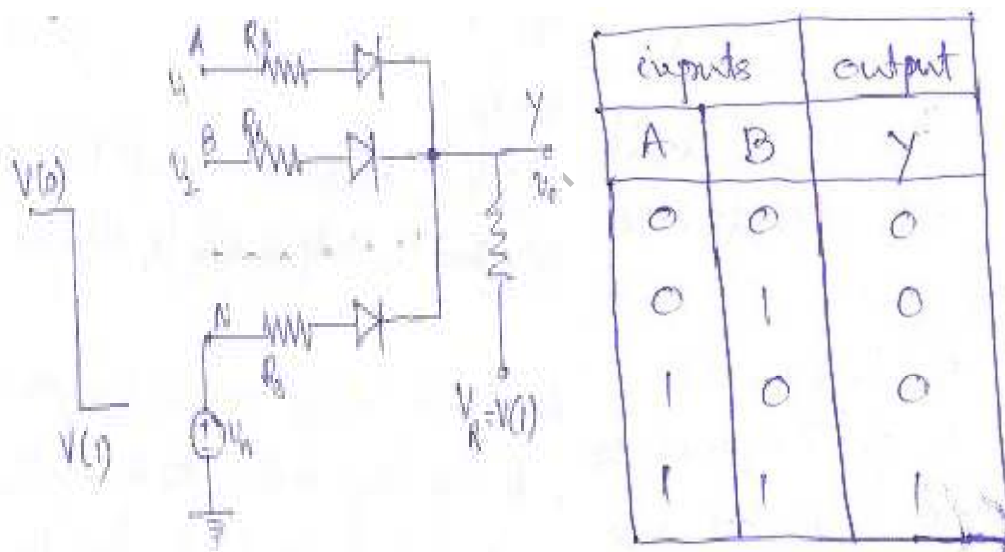
To understand the operation simply, assume that all source resistances R_S are zero and that the diodes are ideal. If any input is at the 0 level $V(0)$, the diode connected to this input conducts and the output is clamped at the voltage $V(0)$ or $Y = 0$.

If all the inputs are at the 1 level $V(1)$, then all diodes are reverse biased and output voltage is $V(1)$

or y = .1

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Taking source resistance R_S and diode forward resistance R_F into account, we can determine the output of the circuit for positive logic system. Assume in inputs out of n are at $V(1)$ and hence in diodes are reverse biased. The remaining n-m diodes conduct and hence the effective circuit of these diodes in parallel consists of

$$(R_s + R_f)/(n-m) \text{ in}$$

series with a voltage V_γ. Then the output is

$$V_0 = V(1) - [V(1) - V(0) - V_\gamma] \frac{R}{\left[R + \frac{(R_s + R_f)}{n-m} \right]}$$

NOT or INVERTER Circuit

The NOT logic circuit has a single input and single output. It is defined as the output of a NOT circuit takes on the 1 state if and only if the input does not take on the 1 state. The following transistor circuit performs the logic NOT operation in the dc positive logic system.
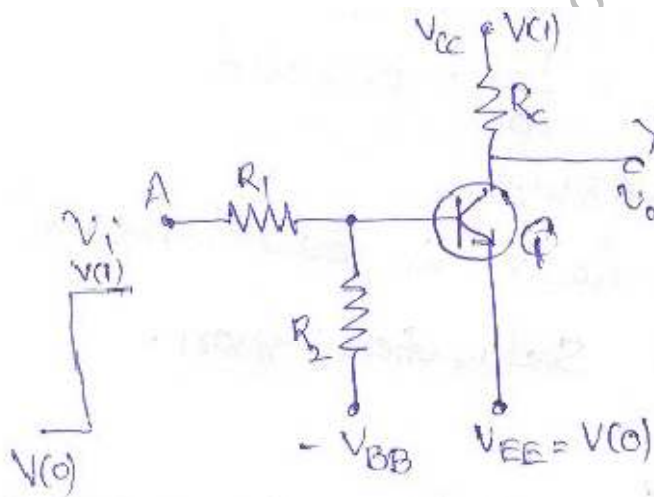
_If the input is low then the parameters are chosen so that in Q is OFF and hence output is high.

_ When the input is changed to high state , then the circuit parameters are picked so that the transistor Q is in saturation and then output is zero. the saturation voltage will be very low i.e., a few tents of a volt and that can be neglected.

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NAND Gate

A negation following an AND gate is called a NOT-AND or NAND gate. A positive NAND circuit is implemented by a cascade of diode AND and a transistor NOT as shown in the circuit.

inputs		output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0
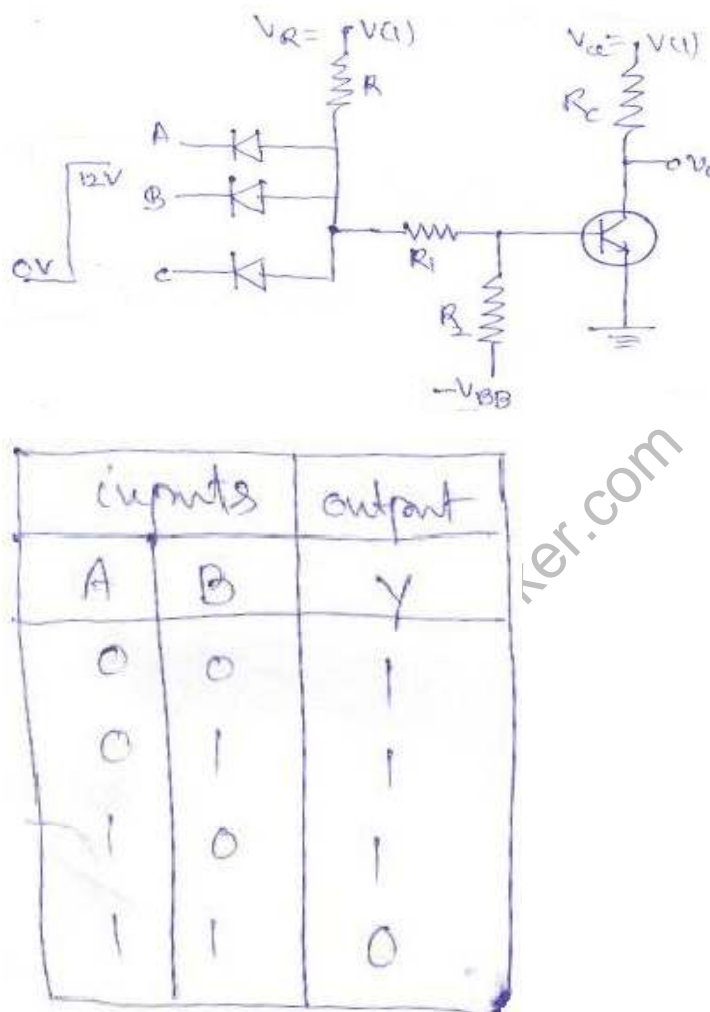
Fig.3 input NAND gate

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Truth table for two input NAND circuit is mentioned. Similarly a NOR circuit can also be designed by cascading a diode NOT with a resistance OR But the positive NAND gate is same as that of a negative NOR. These NAND and NOR circuits are involving with diodes and transistors, these are also called as Diode-Transistor logic (DTL) gates.

In the above DTL configurations, the same can be implemented by omitting the diodes. Then logic gates are called transistor resistor logic TRL or Resistor-Transistor Logic RTL. If these resistors are shunted with capacitors then they are called as Resistor- Capacitor-Transistor (RCTL) logic circuits.

6.1 Logic IC families:

- Most of logic gates, flip-flops, counters, shift registers, encoders, and decoders are available in several logic families.
- TTL, ECL, IIL, MOS, CMOS are the various logic families.

6.2 TTL two input NAND gate:

The following circuit diagram represents the TTL NAND gate with multi emitter transistor.

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Operation of the circuit:

The maximum number of emitters connected to the transistor is 8. When the two inputs A and B applied to the circuit, the two emitter base junctions are reverse biased and hence Q1will be in off state. The collector of Q1is connected to base of Q4 and collector voltage is high because of it is in off state hence base voltage of Q4 is also high hence Q4 will be on and Q3 off and hence Q2 is on and final output is low. If one of the inputs is low and another is high, Q1will be in off state. The collector of Q1is connected to base of Q4 and collector voltage is high because of it is in off state hence base voltage of Q4 is also high hence Q4 will be on and Q3 off and hence Q2 is on and final output is low. When both the inputs A and B are low emitter base junctions are forward biased and hence Q1will be in on state. The collector of Q1is connected to base of Q4 and collector voltage is low because of it is in on state hence base voltage of Q4 is also low hence Q4 will be off and Q3 on and hence Q2 is off and final output is high.

By the above operation we can say that TTL acts as NAND gate.

6.3 ECL NOR GATE:

The following circuit diagram represents the ECL NOR GATE with three inputs.
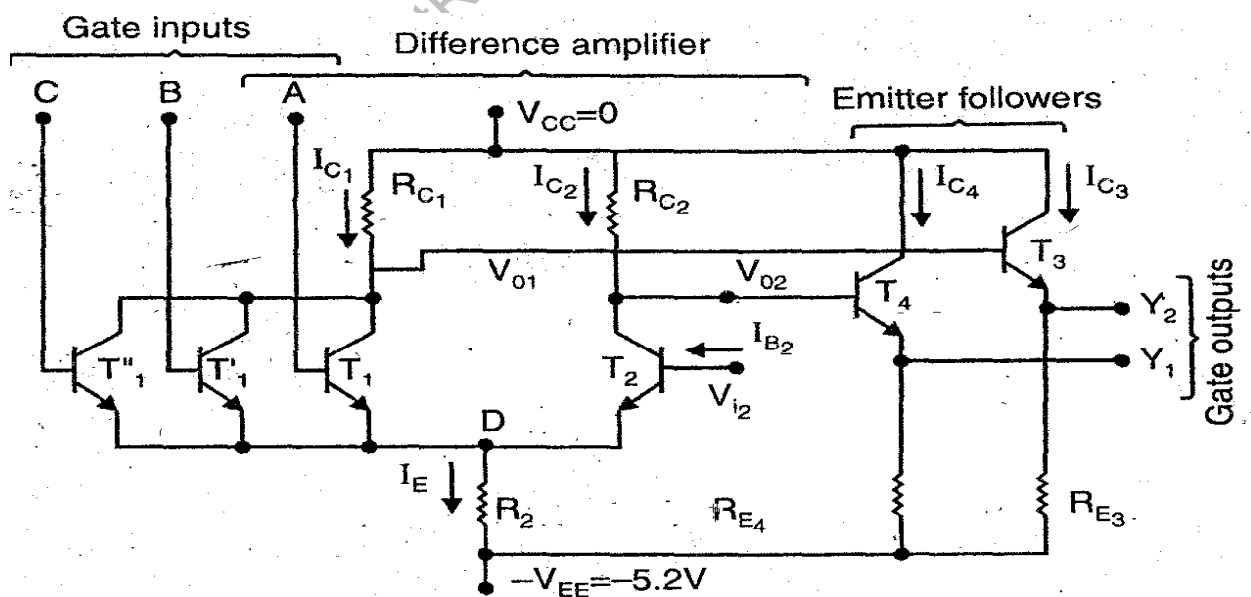
Fig. (A) A 3-input ECL OR/NOR Gate

Pulse & Digital Circuits

Circuit description:

The above diagram contains the inputs as A, B, C through the transistors T_1 , $T_1^{'}$, $T_1^{''}$ of which emitters are coupled and the combination of T_1 , $T_1^{'}$, $T_1^{''}$ and T_2 will acts as differential amplifier. The two collector currents in this configuration are IC1 and I_{C2} respectively. If one current increases another will get decrease. The two transistors T_2 ,T_3 are emitter followers.

Circuit operation:

When A,B,C are low the transistors T_1 , $T_1^{'}$, $T_1^{''}$ will be off and the transistor T_2 will be ON because of T_3 will be ON output of nor gate is HIGH and because of T_4 is OFF output is LOW at or output.

when any one of the inputs high, corresponding transistor is ON and the transistor T_2 will be OFF because of T_3 will be OFF output of nor gate is LOW and because of T_4 is ON output is HIGH at or output.

when all of the inputs high, corresponding transistors T_1 , $T_1^{'}$, $T_1^{''}$ will be ON and the transistor T_2 will be OFF Because of T_3 will be OFF output of nor gate is LOW and because of T_4 is ON output is HIGH at or output.

MOS (metal oxide semiconductor) logic:

This logic uses MOSFETS instead of Bipolar junction Transistors.

Advantages:

 - Easy to fabricate.
 - Inexpensive.
 - Require less power.
 - Less chip area and high fan-out

Pulse & Digital Circuits

NFET and PFET Transistors:

- N channel device: built directly in the P substrate with N-doped source and drain junctions and normally N-doped gate conductor

  ◦ Requires positive voltage applied to gate and drain (with respect to source) for electrons to flow from source to drain (thought of as positive drain current)

- P channel device: built in an N-well (a deep N-type junction diffused into the P substrate) with P-doped source and drain junctions and N or P-doped gate

  ◦ Requires negative voltage applied to gate and drain (with respect to source) for electrons to flow from drain to source (thought of as negative drain current**)**

6.4 CMOS logic family

- **CMOS stands for *Complementary Metal Oxide Semiconductor***

  ◦ **Complementary:** there are N-type and P-type transistors. N-type transistors use electrons as the current carriers. P-type transistors use holes as the current carriers.

  ◦ **Metal:** the gate of the transistor was made of aluminum metal in the early days, but is made of polysilicon today.

  ◦ **Oxide**: silicon dioxide is the material between the gate and the channel

  ◦ **Semiconductor:** the semiconductor material is silicon, a type IV element in the periodic chart. Each silicon atom bonds to four other silicon atoms in a tetrahedral crystal structure.

Pulse & Digital Circuits

Simple CMOS Circuits: *The Inverter Gate*
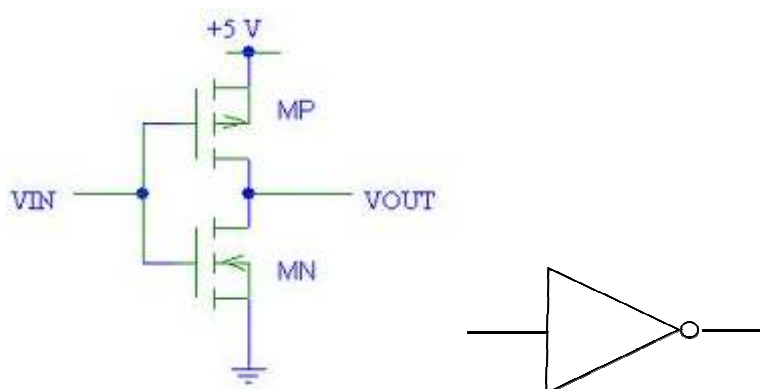
- **The simplest complementary MOS (CMOS) circuit is the inverter:**

  ◦ NFET & PFET gates are connected together as the input

  ◦ NFET & PFET drains are connected together as the output

  ◦ NFET & PFET sources are connected to Gnd and V_{dd}, respectively.

  ◦ NFET substrate is normally connected to Gnd for all NFET devices in the circuit

  ◦ PFET well is normally connected to V_{dd} (most positive voltage in circuit) for all PFET devices

- **Operation:**

  ◦ If V_{in} is down (0 volts), NFET is OFF and PFET is ON pulling V_{out} to V_{dd} (high = 1)

  ◦ If V_{in} is up (at V_{dd}), NFET is ON hard and PFET is OFF pulling V_{out} low to Gnd ("0")

  ◦ With V_{in} at 0 or V_{dd}, no dc current flows in inverter

CMOS Circuits: *2-way NAND*

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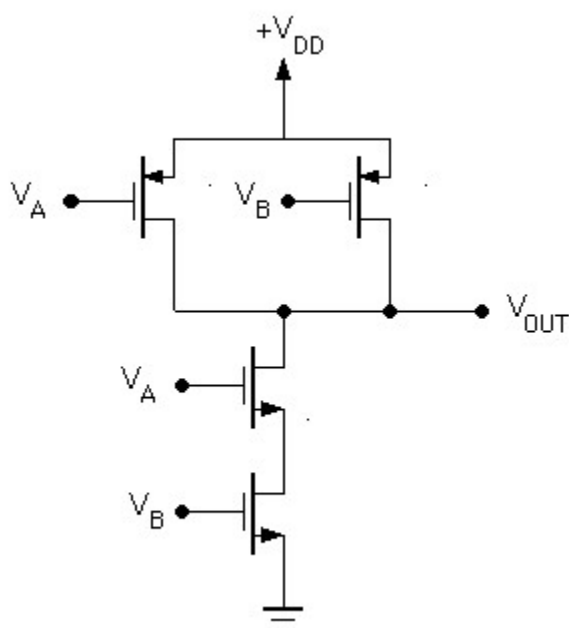
- **Circuit Topology:**

  ◦ T1 and T2 are N-FET devices connected in series; T3 and T4 are P-FET devices connected in parallel with their sources at Vdd and their drains at Vout.

  ◦ Inputs A and B are connected to the gates of T1 & T3 and T2 & T4, respectively.

  ◦ T2, T3, & T4 operate as "grounded source" devices, but T1 has its source generally above Gnd potential.
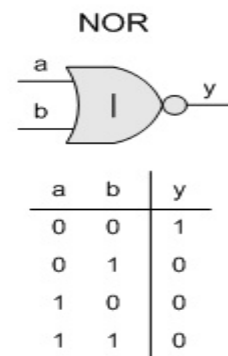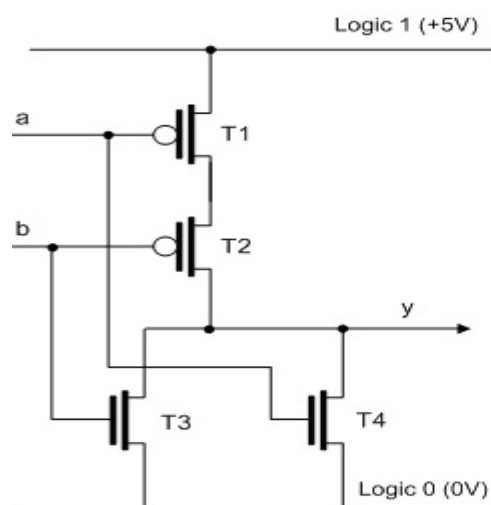
- **Operation:**

  ◦ If both A and B are high (at V_{dd}), both T1 and T2 are ON hard, therefore pulling V_{out} low (to zero volts). Both T3 and T4 are OFF due to their gate-to-source voltages (Vgs) being at 0 volts, thus preventing any dc curren**t.**

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- If either A or B (or both) are low (at 0 volts), either T1 or T2 (or both) are OFF; T3 or T4 (or both) are ON hard, thus pulling Vout high to V_{dd} (a "1" output).

CMOS Circuits: *2-way NOR*

- **Circuit Topology:**

  - T1 and T2 are N-FET devices connected in parallel with their sources at Gnd and drains at V_{out}; T3 and T4 are P-FET devices connected in series.

  - Inputs A and B are connected to the gates of T1 & T3 and T2 & T4, respectively.

  - Operation:

  - If either A or B is high, T1 and/or T2 are ON hard and either T3 or T4 (or both) are OFF, pulling V_{out} to gnd. No dc current flows.

  - If both A and B are low (at gnd), both T1 and T2 are OFF and both T3 and T4 are ON hard, thus pulling V_{out} to V_{dd} (a "1" output).

Pulse & Digital Circuits

- ◦ T1, T2, and T3 operate as common source, but T4's source potential will drop below V_{dd}.
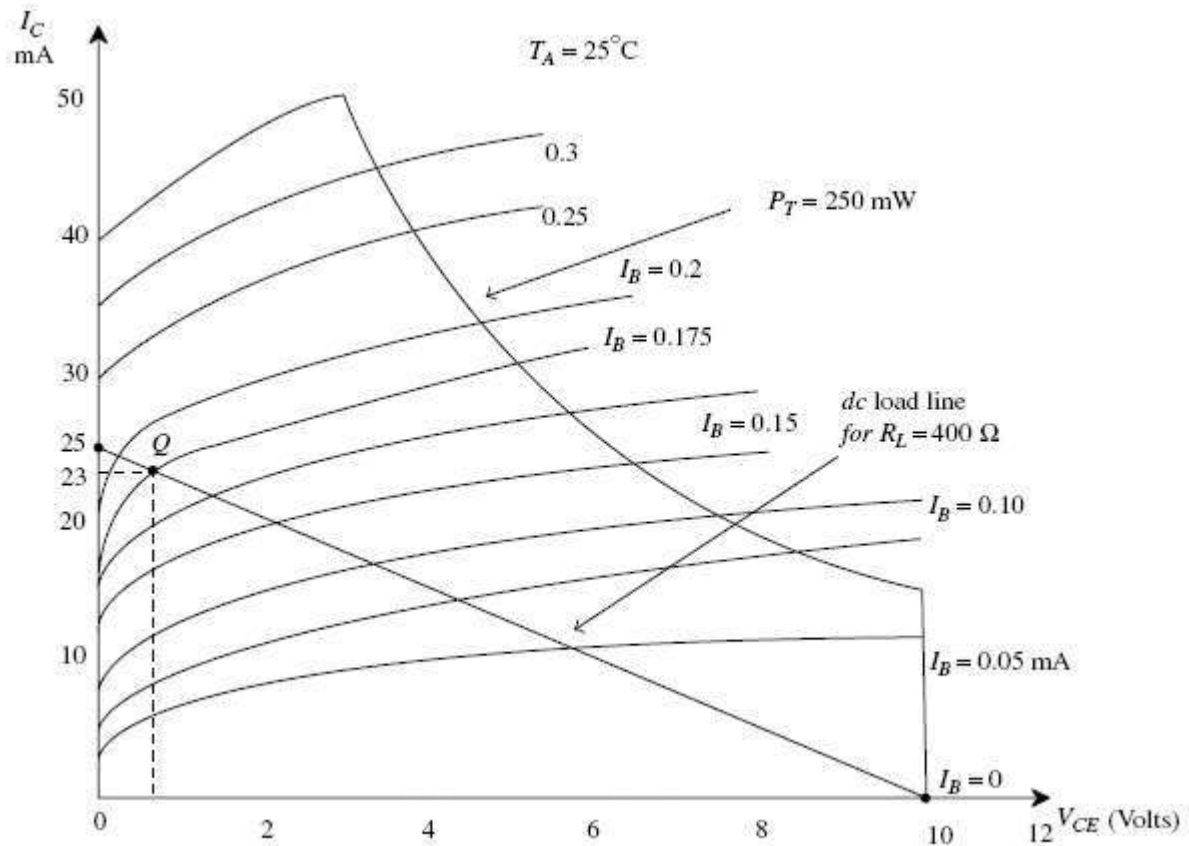
Important Questions:

1. What are two logic levels represented by logic sytem? How they can be represented?

2. Explain how TTL acts as NAND gate?

3. What is a totem pole configuration?

4. Explain how ECL acts as NOR gate?

5. Explain CMOS Inverter circuit?

6. Explain the operation of D-FlipFlop?

Pulse & Digital Circuits

FIGURE 6.36 Typical output characteristics of an n–p–n transistor in the CE mode

UNIT-IV - b

Sampling gates

INTRODUCTION

A sampling gate is a transmission circuit that faithfully transmits an input signal to the output for a finite time duration which is decided by an external signal, called a gating signal (normally rectangular in shape), as shown in Fig. 11.1.

The input appears without a distortion at the output, but is available for a time duration T and afterwards the signal is zero. They can transmit more number of signals. The main applications of

the sampling gates are: (i) multiplexers; (ii) choppers; (iii) D/A converter; (iv) sample and hold circuits, etc. Sampling gates can be of two types:

1. Unidirectional gates: These gates transmit the signals of only one polarity.
2. Bidirectional gates: These gates transmit bidirectional signals (i.e., positive and negative signals).

Earlier, we had seen logic gates in which the output, depending on the input conditions, is either a 1 level or a 0 level. That is, the inputs and outputs are discrete in nature. In a sampling gate, however, the output is a faithful replica of the input. Hence, sampling gates are also called linear gates, transmission gates or time selection circuits. Linear gates can use either a series switch, as shown in Fig. 11.2(a) or a shunt switch, as shown in Fig. 11.2(b). InFig. 11.2(a), only when the switch closes, the input signal is transmitted to the output. In Fig. 11.2(b), only when the switch is open the input is transmitted to the output.
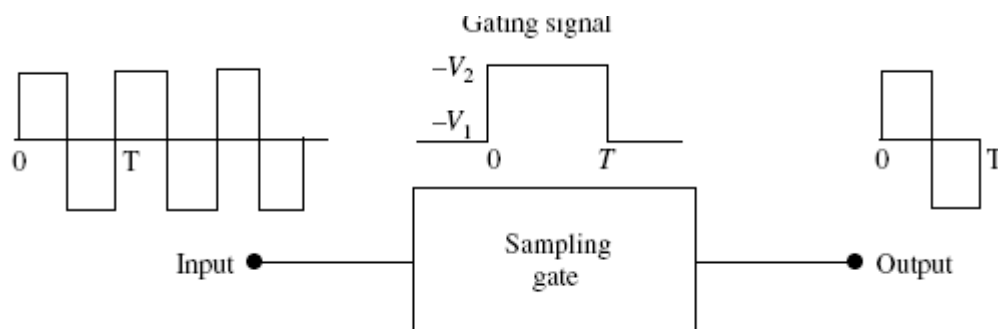
FIGURE 11.1 A sampling gate
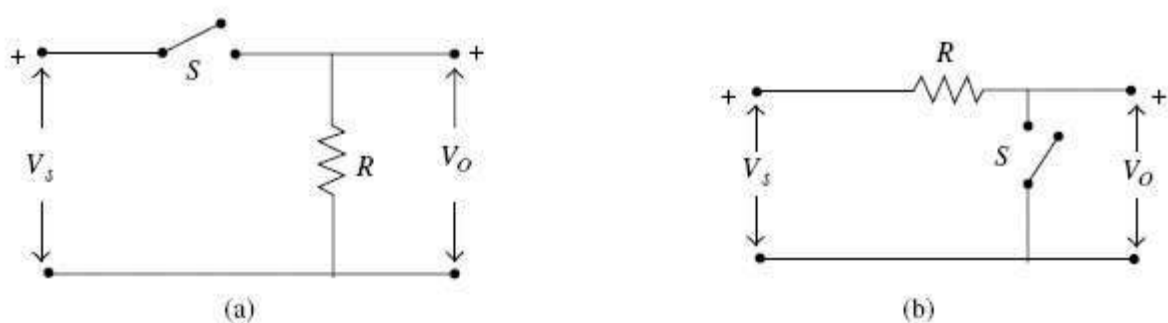
FIGURE 11.2 A linear gate (a) using a series switch; and (b) using a shunt switch

UNIDIRECTIONAL DIODE GATES

A unidirectional gate can transmit either positive or negative pulses (or signals) to the output. It means that this gate transmits pulses of only one polarity to the output. The signal to be

transmitted to the output is the input signal. This input signal is transmitted to the output only when the control signal enables the gate circuit. Therefore, we discuss two types of unidirectional diode gates, namely, unidirectional diode gates that transmit positive pulses and unidirectional diode gates that transmit negative pulses.
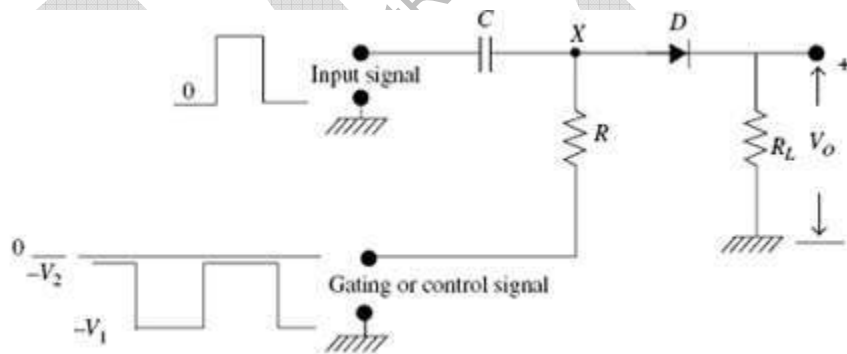
Unidirectional Diode Gates to Transmit Positive Pulses

In order to transmit positive pulses, the unidirectional gate shown in Fig. 11.3 can be used. The gating signal is also known as a control pulse, selector pulse or an enabling pulse. It is a negative signal, whose magnitude changes abruptly between $-V_2$ and $-V_1$.

Consider the instant at which the gating signal is $-V_1$, which is a reasonably large negative voltage. As a result, D is OFF. Even if a positive input pulse is present when the gating signal with value $-V_1$ is present, the diode D remains OFF since the input may not be sufficiently large to forward-bias it. Hence, the output is zero.

Now consider the duration when the gate signal has a value $-V_2$ (smaller negative value) and when the input is also present (coincidence occurs). Assume that the control signal has peak-to-peak swing of 25 V and the signal has peak-to-peak swing of 15 V.

1.   Let, for example, $-V_1 = -40$ V, $-V_2 = -15$ V and the signal amplitude be 15 V, as shown in Fig. 11.4(a). The net voltage at the anode of the diode, when the input is present for the duration of the gating signal, is 0. The diode is OFF and the output in this case is zero.

**FIGURE 11.3** The unidirectional gate to transmit positive pulses
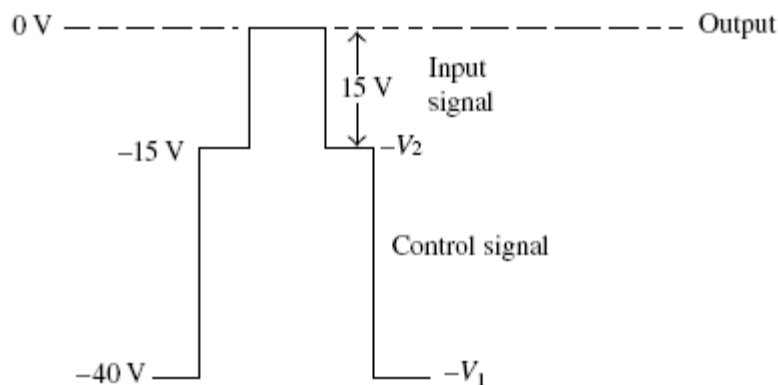
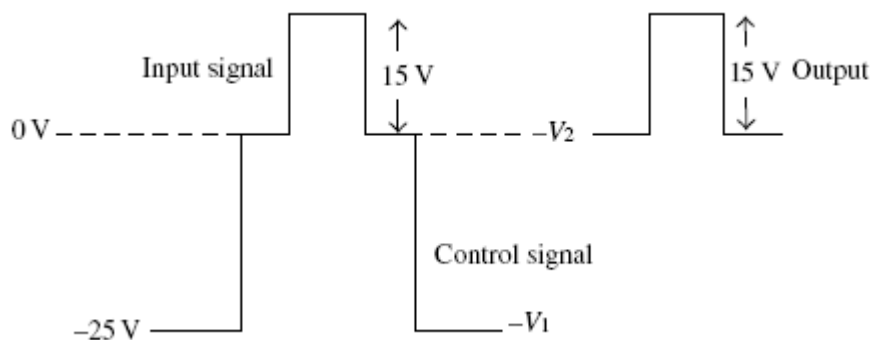**FIGURE 11.4(a)** The control signal with $-V_1 = -40$ V, $-V_2 = -15$ V and the input amplitude 15 V

2.   Now, change the levels to $-V_1 = -35$ V, $-V_2 = -10$ V and the signal amplitude remains constant at 15 V, as shown in Fig. 11.4(b). Only when the input forward-biases the diode, there is an output. The output in this case is a pulse of amplitude 5 V (assuming an ideal diode). The duration of the output is the same as the duration of the input signal.

3.   Now let $-V_1 = -30$ V, $-V_2 = -5$ V and the signal amplitude be 15 V, as shown in Fig. 11.4(c). As the signal above the zero level is 10 V, the output is a pulse of amplitude 10 V and has the same duration as the input.

4.   Let $-V_1 = -25$ V, $-V_2 = 0$ V and the signal amplitude be 15 V, as shown in Fig. 11.4(d). The output in this case is 15 V and has the same duration as the input.

5.   Let $-V_2 = +5$ V and $-V_1 = -20$ V, as shown in Fig. 11.4(e). In this case, the output not only contains the input but also a portion of the control signal. The desired signal at the output is seen to be riding over a pedestal. We see that the output of the gate changes by adjusting $-V_2$ and in the last case it is seen that the output is superimposed on a pedestal of 5 V. Thus, the output is influenced by the control signal.
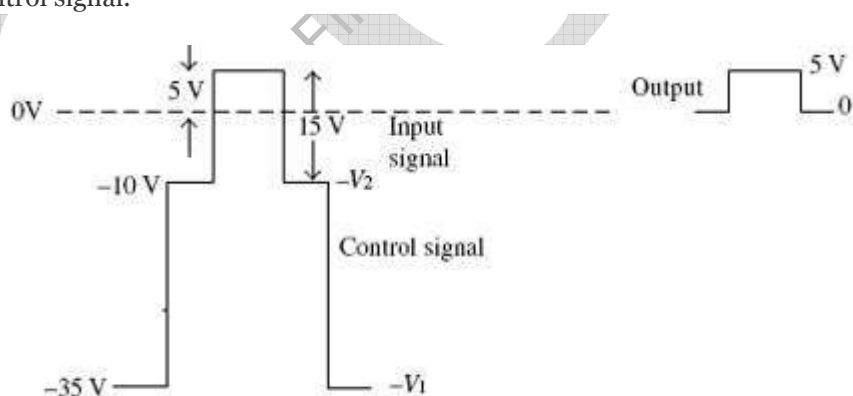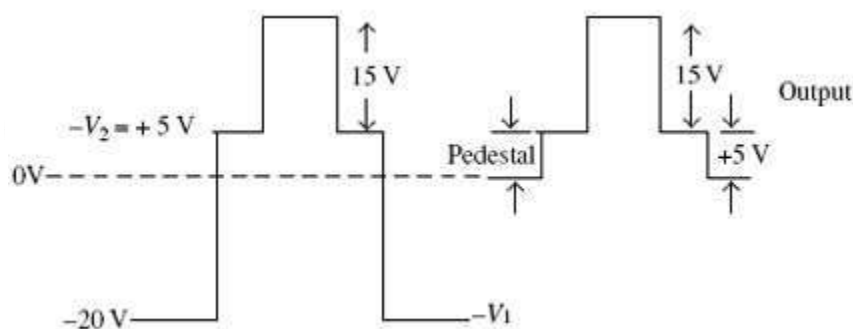

FIGURE 11.4(b) The control signal with $V_1 = -35$ V, $-V_2 = -10$ V and the input amplitude 15 V
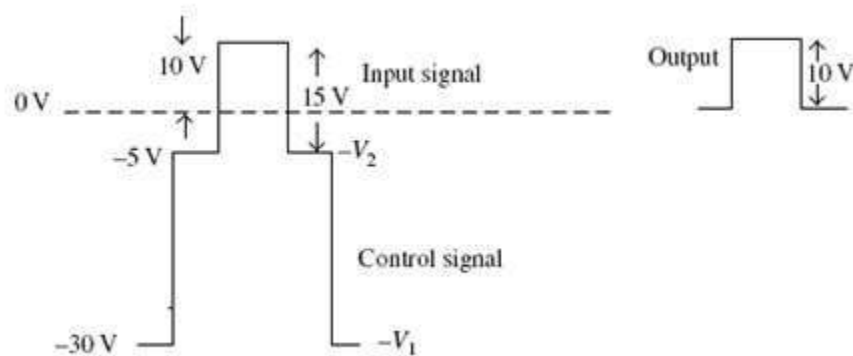
FIGURE 11.4(c) The control signal with $V_1 = -30$ V, $- V_2 = -5$ V and the input amplitude 15 V

FIGURE 11.4(d) The control signal with $V_1 = -25$ V, $- V_2 = 0$ V and the input amplitude 15 V

FIGURE 11.4(e) The control signal with $V_1 = -20$ V, $- V_2 = 5$ V and the input amplitude 15 V

For a gating signal, the RC network behaves as an integrator. Hence, the gate signal is not necessarily a rectangular pulse but rises and falls with a time constant RC. As a result, there is a distortion in the gate signal. However, if the duration of the input signal (a pulse) is much smaller than the duration of the gate, this distortion associated with the gating signal is not necessarily

transmitted to the output; and the output is a sharp pulse as desired, provided the pedestal is eliminated, as shown in Fig. 11.4(f). On the contrary, if there is a pedestal, there is a corresponding distortion in the output, as shown in Fig. 11.4(g).

The advantages of unidirectional diode gates are: (i) they are simple to implement; (ii) have a negligible transmission delay; (iii) the gate draws no current in the quiescent condition; and (iv) by the proper modification of the circuit, more than one input signal can be transmitted through the gate circuit. However, there are two disadvantages of this arrangement. As the control signal and the input signal are directly connected at X (see Fig. 11.3), there could be an interaction between these two sources. The time constant RC, if properly not chosen, can cause the distortion of the gate signal. A two-input unidirectional diode gate is shown in Fig. 11.5(a).
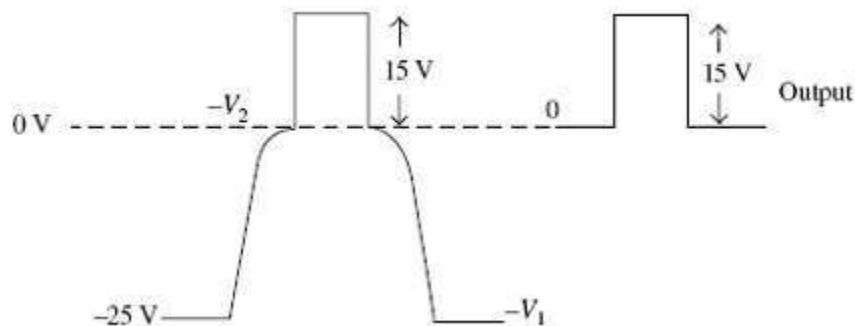
FIGURE 11.4(f) There is no distortion in the output though the control signal is distorted
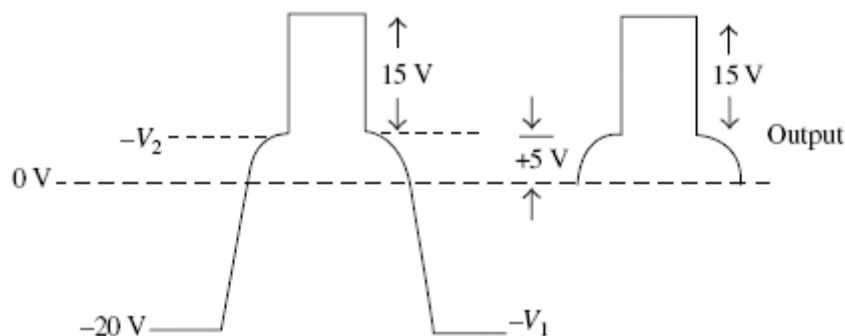

FIGURE 11.4(g) The distorted gate signal giving rise to a distorted pedestal

Let V_{s1} and V_{s2} be the pulses of amplitude 5 V. When both these signals appear at the input simultaneously, having the same duration, the output is shown in Fig. 11.5(b), when $-V_1 = -25$ V and $-V_2 = 0$.

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When the control signal is at $-V_2$ (= 0 V), and if both the inputs are 0 the output is zero. When the inputs are above 0, the output is 5 V. However, when the control input is at $-V_1$(−25 V), no output is available. This negative control signal inhibits the gate. Hence, this circuit is a two-input OR gate with $-V_1$(−25 V) and inhibiting the gate operation. The waveforms shown in Fig. 11.5(b) suggest that time division multiplexing can be employed to simultaneously transmit a number of signals. The limitation of this arrangement is that signal sources may load the control input. To overcome this disadvantage, an arrangement in which the signal sources avoid loading the control input is suggested in Fig. 11.6. Here, the input signals are connected to point X through diodes D_1 and D_2 whereas the control source is connected at X directly to avoid interference and loading.
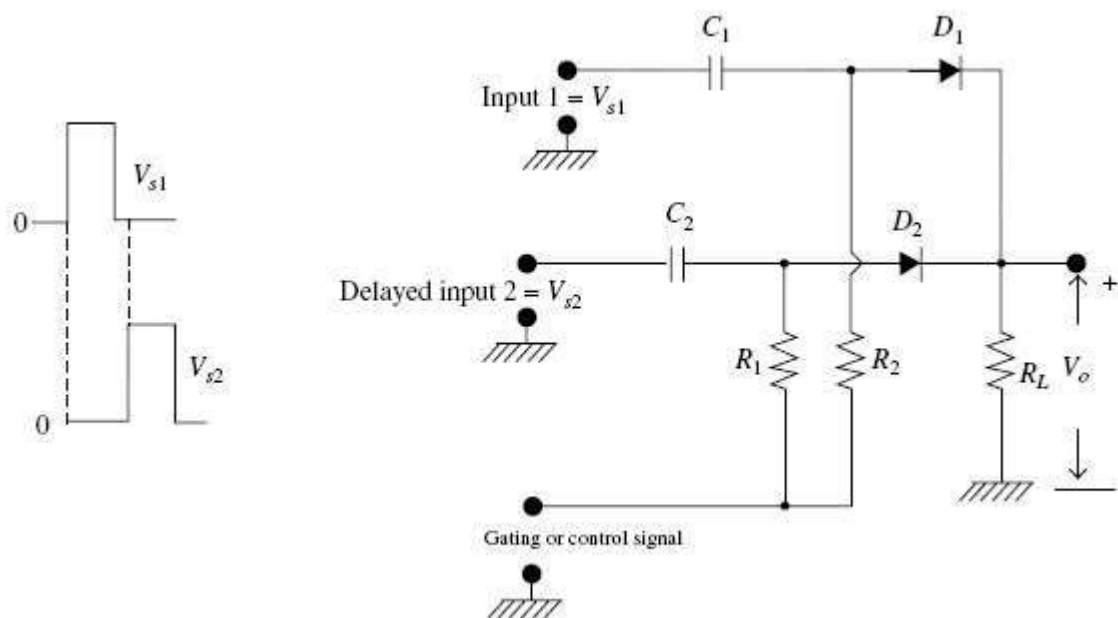
FIGURE 11.5(a) A unidirectional two-input diode gate

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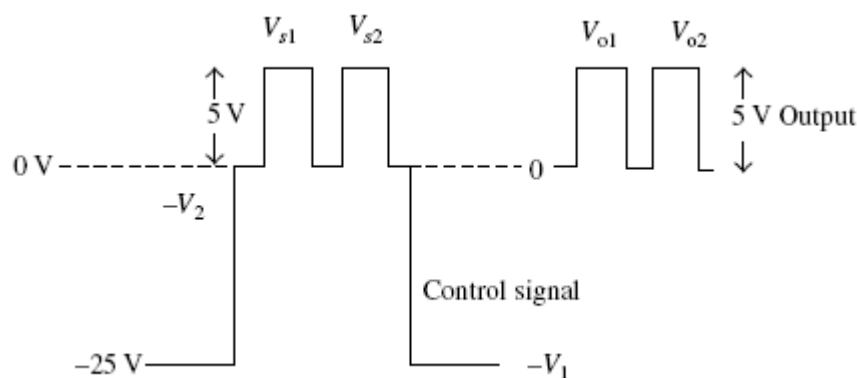
FIGURE 11.5(b) The waveforms of a two-input unidirectional gate
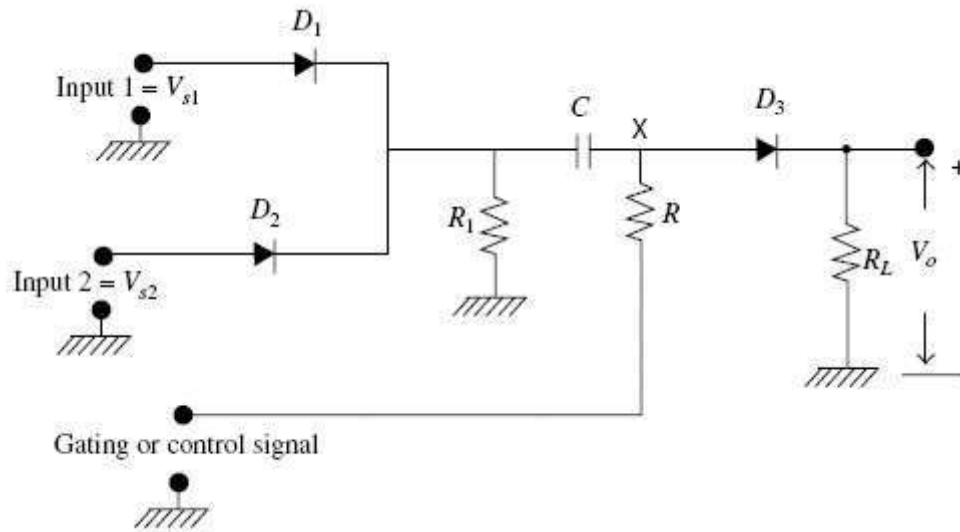
FIGURE 11.6 A two-input diode gate that avoids loading on the control signal

Unidirectional Diode Gates

1.   **A unidirectional diode coincidence gate (AND gate)**: In certain applications, it may become necessary that the input be transmitted to the output only when a set of conditions are simultaneously satisfied. In such cases, a coincidence gate is employed. A unidirectional diode coincidence (AND) gate is shown in Fig. 11.7(a).

When any of the control voltages is at $-V_1(-25\ V)$, point X is at a larger negative voltage, even if the input pulse V_s (15 V) is present. D_o is reverse-biased. Hence, there is no signal at the output.
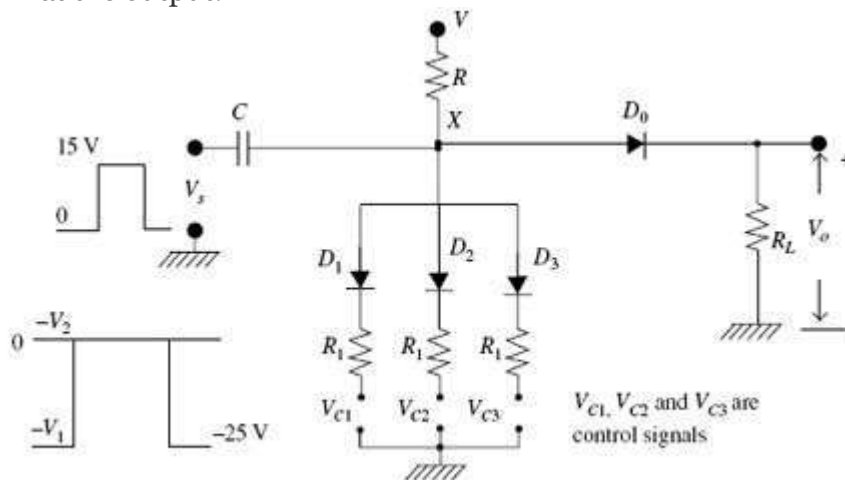
FIGURE 11.7(a) A unidirectional diode AND gate with multiple control signals
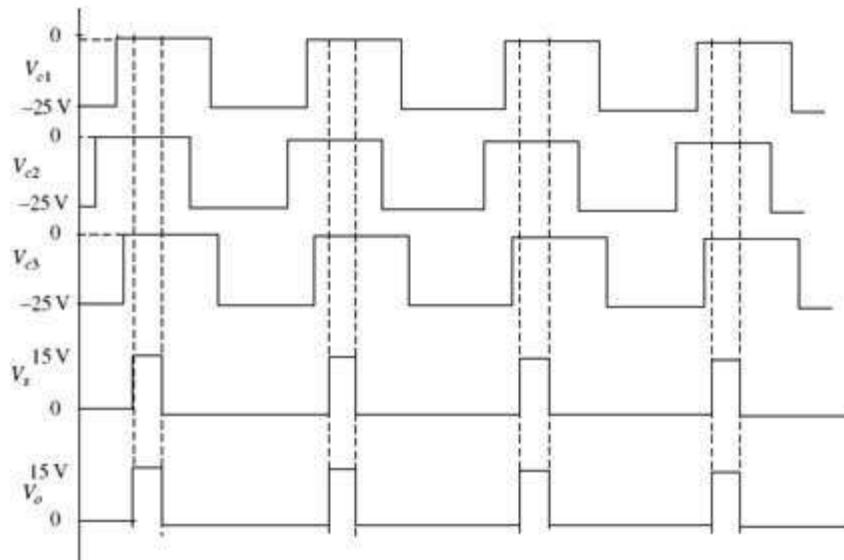
FIGURE 11.7(b) The waveforms of the coincidence (AND) gate

When all the control voltages, on the other hand, are at $-V_2$ (0 V), if an input signal V_s (15 V) is present, D_o is forward-biased and the output is a pulse of 15 V. Thus, only when all the control signals are at 0 V (1 level) and if an input signal is present, then it is transmitted to the output. Hence, this circuit is a coincidence circuit or AND circuit, as shown in Fig. 11.7(b).

2.   **A unidirectional diode OR gate:** Consider the gate circuit shown in Fig. 11.8(a). Let the control voltages vary from -50 V to 0 V. If any control signal V_C (say V_{C1}) is at 0 V, D_1 conducts and behaves as a short circuit. Then the resultant circuit is shown in Fig. 11.8(b). If R_s is 1 kΩ and if I is specified as 1 mA then $R = 149$ kΩ. The voltage at X is now at -1 V.

Hence, D_o is reverse-biased and is an open circuit; and so the output is zero. Now, if a pulse V_s (= 10 V) is applied at the input, D_o is forward-biased and D_1 and D_2 are reverse-biased. The output is 10 V.
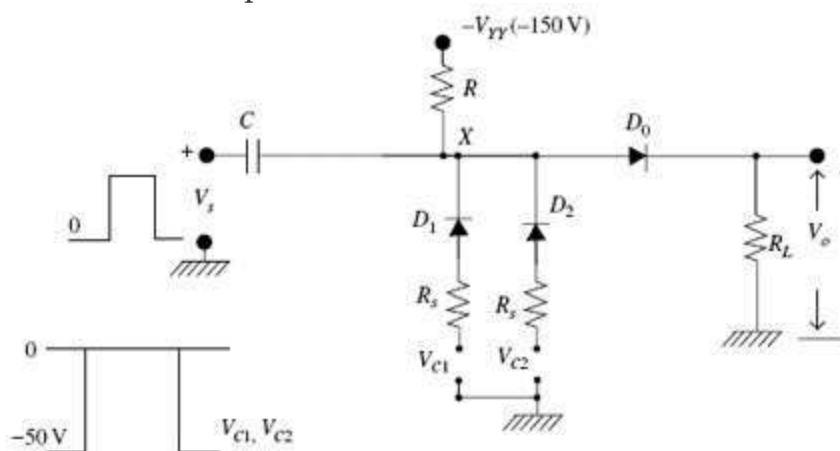
FIGURE 11.8(a) An OR sampling gate

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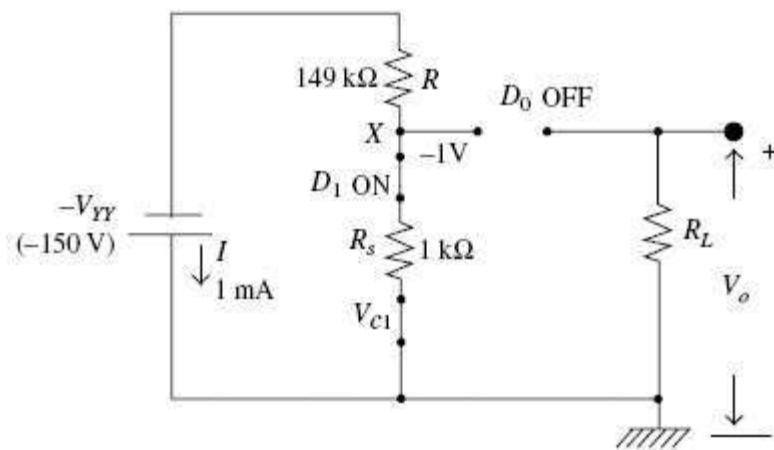
FIGURE 11.8(b) The circuit of Fig. 11.8(a) when any of the control signals and inputs is zero
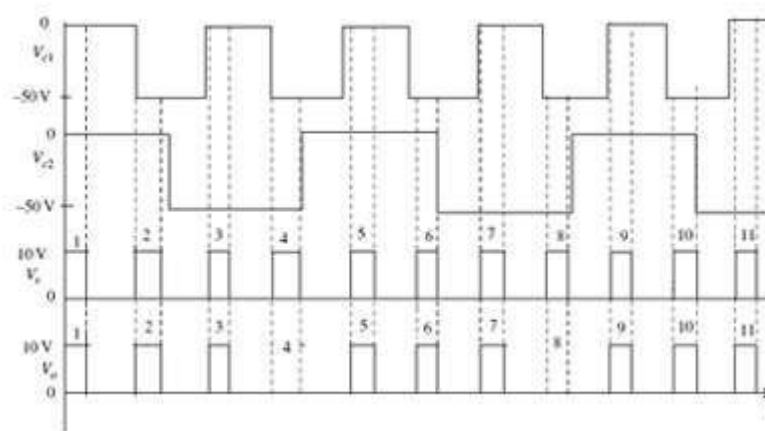
Thus, the circuit shown in Fig. 11.8(a) is a gate that transmits the input signals to the output when any one of the control inputs is 0 V (1 level). This circuit is an OR circuit. The waveforms are shown in Fig. 11.8(c). The truth table, given in Table. 11.1 with control signals as logical inputs, verifies the OR operation. We see from the waveforms shown in Fig. 11.8(c) and Table.11.1 that the output is 0 V (0 level) for input pulses 4 and 8, for which both the control signals are –50 V (0 level).

3. **Unidirectional diode gate that eliminates pedestal**: In the unidirectional gates discussed till now, if the upper level of the gating signal $(-V_2)$ is exactly zero volts, the gate is enabled and an input is faithfully transmitted to the gate output terminals. The output can also be derived if $-V_2$ is a positive voltage (say 5 V). In this case, the output will have a pedestal and the signal is superimposed on it. To ensure that the output is a faithful replica of the input even if the upper level of the control signal is positive (i.e., to eliminate pedestal), the circuit shown in Fig. 11.9(a) is employed.

   1. If the input V_s is zero and if the enabling control signal is not present, D_1 conducts and the negative voltage at X reverse-biases D_0 and $V_o =$ 0, shown in Fig. 11.9(b).

   TABLE 11.1 The truth table of the OR gate with control signals as logical inputs

Input pulse number	State of V_{C1}	State of V_{C2}	Output V_o
1	0 V (1 level)	0 V (1 level)	10 V (1 level)
2	−50 V (0)	0 V (1)	10 V (1)
3	0 V (1)	−50 V (0)	10 V (1)
4	−50 V (0)	−50 V (0)	0 V (0)
5	0 V (1)	0 V (1)	10 V (1)
6	−50 V (0)	0 V (1)	10 V (1)
7	0 V (1)	−50 V (0)	10 V (1)
8	−50 V (0)	−50 V (0)	0 V (0)
9	0 V (1)	0 V (1)	10 V (1)
10	−50 V (0)	0 V (1)	10 V (1)
11	0 V (1)	−50 V (0)	10 V (1)

FIGURE 11.8(c) The waveforms of the OR gate shown in Fig. 11.8(a).
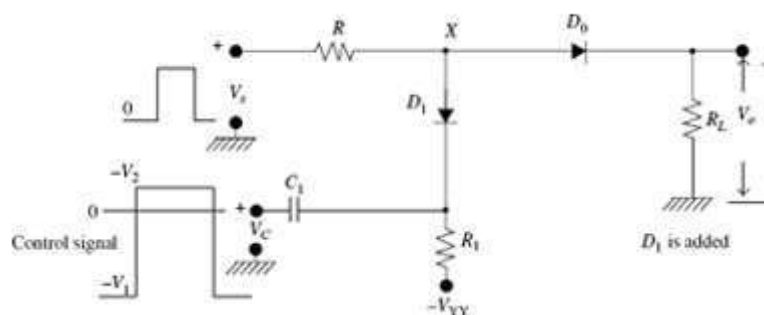
FIGURE 11.9(a) A sampling gate that is insensitive to the upper level ($-V_2$) of the control signal
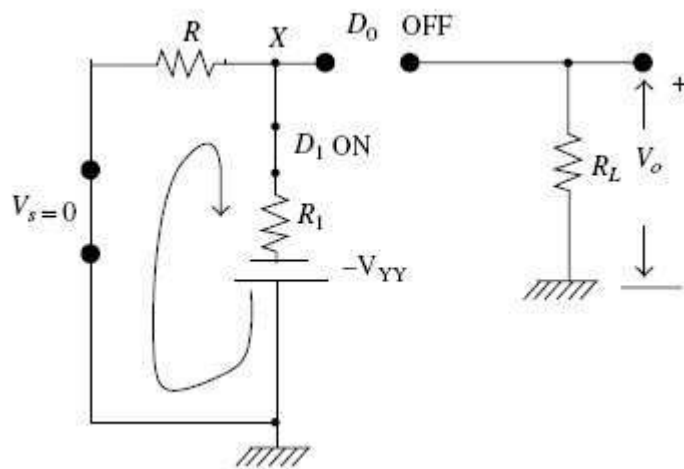
FIGURE 11.9(b) The circuit of <u>Fig. 11.9(a)</u> when $V_s = 0$ and the control signal is absent

FIGURE 11.9(c) The circuit when the control signal is positive and the input is present

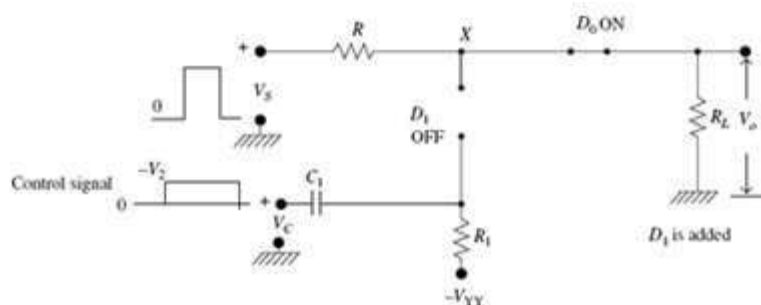2.   If the control voltage is now positive, D_1 is reverse-biased and is OFF, as shown in<u>Fig. 11.9(c)</u>. An input signal V_s (a positive pulse) ensures conduction of D_o and hence, the input signal is present at the output for the duration of the control signal. There is no pedestal in the output even though the control signal has a positive voltage as its upper level.

A Unidirectional Diode Gate to Transmit Negative Pulses

A unidirectional diode gate is shown in <u>Fig. 11.3</u>, to transmit the positive pulses when the gating signal is present. Similarly, a unidirectional diode gate to transmit negative pulses can be constructed as shown in <u>Fig. 11.10</u>. The difference between these two gates is that the input signals are negative pulses and the gating signal varies between V_1 and V_2 as shown in<u>Fig. 11.10</u> and the diode is connected in the opposite direction.

When the gating signal is at V_1, the voltage at X is a large positive voltage as a result D is reverse-biased. If an input signal is now present until the magnitude of the input is more negative than the

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positive voltage at X, the diode will not conduct, i.e., for the diode to conduct and thus transmit the signal to the output, the input is required to have a large negative value. Even if the diode conducts only the peak of the input will be transmitted to the output, but not the entire input signal. On the other hand, when the amplitude of the gating signal is V_2, a small positive voltage, if a negative pulse is present at the input it can make the diode conduct. As such the output is present when the gating signal is at V_2.

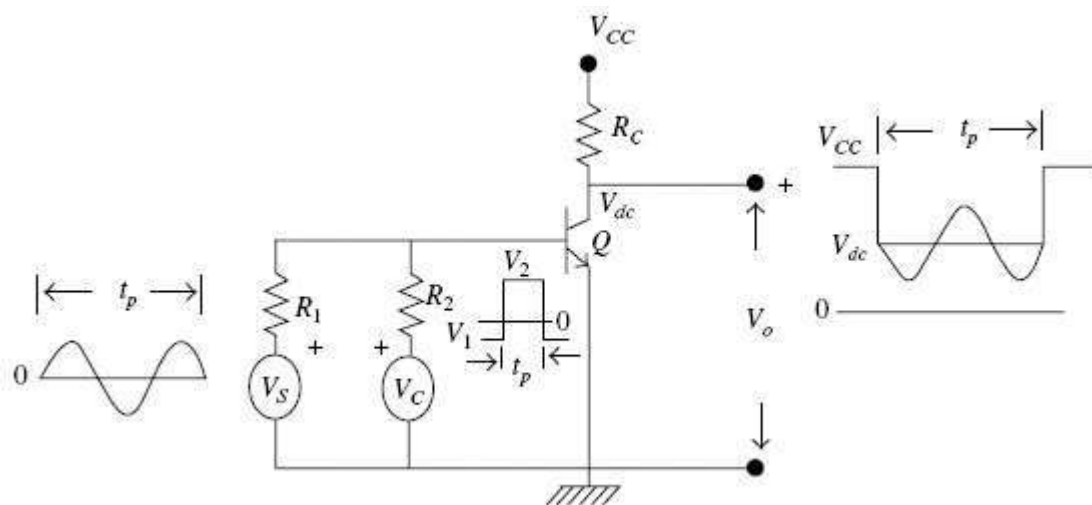<div align="center">BIDIRECTIONAL SAMPLING GATES</div>

Till now we have considered gates that pass only unidirectional signals. Bidirectional sampling gates transmit both positive and negative signals. These gates can be derived using diodes, BJTs, FETs, etc. We are going to consider some variations of the bidirectional gates.
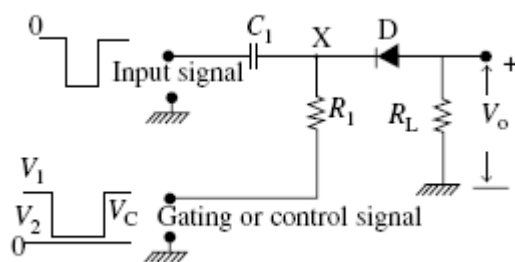
FIGURE 11.10 The unidirectional diode gate to transmit negative pulses

<div align="center">SINGLE-TRANSISTOR BIDIRECTIONAL SAMPLING GATES</div>

A bidirectional sampling gate using a single transistor is shown in Fig. 11.11. The control signal and the input are applied to the base of Q. The control signal is a pulse whose amplitude varies between V_1 and V_2 and has a duration t_p sufficient enough for a signal transmission. As long as V_C is at the lower level V_1, Q is OFF and at the output we only have a dc voltage V_{CC}. However, when V_C is at its upper level V_2, Q is ON for the duration t_p and if the input signal is present during this period, it is amplified and transmitted to the output with phase inversion but referenced to a dc voltage V_{dc}. At the end of t_p, Q is again OFF and the dc voltage at its collector jumps to V_{CC}. Thus, the signal is transmitted when the gating signal is at V_2. However, the output contains a pedestal.
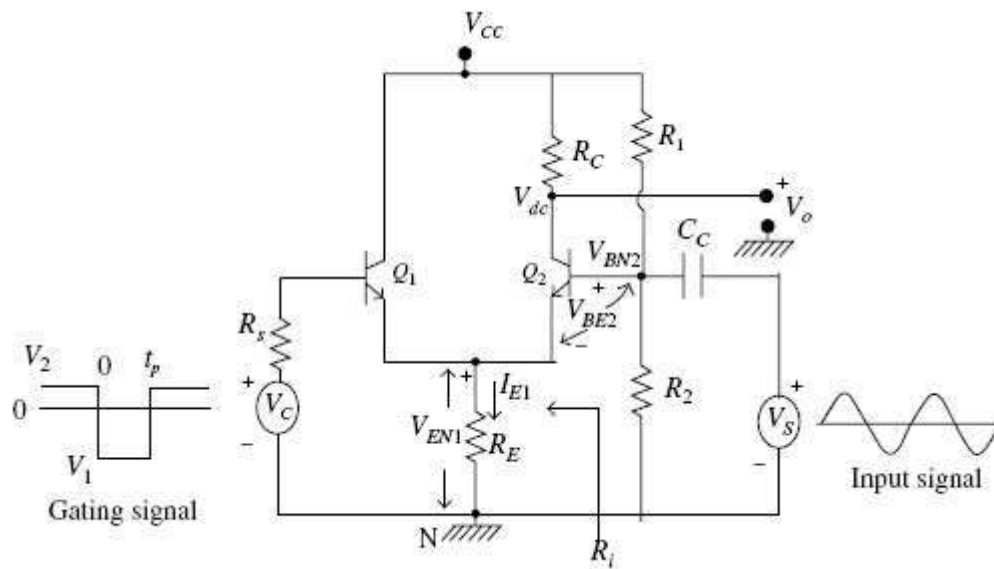
FIGURE 11.11 A bidirectional transistor gate

Two-transistor Bidirectional Sampling Gates

The Fig. 11.12(a) shows another bidirectional transistor gate where two devices Q_1 and Q_2 are used and the control signal and the input signal are connected to the two separate bases.

There is no external dc voltage connected to the base of Q_1, only the gating signal V_C is connected. Let the control voltage be at its upper level, V_2. Then, Q_1 is ON and there is sufficient emitter current I_{E1} which results in V_{EN1} across R_E. Q_2 is biased to operate in the active region using R_1 and R_2. The voltage at the base of Q_2 with respect to its emitter (V_{BE2}) is ($V_{BN2} - V_{EN1}$). If this voltage is sufficient enough to reverse-bias the base emitter diode of Q_2, then Q_2 is OFF. There is no output signal, but only a dc voltage V_{CC} is available. However, when the gating signal is at its lower level V_1, Q_1 is OFF and Q_2 operates in the active region and can also operate as an amplifier. If an input signal is present, there is an amplified output V_o. The presence of R_E increases the input resistance R_i and thus, the signal source is not loaded.

From the waveforms shown in Fig. 11.12(b) it is seen that the output is V_{CC} when Q_2 is OFF. When the gating signal drives Q_1 OFF and Q_2 ON, the dc voltage at the collector of Q_2 falls to V_{dc} (a voltage much smaller than V_{CC}). During the period of the gating signal, the input signal is amplified and phase inverted by Q_2 and is available at the output. Again at the end of the gating signal Q_2 goes OFF and V_o jumps to V_{CC}. Hence, the signal is superimposed on a pedestal.

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FIGURE 11.12(a) A bidirectional transistor gate
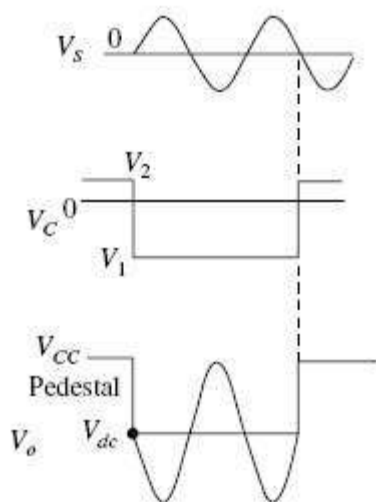
FIGURE 11.12(b) The waveforms

## 11.3.3 A Two-transistor Bidirectional Sampling Gate that Reduces the Pedestal

A circuit arrangement that reduces the pedestal is shown in Fig. 11.13. The control signals applied to the bases of Q_1 and Q_2 may have the same amplitude but are of a opposite polarity. When the gating signal is connected to Q_1 at $T = 0-$, it is negative (at level V_1). The net voltage at the base of Q_1 is $-(V_{BB1} + V_1)$. Therefore, Q_1 is OFF. At the same time the gating signal connected to Q_2 is positive and is   . The net voltage at the base of Q_2 is $(- V_{BB2})$ and is positive and therefore, drives Q_2 ON. Q_2 draws a collector current I_C. As a result, there is a dc voltage V_{dc} at its collector and $V_o = V_{dc}$. However, when the gating voltage at the base of Q_1 drives Q_1 ON and into the active

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region, at t = 0+, Q_2 goes OFF as the gating signal is   . During this period when Q_1 is ON, if the input signal is present, it is amplified and is available at the output, with phase inversion. The bias voltages V_{BB1} and V_{BB2} are adjusted such that the quiescent current in Q_1 and Q_2 when ON is the same (= I_C) and consequently the quiescent dc voltage at the output is V_{dc}. Therefore, the dc reference level practically is V_{dc}. At the end of the time period t_p, Q_1 once again goes into the OFF state and Q_2 into the ON state and the dc voltage at the output is V_{dc}. As such the pedestal can be eliminated. However, our assumption is that the gating signals are ideal pulses (with zero rise time). In this case, the instant Q_1 switches ON, Q_2 switches OFF, as shown in Fig. 11.14(a). However, in practice the gating signals may not be ideal pulses but have a finite rise time and fall time; these may then give rise to spikes in the output shown in Fig. 11.14(b).

Let V_{BE} be the voltage between the base and emitter terminals of a transistor when the device is in the active region. If the gating pulse is at its lower level (, negative), the net voltage as we have seen at the base of Q_2 is far below the cut-off. As a result, Q_2 goes OFF at $t = t_2$. At the same instant, Q_1 is required to go into the ON state, as the gating signal at its base is positive. However, because of the finite rise time associated with the gating signal at the base of Q_1, it may not necessarily go into the ON state at the instant Q_2 has gone into the OFF state(t_2) and may go into the ON state at $t = t_1$. The result is that the output is nearly V_{CC} during the interval t_2 to t_1. This voltage, however, falls to V_{dc} when eventually Q_1 is ON. A spike is developed at the output. Similarly, at the end of the gating signal Q_1 goes OFF (at $t = t_4$) before Q_2 goes ON (at $t = t_3$). Another spike develops at the output. It is seen that the gating signals themselves give rise to spikes in the output. If the rise time of the gating signal is large, these spikes are of larger duration as shown in Fig. 11.14(b), where as if the rise time of the gating signal is small, these output spikes are of smaller duration as shown in Fig. 11.15. If the rise time of the gating signal is small when compared to the duration of the gating signal, even though the spikes may occur in the output, as the duration of the signal is smaller than the spacing between the spikes, these spikes will not cause any distortion of the signal and hence, are not objectionable, as shown in Fig. 11.15.

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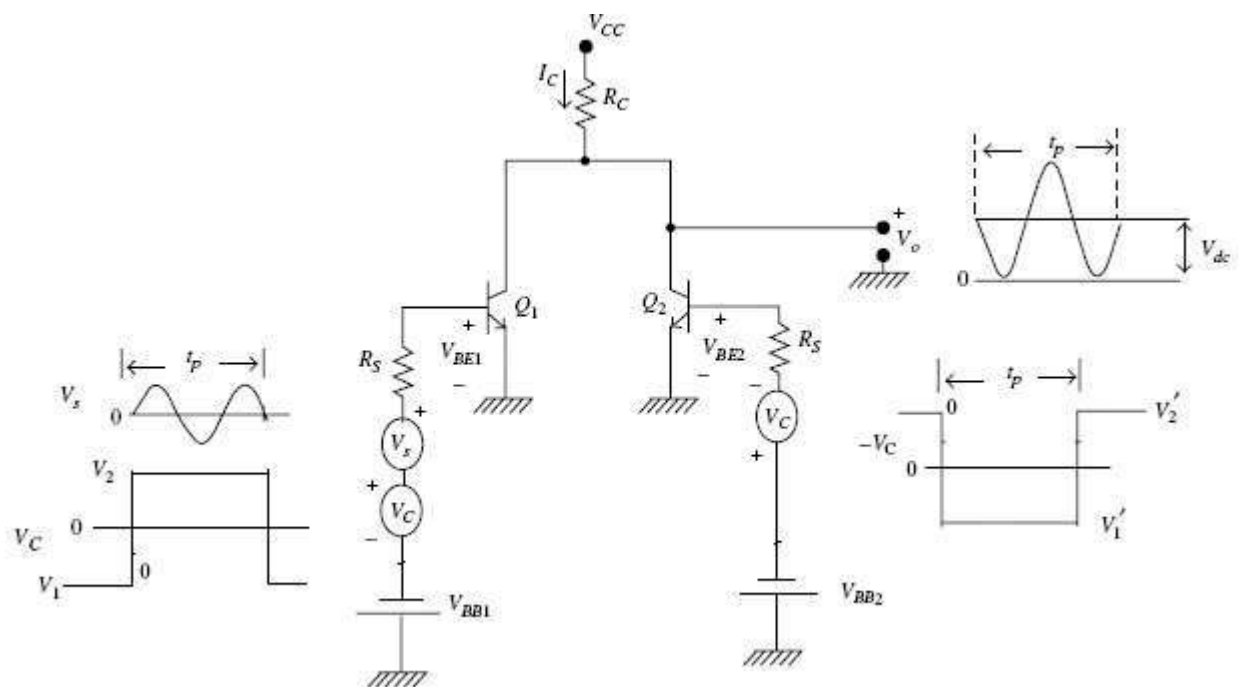
FIGURE 11.13 Circuit that reduces the pedestal
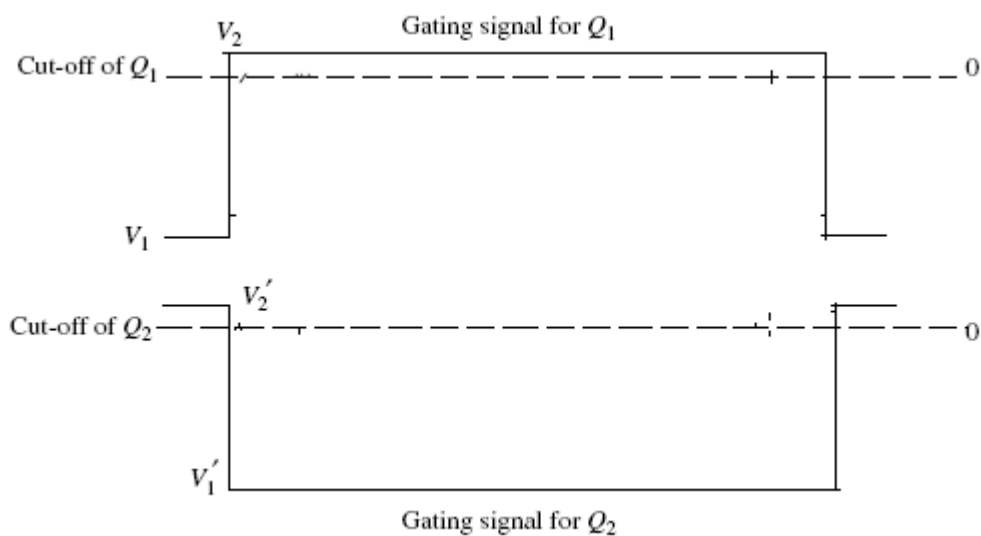
FIGURE 11.14(a) There are no spikes in the output when the gating signals are ideal
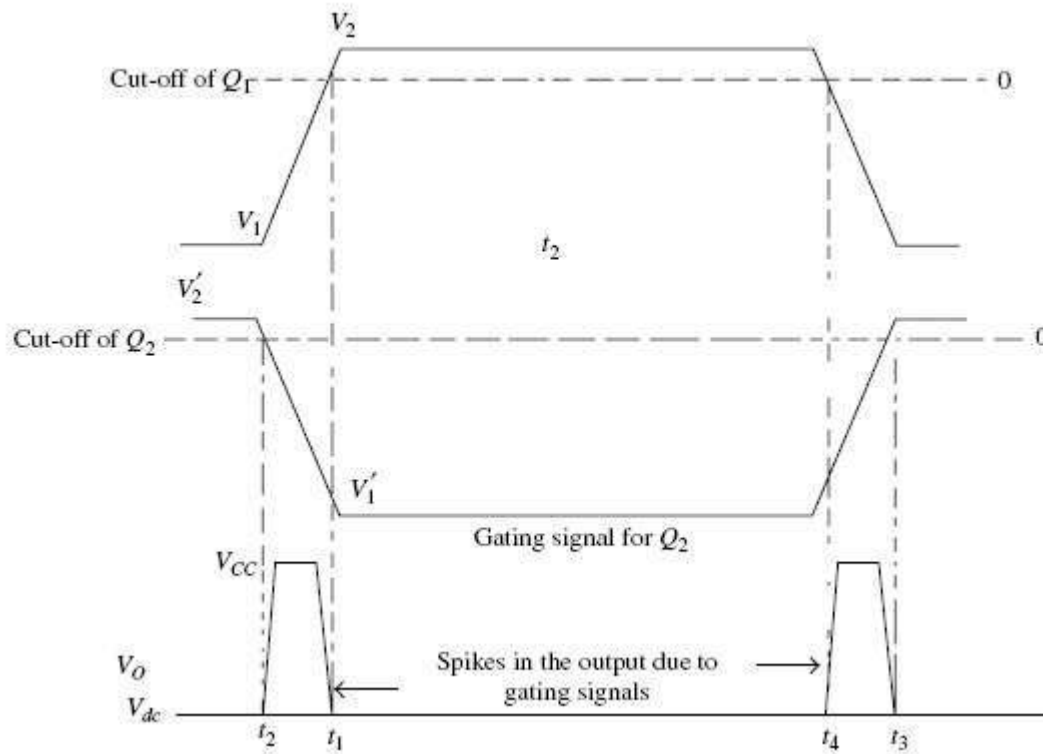
FIGURE 11.14(b) The spikes of a longer duration if the rise time of the gating signal is large

### A Two-diode Bridge Type Bidirectional Sampling Gate that Eliminates the Pedestal

A bidirectional diode gate that eliminates the pedestal is shown in Fig. 11.16(a). R_1, R_1, D_1 and D_2 form the four arms of the bridge. When the control signals are at V_1, D_1 and D_2 are OFF and no input signal is transmitted to the output. However, when the control signals are at V_2, diode D_1 conducts if the input (= V_s) are positive pulses and diode D_2 conducts if the input are negative pulses. Hence, these bidirectional inputs are transmitted to the output. This arrangement because of the circuit symmetry eliminates a pedestal. Consider one half of the circuit that transmits the positive pulses to the output when D_1 conducts (because of symmetry), as shown in Fig. 11.16(b).

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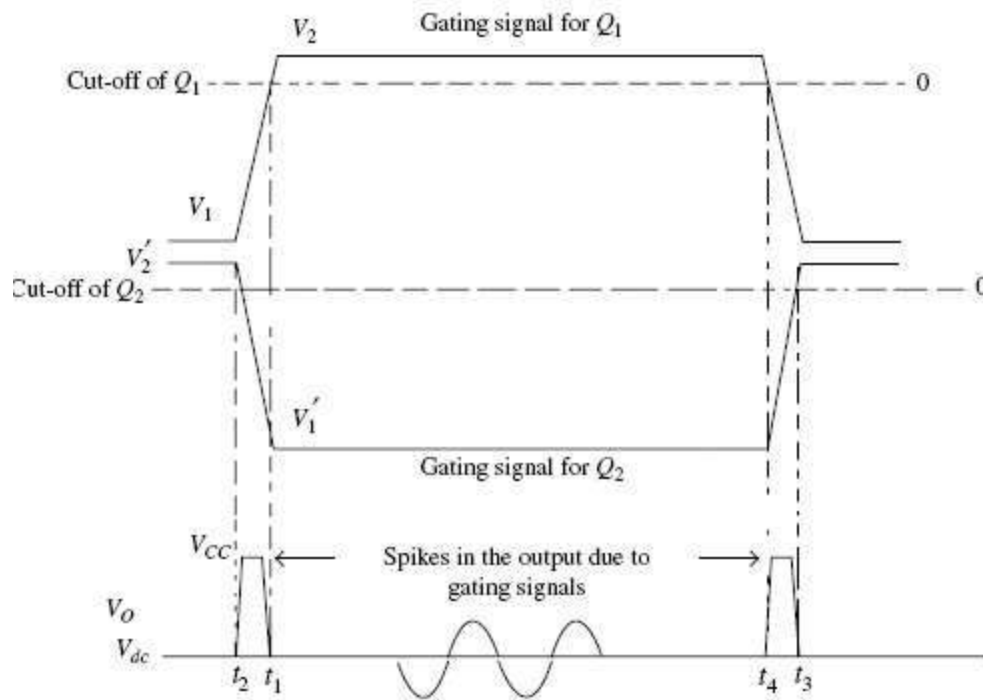
**FIGURE 11.15** The spikes of relatively smaller duration when the rise time of the gating signals is small

Thévinizing the circuit shown in Fig. 11.16(b) at node A, the Thévenin voltage source magnitude due to V_s (shorting V_C source, considering one source at a time) and its internal resistance are calculated using the circuit shown in Fig. 11.16(c).
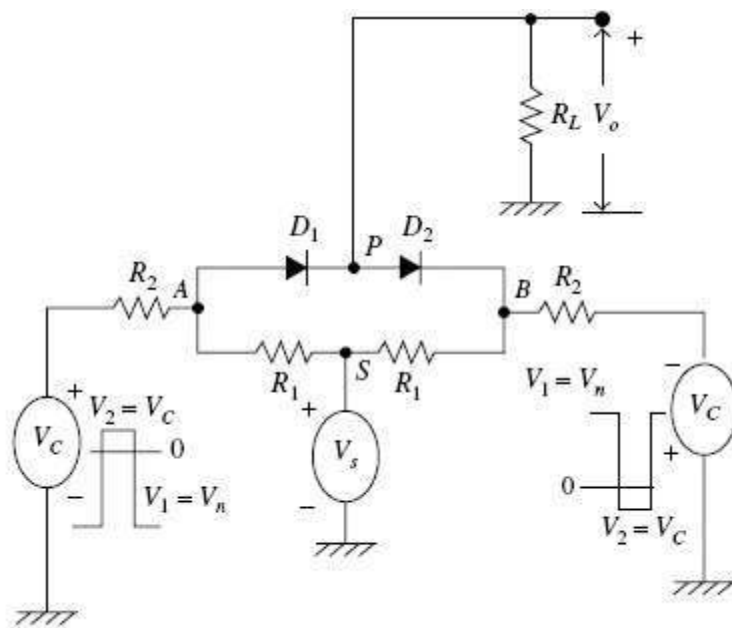
FIGURE 11.16(a) A bidirectional gate in the form of a bridge circuit

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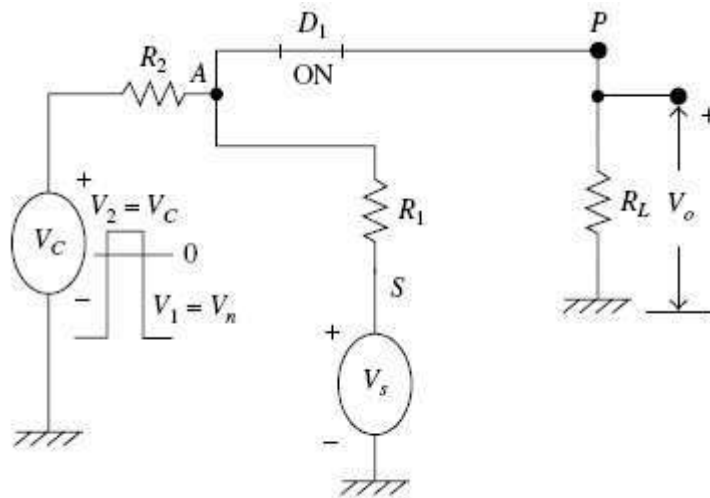
FIGURE 11.16(b) The circuit that transmits the positive pulses to the output
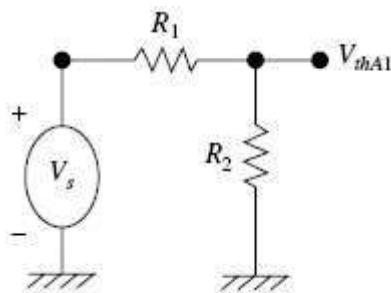
FIGURE 11.16(c) The equivalent circuit to calculate voltage at node A due to V_s source
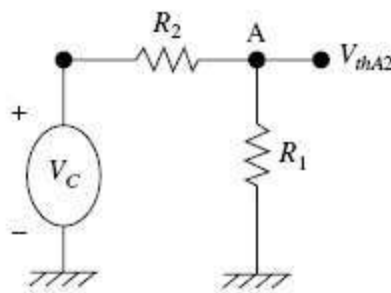
FIGURE 11.16(d) The equivalent circuit to calculate voltage at node A due V_C source

$$V_{thA1} = \frac{R_2}{R_1 + R_2} V_s \qquad = \alpha V_s$$

where $\alpha = \dfrac{R_2}{R_1 + R_2}$ and $R_{th1} = R_1 \,\|\, R_2 = \dfrac{R_1 R_2}{R_1 + R_2}$

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Similarly, Thevenizing the circuit shown in Fig. 11.16(b) at node A, the Thévenin source due to V_C is (shorting V_s), shown in Fig. 11.16(d).

$$V_{thA2} = \frac{R_1}{R_1 + R_2}V_C \quad R_{th2} = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

$$V_{thA2} = \frac{R_1}{R_1 + R_2}V_C = (1 - \frac{R_2}{R_1 + R_2})V_C = (1 - \alpha)V_C$$

We have $R_{th1} = R_{th2}$.

Redrawing the circuit shown in Fig. 11.16(b) and replacing the diode by its linear model (a battery of value V_y in series with R_f, the forward resistance of the diode), results in the circuit shown in Fig. 11.16(e).

Similarly, considering the circuit when a negative signal is transmitted to the output when D_2 is ON and combining the equivalent circuits of the two halves, we finally have the circuit shown in Fig. 11.16(f).

$$R_3 = R + R_f, \text{ where } R = R_{th1} = R_{th2}$$
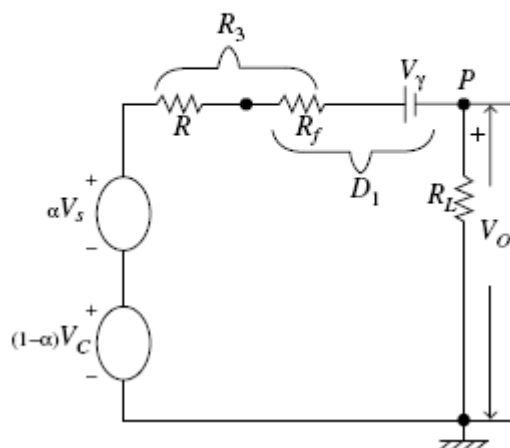
FIGURE 11.16(e) The equivalent circuit of the circuit shown in Fig. 11.16(b)
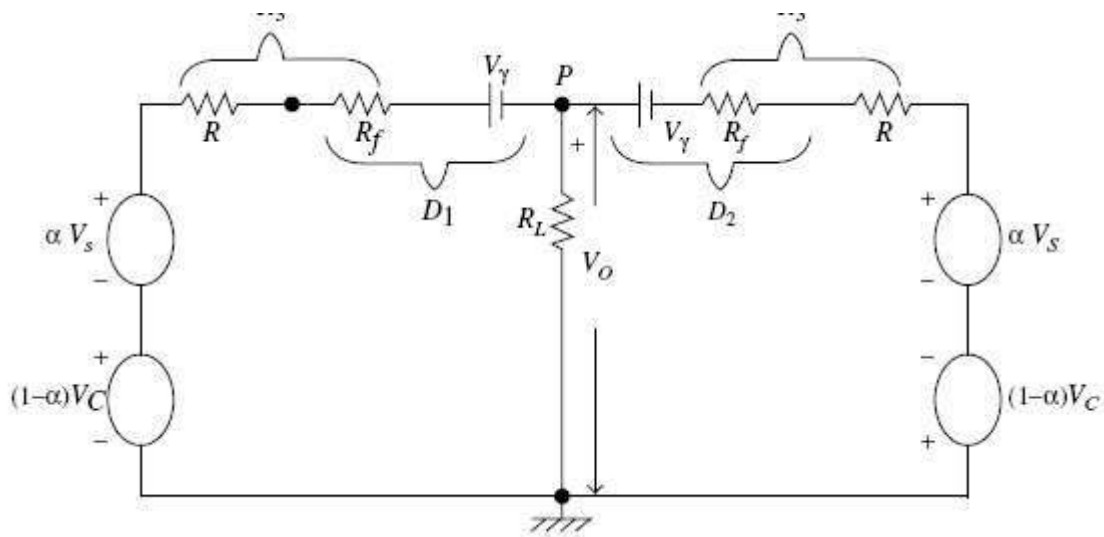
R_f is the diode forward resistance
V_y is its cut-in voltage

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We shall now define the gain of the transmission gate A (strictly speaking this is attenuation) as the ratio of V_o/V_s during transmission period. The control and small diode voltages do not contribute to any current in R_L, the resultant simplified circuit is shown in <u>Fig. 11.16(g)</u>. The open circuit voltage between P and the ground is αV_s and the Thévenin resistance is $R_3/2$, as shown in <u>Fig. 11.16(h)</u>.

$$V_o = \alpha V_s \frac{R_L}{R_L + \dfrac{R_3}{2}} \qquad A = \frac{V_o}{V_s} = \alpha \frac{R_L}{R_L + \dfrac{R_3}{2}}$$
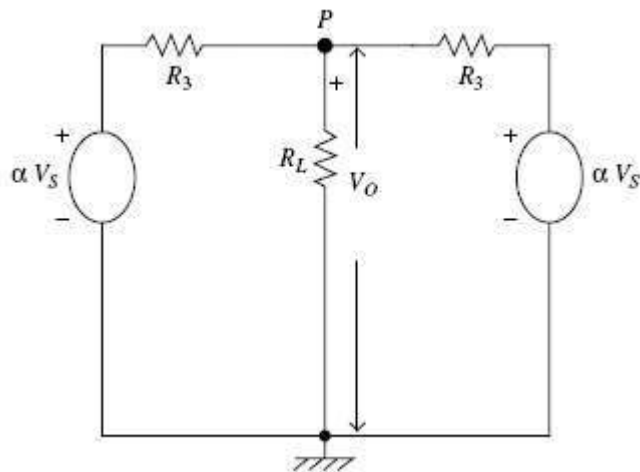
But

$$\alpha = \frac{R_2}{R_1 + R_2}$$

FIGURE 11.16(f) The equivalent circuit of <u>Fig. 11.16(a)</u>
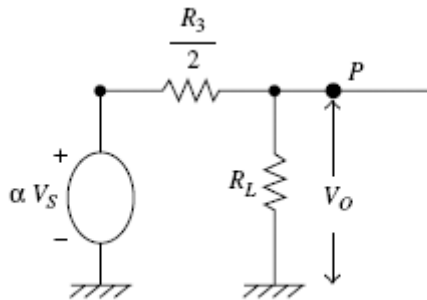
R_f is the diode forward resistance
V_γ is its cut-in voltage

FIGURE 11.16(g) The simplified circuit of <u>Fig. 11.16(f)</u>

FIGURE 11.16(h) The circuit that enables the calculation of gain A

Therefore,

$$A = \frac{R_2}{R_1 + R_2} \times \frac{R_L}{R_L + \dfrac{R_3}{2}} \qquad (11.1)$$

a) Minimum control voltage V_C(min) required to keep both the diodes D_1 and D_2 ON: Let only the gating signals be present. The amplitude and polarity of the gating signals are such that both the diodes D_1 and D_2 conduct, and equal currents flow in these two diodes. When these equal and opposite currents flow in R_L, the net voltage drop is zero and there is no pedestal.

Let V_s be a positive signal. As the amplitude of the signal goes on increasing, the current in D_1 goes on increasing and that in D_2 goes on decreasing. As V_s increases further, the current in D_2 becomes zero (i.e., D_2 is OFF). Thus, there is a minimum control voltage V_C that will keep both the diodes

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ON. To calculate this $V_{C(min)}$, let it be assumed that D_2 has just stopped conducting i.e., the diode current has become zero; the drop across R_3 is zero. Therefore, the output voltage across R_L is the open circuit voltage, as shown in Fig. 11.17(a).
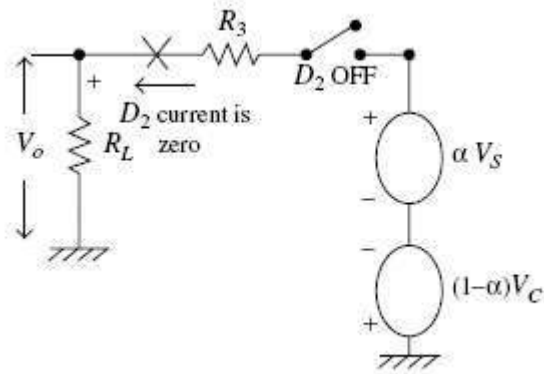
FIGURE 11.17(a) The voltage V_o when D_2 is OFF
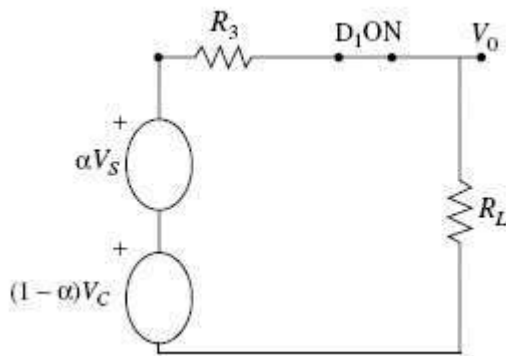
FIGURE 11.17(b) The voltage V_o when D_1 is ON

Now, calculating the output due to the left hand side signal source V_s and control signal $(1-\alpha)V_C$, with the assumption that $V_\gamma \ll V_s$ (i.e., $V_r \approx 0$), as shown Fig. 11.17(b).

$$V_o = [\alpha V_s + (1-\alpha)V_C]\frac{R_L}{R_L + R_3} \qquad (11.3)$$

Eqs. (11.2) and (11.3) represent V_o hence,

$$[\alpha V_s + (1 - \alpha)V_C]\frac{R_L}{R_L + R_3} = \alpha V_s - (1 - \alpha)V_C$$

$$\alpha V_s\left(1 - \frac{R_L}{R_L + R_3}\right) = (1 - \alpha)V_C\left(\frac{R_L}{R_L + R_3} + 1\right) \qquad \alpha V_s\left(\frac{R_3}{R_L + R_3}\right) = (1 - \alpha)V_C\left(\frac{R_3 + 2R_L}{R_L + R_3}\right)$$

$$\alpha V_s R_3 = (1 - \alpha)V_C(R_3 + 2R_L)$$

$$\alpha = \frac{R_2}{R_1 + R_2} \text{ and } 1 - \alpha = 1 - \frac{R_2}{R_1 + R_2} = \frac{R_1}{R_1 + R_2}$$

$$\frac{R_2 R_3}{R_1 + R_2}V_s = \frac{R_1}{R_1 + R_2}(R_3 + 2R_L)V_C$$

$$V_{C(\min)} = \frac{R_2}{R_1} \times \frac{R_3}{R_3 + 2R_L}V_s \qquad\qquad (11.4)$$

$V_{C(\min)}$ decreases with increasing R_L.

b) **Minimum control voltage $V_n(\min)$ to ensure that D_1 and D_2 are reverse-biased:** We have calculated the minimum control voltage $V_{C(\min)}$ i.e., needed to keep both the diodes, D_1 and D_2 ON. Similarly we calculate the minimum control voltage $V_{n(\min)}$ i.e., required to keep D_1 and D_2 OFF when no transmission takes place. If both the diodes are reverse-biased, the output voltage at point P is zero and P is at the ground potential, shown in <u>Fig. 11.18(a)</u>. As D_1 is reverse-biased, it behaves as an open circuit. As a result, the input appears at the output.
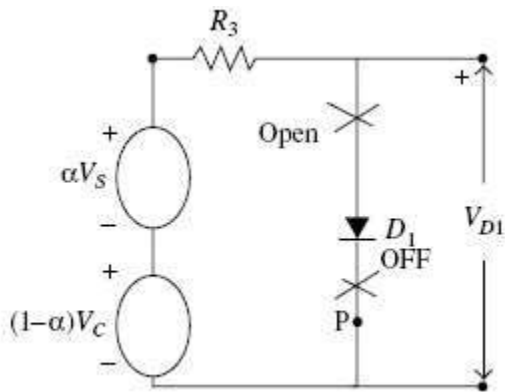
FIGURE 11.18(a) The gate circuit when D_1 and D_2 are reverse-biased
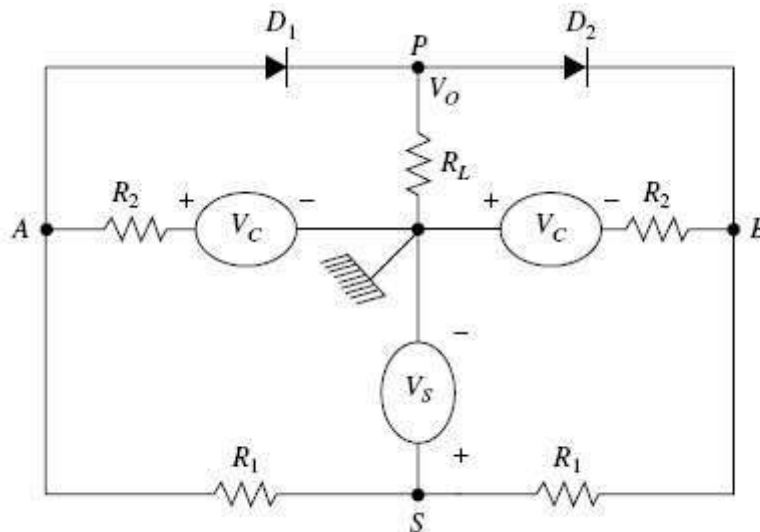
FIGURE 11.19(a) The bidirectional gate redrawn in the form of a bridge

V_{D1} = Voltage across D_1 = $[\alpha V_s + (1 - \alpha)V_C]$

If V_n is the magnitude of V_C at the lower level,

$V_{D1} = [\alpha V_s + (1 - \alpha)V_n]$

For D_1 to be OFF, V_{D1} must be either zero or negative. If V_{D1} is zero,

$$[\alpha V_s + (1 - \alpha)V_n] = 0 \qquad V_n = V_{n(\min)} = \frac{-\alpha V_s}{1 - \alpha} \qquad \frac{\alpha}{1 - \alpha} = \frac{R_2}{R_1}$$

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Therefore,

$$V_{n(min)} = \frac{-R_2}{R_1} V_s \qquad (11.5)$$

In practice $V_{C(min)}$ and $V_{n(min)}$ are larger by 25 per cent. The bidirectional diode gate shown in Fig. 11.16(a) is redrawn as shown in Fig. 11.19(a). If the two control voltages are equal in magnitude but opposite in polarity the pedestal is not present in the output.

c) **Input resistance**: The purpose of the control signal is to enable the gate and the current drawn from the signal source does not depend on the control voltage. This current depends on the state of the diodes, whether they are ON or OFF. Here we assume that D_1 and D_2 as ideal diodes.

When the diodes D_1 and D_2 are OFF from Fig. 11.19(a) the equivalent circuit is as shown in Fig. 11.19(b) (obtained by open circuiting the diodes D_1 and D_2 and short circuiting V_C sources). The input resistance is calculated using the circuit shown in Fig. 11.19(b).

(i) When D_1 and D_2 are OFF

$$R_i = (R_1 + R_2)||(R_1 + R_2) \qquad (11.6)$$

$$R_i = \frac{(R_1 + R_2)}{2}$$
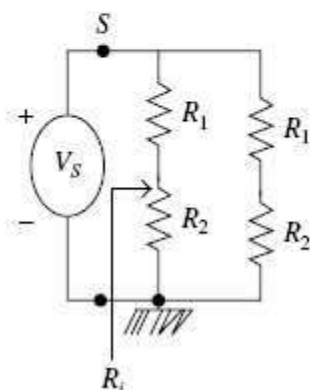
FIGURE 11.19(b) The circuit of Fig. 11.19(a) when D_1 and D_2 are OFF
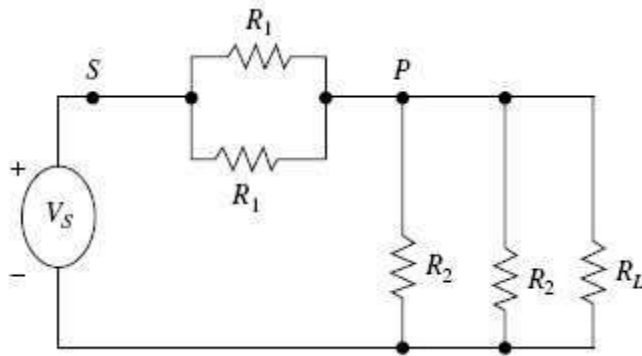
FIGURE 11.19(c) The circuit of Fig. 11.19(a) when D_1 and D_2 are ON
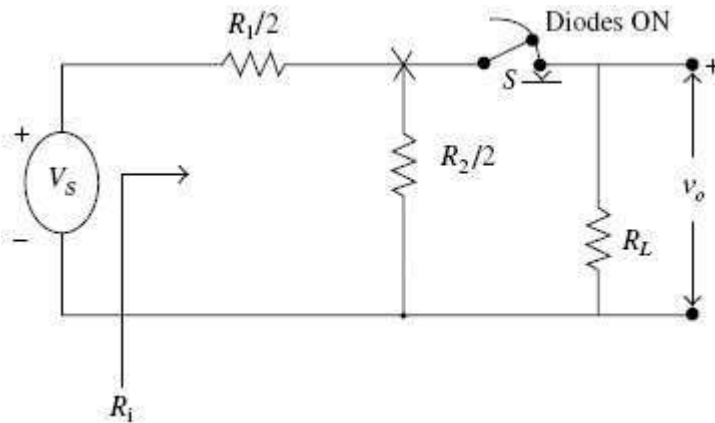
FIGURE 11.19(d) The simplified circuit of Fig. 11.19(c)

When the diodes are ON, the equivalent circuit is as shown in Fig. 11.19(c). The circuit of Fig. 11.19(c) after simplification is redrawn as shown in Fig. 11.19(d).

From the circuit in Fig. 11.19(d), input resistance R_i when the diodes are conducting is,

$$R_i = \frac{R_1}{2} + \frac{\frac{R_2}{2}R_L}{\frac{R_2}{2} + R_L}$$

$$R_i^1 = \frac{R_1}{2} + \frac{R_2 R_L}{R_2 + 2R_L} \qquad (11.7)$$

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Now to calculate the gain of the transmission gate, A, let us calculate the Thévenin voltage source magnitude and its internal resistance. The circuit in Fig. 11.19(d) now reduces to that shown in Fig. 11.19(e).
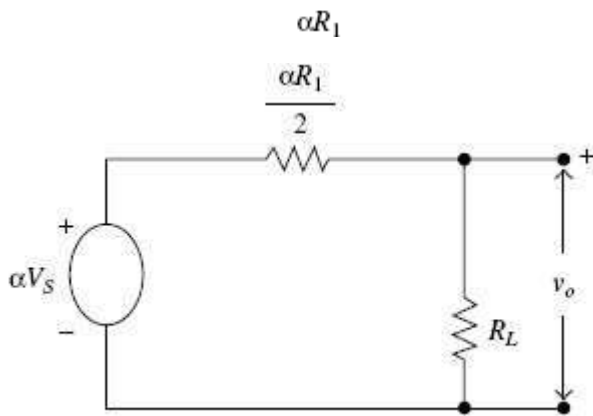
$$V_{th} = V_s \times \dfrac{\dfrac{R_2}{2}}{\dfrac{R_1}{2} + \dfrac{R_2}{2}} = V_s \times \dfrac{R_2}{(R_1 + R_2)} = \alpha V_s$$

$$R_{th} = \dfrac{R_1}{2} \| \dfrac{R_2}{2} = \dfrac{R_1 R_2}{2(R_1 + R_2)} = \alpha \dfrac{R_1}{2}$$

**FIGURE 11.19(e)** The simplified circuit of Fig. 11.19(d)

$$V_o = \dfrac{\alpha V_s R_L}{R_L + \alpha \dfrac{R_1}{2}}$$

$$A = \dfrac{V_o}{V_s} = \dfrac{\alpha R_L}{R_L + \alpha \dfrac{R_1}{2}} = \dfrac{\alpha}{1 + \alpha \dfrac{R_1}{2R_L}} \qquad (11.8)$$

Eq. (11.8) gives the expression for the transmission gain.

Four-diode Gates

The main disadvantages with two-diode gates are (i) although A is called the gain, the circuit actually offers a large attenuation to the signal since A is small (much less than 1); (ii) the two control voltages V_C and $-V_C$ should be equal in magnitude and opposite in polarity, failing which, there could be a pedestal in the output and (iii) $V_{n(min)}$ can be appreciably large, as seen in Example 11.1. These limitations can be overcome in a four diode gate shown in Fig. 11.20(a). The differences seen in the four diode gate as compared to a two diode gate shown in Fig. 11.16(a) are (i) instead of connecting control signals at points A and B, sources $+V$ and $-V$ are connected at these points and (ii) the control signals are connected through the two additional diodes D_3 and D_4 to points P_1 and P_2.
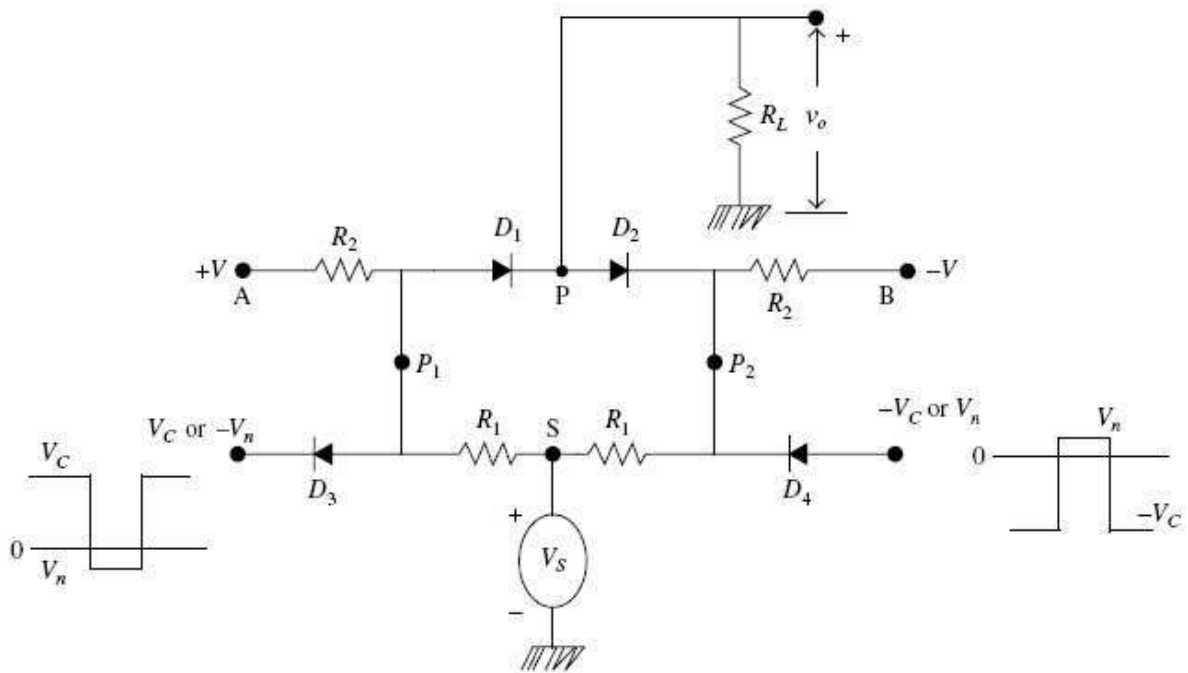
FIGURE 11.20(a) A four-diode gate

When the control voltages are V_C and $-V_C$, D_3 and D_4 are reverse-biased and are OFF. However, D_1 and D_2 are ON because of $+V$ and $-V$. The signal is connected to the load through R_1 and the conducting diodes, as shown in Fig. 11.20(b).

When the signal is transmitted, as D_3 and D_4 are OFF, even if there is a slight imbalance in the two control voltages $+V_C$ and $-V_C$, there is no pedestal at the output. Alternately, if the control voltages are at $-V_n$ and V_n respectively, D_3 and D_4 conduct. As a result, D_1 and D_2 are OFF and now the output is zero. When D_3 and D_4 are OFF, the circuit is similar to a two diode gate and A is the

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same as given in Eq. (11.1) except for the fact that V_C and $-V_C$ are replaced by V and $-V$. Also, the minimum value of voltage $V_{(min)}$ is the same as $V_{C(min)}$ in Eq. (11.4).

Therefore,

$$V_{min} = \frac{R_2}{R_1} \times \frac{R_3}{R_3 + 2R_L} \times V_s \qquad (11.9)$$

Let us now compute $V_{C(min)}$. If $R_f \ll R_L$, for a positive V_s the voltage at P_1 is AV_s. If D_3 is to be OFF, V_C must at least be equal to AV_s.

ie., $V_{C(min)} \approx AV_s \qquad (11.10)$

$V_{n(min)}$ is calculated to satisfy the condition that D_2 is OFF and D_4 is ON. Then we calculate the voltage at the cathode of $D_4 (K_2)$ due to sources $-V$ and V_s using the superposition theorem, as shown in Fig. 11.20(c). The minimum voltage $V_{n(min)}$ should at least be equal to V_{K2}.

Therefore,

$$V_{n(min)} = V_s \times \frac{R_2}{R_1 + R_2} - V \times \frac{R_1}{R_1 + R_2} \qquad (11.11)$$
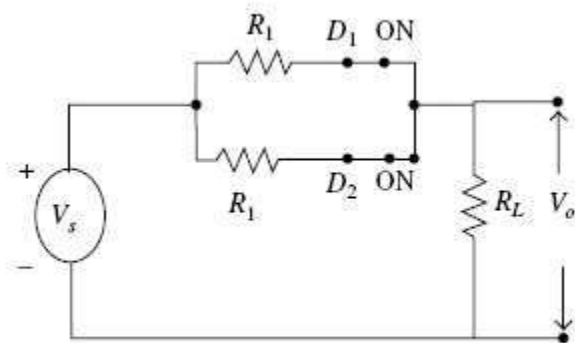
FIGURE 11.20(b) The circuit of Fig. 11.20(a) when D_1 and D_2 are ON and D_3 and D_4 are OFF

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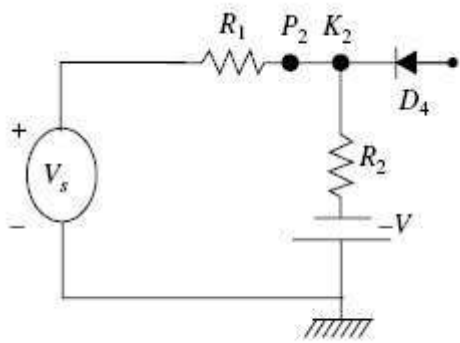
FIGURE 11.20(c) The circuit to calculate the voltage at the cathode of D_4

Six-diode Gates

For the four-diode gate shown in Fig. 11.20(a), the voltages $+V$ and $-V$ need to be large and have to be balanced to avoid pedestal. This gate circuit is insensitive to slight variations in the control voltages. Also, for the four diode gate [see Fig. 11.21(a)], the control voltages tend to become large and further there is a need for balanced control voltages, which is difficult. However, in the former case it is easy to choose large desired values for $+V$ and $-V$ and also easy to balance these two voltages as these are dc sources. For the circuit shown in Fig. 11.21(a), R_L is connected through a parallel path with the result the current is shared by these two parallel branches. The transmission gain A in both the cases, however, is approximately unity. A six diode gate is shown in Fig. 11.22, and it combines the features of the gate circuits shown in Figs. 11.20(a) and 11.21(a).

When no signal is transmitted, D_5 and D_6 conduct while D_1 to D_4 remain OFF. During the transmission, D_5 and D_6 are OFF and this six diode gate is equivalent to the four diode gate seen in Fig. 11.21(a), earlier. If the diodes D_5 and D_6 remain OFF for the signal amplitude V_s, then,
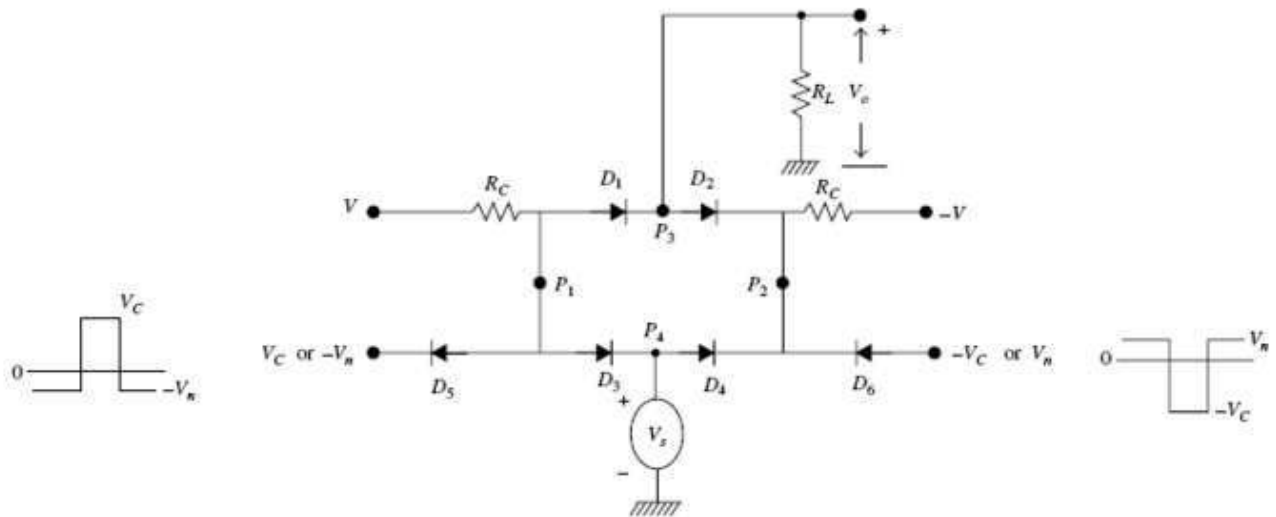
$$V_{C(min)} = V_s \qquad\qquad (11.18)$$

The minimum required value of V_n is $V_{n(min)}$ and is equal to V_s since the transmission diodes D_1 to D_4 will not conduct unless V_s exceeds V_n.

Hence,

$$V_{n(\min)} = V_s \qquad\qquad\qquad (11.19)$$

The expression for A is given by Eq. (11.16).

FIGURE 11.22 A six-diode gate

APPLICATIONS OF SAMPLING GATES

Sampling gates find applications in many circuits. Sampling gates are used in multiplexers, D/A converters, chopper stabilized amplifiers, sampling scopes, etc. Here, the three specific applications of the sampling gates in: chopper stabilized amplifier; sampling scope and time division multiplexer are discussed.

Chopper Stabilized Amplifiers

Sometimes it becomes necessary to amplify a signal v that has a very small dv/dt and that the amplitude of the signal itself is very small, typically of the order of milli-volts. Neither, ac amplifiers using large coupling condensers nor dc amplifiers with the associated drift would be useful for such an application. A chopper stabilized amplifier employing sampling gates can be a useful option in such an application, as shown in Fig. 11.27(a).
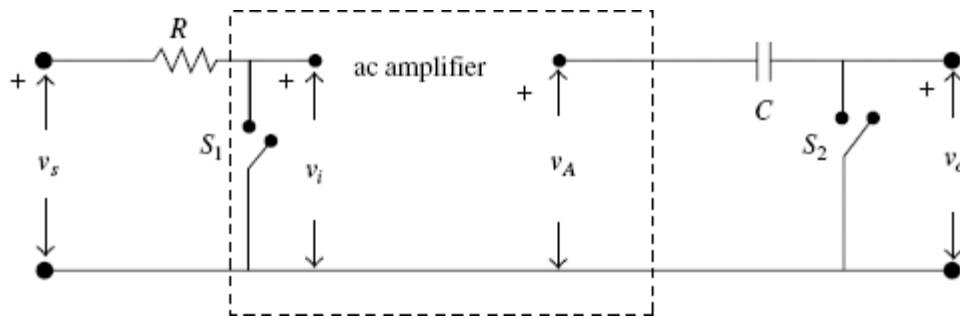
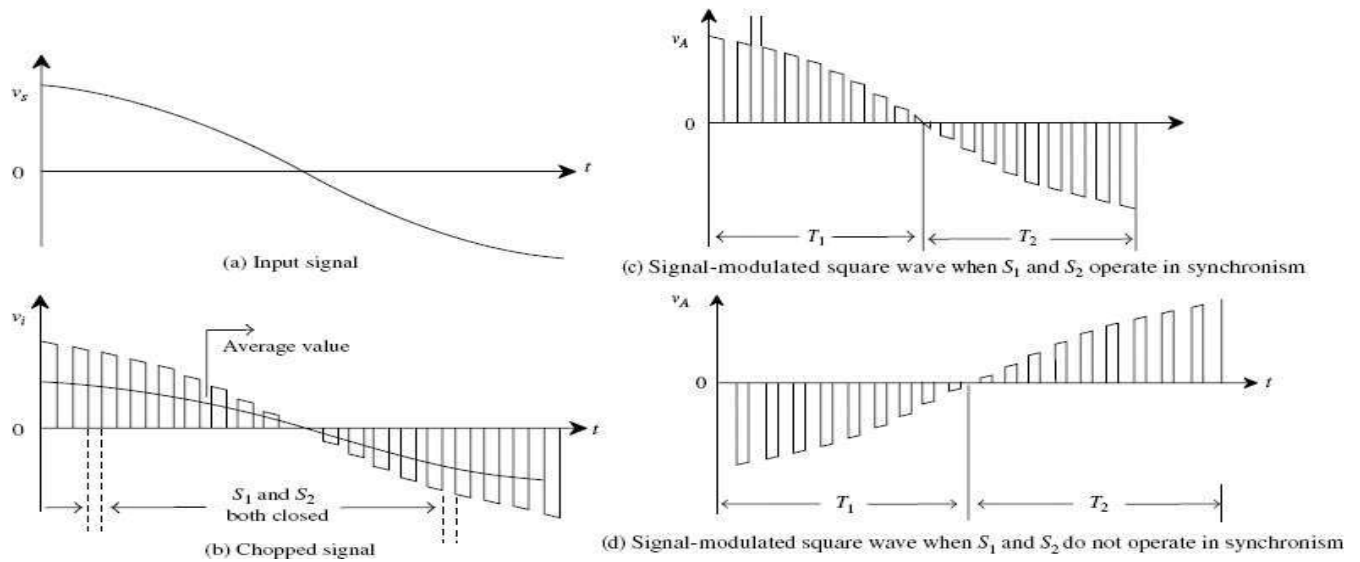**FIGURE 11.27(a)** A chopper stabilized amplifier

Let the input v_s to the amplifier be a slowly varying sinusoidal signal. Switch S_1 and S_2 open and close synchronously at a fast rate i.e., the switching frequency is significantly larger than the signal frequency. When S_1 is open, v_i is the same as v_s. When S_1 is closed, $v_i = 0$. As the switching frequency is large, the samples are taken at smaller time intervals. With the result, the signal v_i contains pulses with almost flat tops and have the same amplitude of the input signal as is available at the instant of sampling. As a result, the input of the amplifier v_i is a chopped signal—R and S_1 constitute the chopper. Hence, v_i can be described as a square wave at the switching frequency (if dv/dt is small), i.e., amplitude modulated by the input signal and superimposed on a signal (dashed line) that is proportional to v_s. The waveform v_A at the amplifier output is an amplitude modulated square wave, as shown in <u>Fig. 11.27(b)</u>. Hence, a chopper is also called a modulator.

Let S_1 and S_2 operate in synchronism. During $t = T_1$, the negative going component of v_A is zero and during $t = T_2$ the positive going component is zero. Also, because of the amplifier, v_o is greater than v_i in amplitude. Except for this change, v_A is similar to v_i, as shown in <u>Fig. 11.27(c)</u>. This signal is passed through a low pass filter which eliminates the squarewave and retrieves the original signal. If S_2 opens when S_1 is closed, the output is shifted in phase by 180°, as shown in <u>Fig. 11.27(d)</u>. C and S_2 constitute a synchronous detector. The chopper eliminates the need for a dc stabilized amplifier. This amplifier is called a chopper stabilized amplifier.
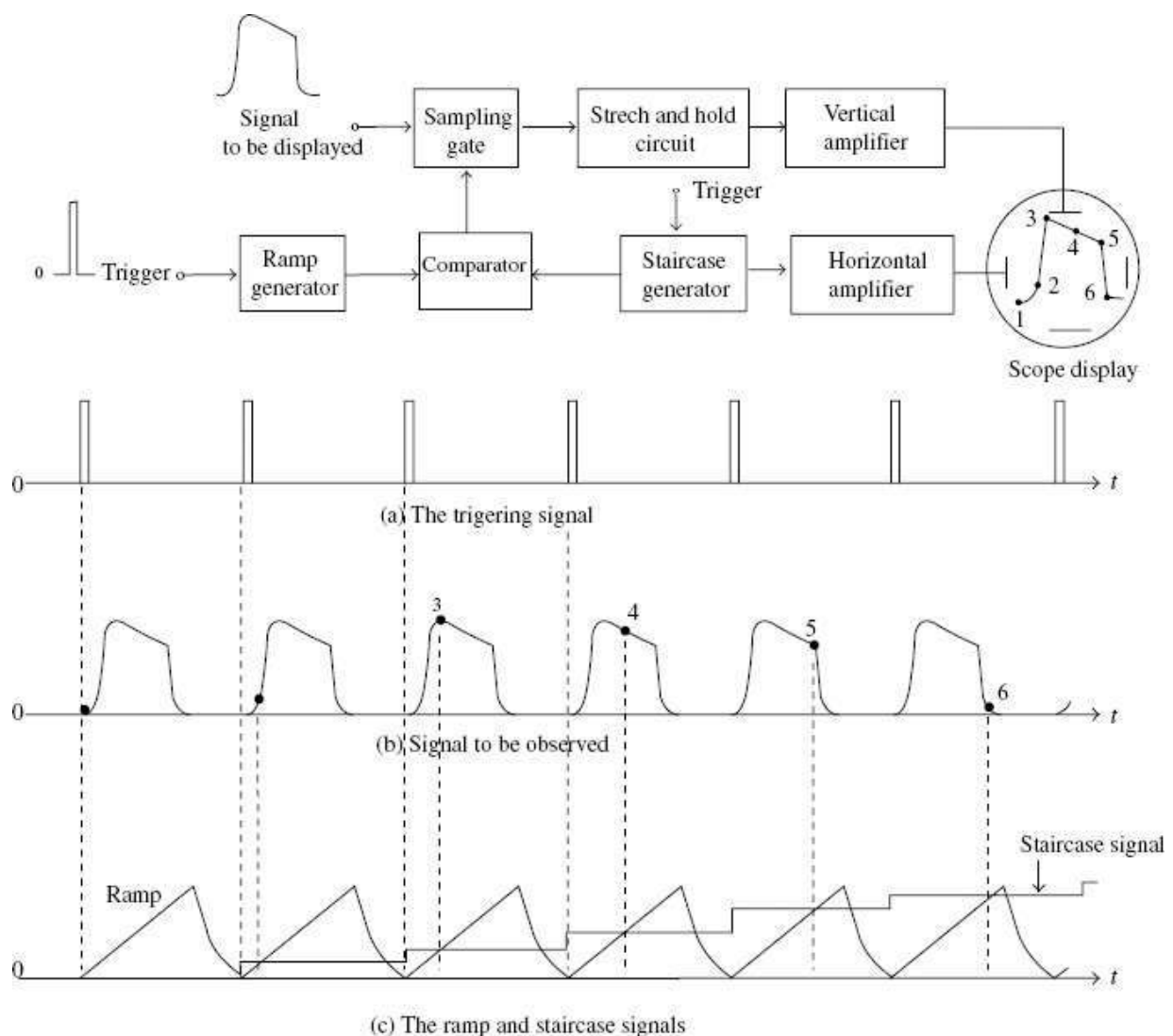
Sampling Scopes

Another application of a sampling gate is in a sampling scope used to display very fast periodic waveforms, having a rise time of the order of nano-seconds. A general purpose CRO may be used for displaying such waveforms. However, a CRO needs a wideband amplifier. A sampling scope eliminates the use of the high gain wideband amplifier. The basic principle of

a sampling scope is explained with the aid of a block diagram shown in Fig. 11.28(a) and the waveforms are shown in Fig. 11.28(b).

(a) Input signal

(b) Chopped signal

(c) Signal-modulated square wave when S_1 and S_2 operate in synchronism

(d) Signal-modulated square wave when S_1 and S_2 do not operate in synchronism

**FIGURE 11.27(b)** The waveforms of the chopper stabilized amplifier

FIGURE 11.28(a) The waveforms that explain the principle of sampling-scope

Let the trigger signals shown in <u>Fig. 11.28(a)</u> occur slightly prior to the occurrence of the pulses that are to be displayed on the screen. These trigger signals trigger ramp and staircase generators. The staircase generator has constant amplitude between the triggers and its amplitude jumps to a higher level at the instant the trigger is present. The amplitude of the staircase generator remains the same till the presence of the next trigger. The inputs to the comparator are the staircase and ramp signals. The instant the ramp reaches the amplitude of the staircase signal; a pulse is produced at the output of the comparator. This pulsed output of the comparator is used as the control signal for the sampling gate. When a control signal is present, the gate transmits a sample of the signal to the vertical amplifier whose amplitude is the same as that of the signal at the instant of sampling and has the same duration as the control signal. Points 1, 2..., 6 are the instants at which the samples are taken. The output of the staircase generator is connected to the horizontal deflecting plates.

When one sample is taken, say at instant 1, to go to the next sample, i.e., sample 2, the amplitude of sample 1 should be held constant till the next trigger pulse arrives. Therefore, it becomes necessary to hold the amplitude of the input signal between successive triggers and hence, the need for a stretch and hold circuit. The staircase generator moves the spot horizontally across the screen in steps and at each step the spot is deflected vertically proportional to the signal amplitude. The CRT beam is blanked normally and is un-blanked only at the time of display of the sample. Thus, the signal is represented by a series of dots.

Multiplexers

An analog time division multiplexer using a sampling gate is shown in Fig. 11.29(a). In the FET Q_1, Q_2 and Q_3 are ON when the control voltages V_{C_1}, V_{C_2} and V_{C_3} are at 0 V. The voltage V is more negative than the pinch off voltage of the FET. As such the FET is OFF when the gate voltage is V. During the period 0 to T_1, V_{C_1} is such that Q_1 is ON. At the same time Q_2 and Q_3 are OFF. Hence, input V_{s_1}, which is the sinusoidal signal is present at the output during this period. During the period T_1 to T_2, Q_2 is ON and Q_1 and Q_3 are OFF. Hence, only V_{s_2} is present at the output during this period. During the period T_2 to T_3, Q_3 is only ON and hence, V_{s_3} is present at the output. The output now contains all the input signals separated by a specific time interval, as shown in Fig. 11.29(b).
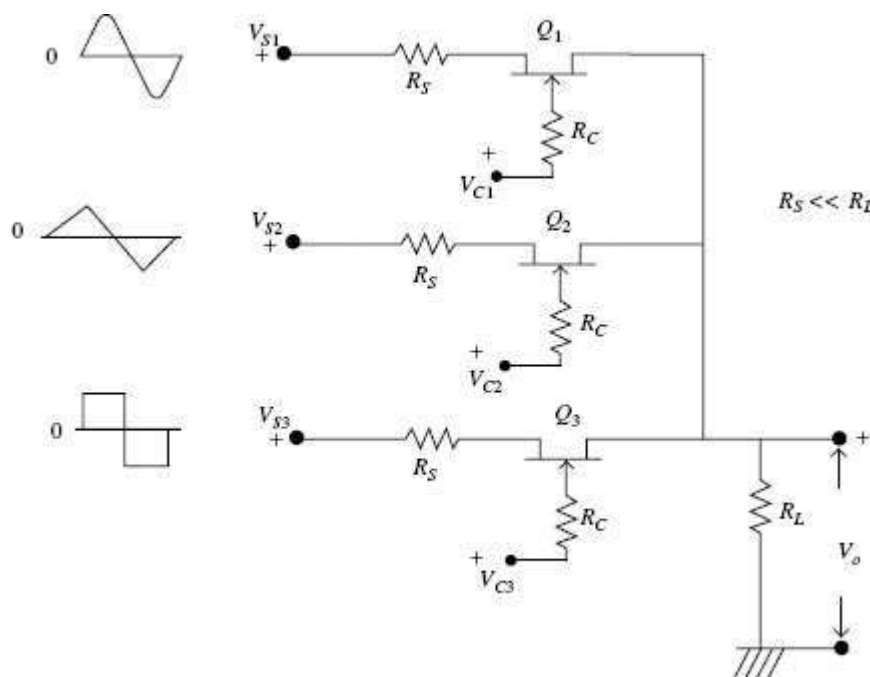
FIGURE 11.29(a) The sampling gate used for time division multiplexing

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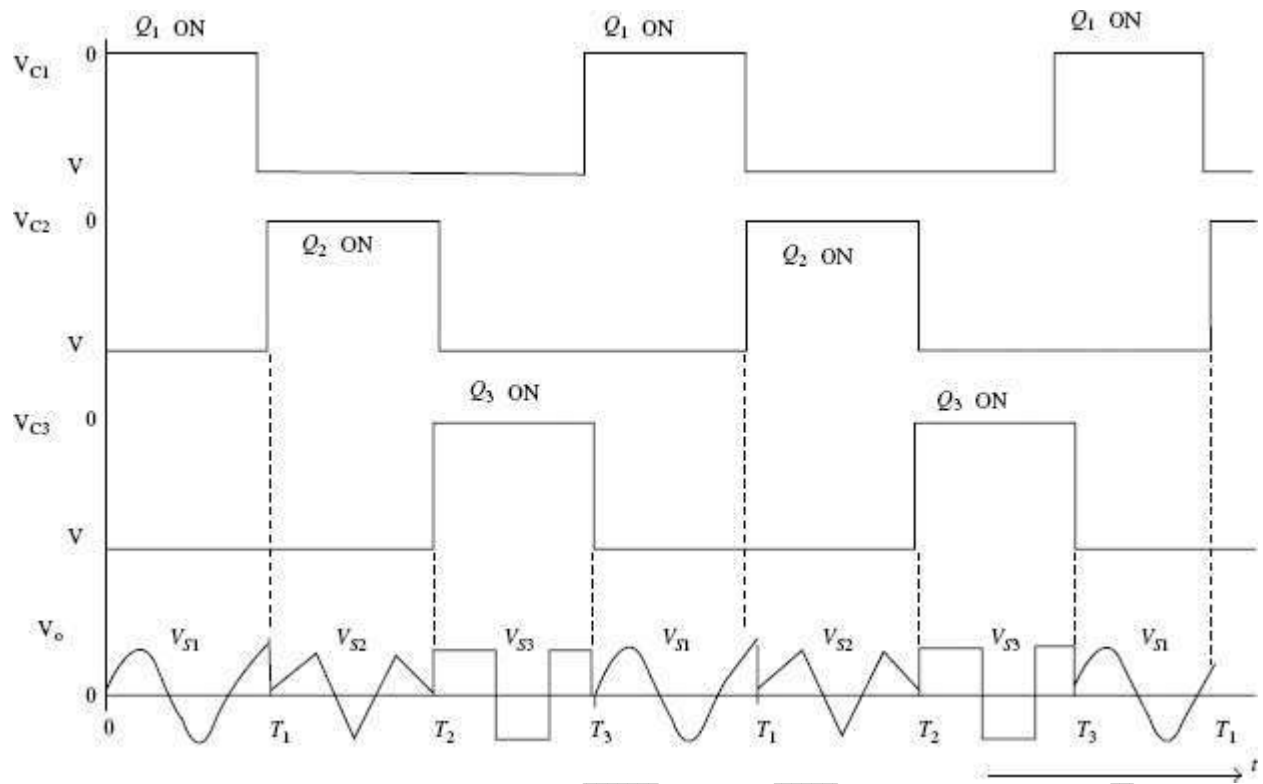
FIGURE 11.29(b) The control signals and the output of the multiplexer