Code: 9A04605

1

B.Tech IV Year II Semester (R09) Regular Examinations, March/April 2013

VLSI DESIGN

(Electronics and Computer Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 Write clearly about:
(a) Oxidation methods.
(b) Photolithography.
(c) Ion implantation.

2 (a) Draw the circuit diagram of a simple BiCMOS inverter and explain its operation.
(b) Compare CMOS with Bipolar transistors in different aspects.

3 Design a stick diagram for NMOS logic shown below: $Y = (A + B + C)'$

4 Realize the logic gates inverter, NAND and NOR gates using NMOS as well as with PMOS technology.

5 (a) On what design parameters does the performance of a chip is measured?
(b) Discuss that "designing the chip is a continuous trade off to optimize these design parameters depending on the application."

6 (a) Design a 3×8 binary decoder using NOR-NOR implementation of PLA.
(b) Implement the following function using PLA and EPROM $f_1 = \overline{ABC} + BC + AC$.

7 Explain the three domains under which the designing of ICs take place with different levels of design abstraction at each domain.

8 (a) With the help of an example explain how physical defects are categorized as logical faults.
(b) Explain the terms Controllability and Observability.

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1 Explain the following terms:
(a) Thermal oxidation technique.
(b) Kinetics of thermal oxidation.

2 (a) Derive an expression for Rds of an n channel enhancement MOSFET in saturation region.
(b) Find g_m and r_{ds} for n channel transistor with V_{GS}=1.2 V, V_t = 0.8 V, W/L = 10, V_{DS} = V_{eff} + 0.5V, $C_{OX}\mu_n$ = 92 μA/v^2. The output impedance constant = 95.3*10^{-3} v^{-1}.

3 Clearly explain the VLSI design flow with a neat flow chart.

4 (a) Explain about switch logic.
(b) Describe constructional features and performance characteristics of pseudo-NMOS logic.

5 (a) Explain through an example the role of pass transistors in optimizing the chip design.
(b) With the help of a circuit diagram explain the working of three transistor dynamic RAM cell.

6 (a) Give a brief description about CPLDs.
(b) With the help of architectural diagram explain the working of FPGA.

7 Summarize in detail the wide variety of simulators used at different levels of design abstraction.

8 (a) Write about fault grading and fault simulation.
(b) Explain the following fault simulation methods:
(i) Serial fault simulation. (ii) Parallel fault simulation.
(iii) Concurrent fault simulation.

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1 Explain clearly about CMOS process enhancements.

2 (a) Determine the pull-up and pull down ratio for an nMOS inverter driven through one or more pass transistors with neat equivalent circuits.
(b) What are different forms of pull-ups?

3 (a) Draw the structure of a transistor.
(b) What are the transistor parasitics.
(c) Write about tub ties, wires, vias.
(d) What distinguishes a tub tie from an n diff-metal 1via?

4 (a) What do you mean by inverter delay? Explain.
(b) Draw the model for deviation of the time delay and explain it.

5 (a) With the help of a logical schematic explain the working of a comparator.
(b) Implement a parity generator using standard dynamic CMOS logic?

6 (a) Differentiate between FPGA and PLA.
(b) Implement the following functions using multiple outputs PLA.

$$f_1 = \overline{ABC} = +AB + BC + CA.$$

$$f_2 = AB\overline{C} + A\overline{B}C + \overline{A}BC.$$

7 (a) Explain about event driven simulation.
(b) Using VHDL as a tool, write a program to synthesize a mod 10 counter.

8 (a) What are BIST techniques?
(b) Explain how BILBO is used for scan-path-test and also as a test vector generator.

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VLSI DESIGN

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1 (a) What are the problems of IC designs?
(b) Explain clearly about power consumption in CMOS.

2 (a) Explain about MOS gate capacitance model with the required diagrams.
(b) MOS diffusion capacitance model with neat diagrams.

3 Design stick diagram and layout for the NMOS logic shown below:
$Y= [(A+B)*C]^{/}$.

4 (a) Draw the cross sectional view of a chip showing wires and vias.
(b) Explain about wire parasitics.
(c) For an aluminum interconnect, L=1 cm, W = 3 μm and H = 1μm, t_{ox} = 0.8μm, ρ = 31μohm and C_L = 2.5 pF. Calculate propagation delay Tp of aluminum interconnect.

5 (a) With the help of a circuit diagram explain the working of a dynamic one bit storage element?
(b) Using the storage element implement a 4-bit dynamic shift register.

6 Explain about various techniques of programmable logic used to optimize the investment made in the system design?

7 With respect to logic synthesis explain the following:
(a) Flattering.
(b) Factorization.
(c) Mapping.

8 (a) What is meant by fault simulation? Explain.
(b) Compare Serial fault simulation and parallel fault simulation.

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