

Code: 15A04306

B.Tech II Year I Semester (R15) Regular &amp; Supplementary Examinations November/December 2018

**DIGITAL LOGIC DESIGN**

(Common to CSE and IT)

Time: 3 hours

Max. Marks: 70

**PART – A**  
(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

- (a) What is an unit distance code? Give an example.
- (b) Find the complement of the function:  $F = x(y'z' + yz)$  by taking their duals and complementing each literal.
- (c) Define don't care condition with example.
- (d) State the limitations of Karnaugh map.
- (e) Define priority encoder.
- (f) Distinguish between encoder and multiplexer.
- (g) Define shift registers.
- (h) Give the comparison between combinational circuits and sequential circuits.
- (i) What is mask-programmable?
- (j) Define fan-in and fan-out of a logic gate.

**PART – B**

(Answer all five units, 5 X 10 = 50 Marks)

**UNIT – I**

- 2 (a) Using 2's compliment, perform  $(42)_{10} - (68)_{10}$ .
- (b) Simplify the following expression:  $Y = (A + B)(A + C')(B' + C')$

**OR**

- 3 (a) Simplify the following three variable expressions using Boolean algebra:  $Y = \sum m(1, 3, 5, 7)$ .
- (b) Convert the given expression in standard POS form:  $Y = (A + B)(B + C)(A + C)$ .

**UNIT – II**

- 4 Minimize the following function using Karnaugh map method and draw simplified logic diagram:  
 $(A, B, C, D, E) = \sum m(0, 7, 8, 9, 10, 12, 14, 16, 18, 20, 24, 28) + \sum d(2, 5, 13)$

**OR**

- 5 (a) Implement the following function in NAND-NAND two level forms and draw the circuit:  
 $Y = AC + ABC + A'BC + AB + D$
- (b) Convert the given expression in standard SOP form and draw the logic diagram:  $Y = A + ABC$ .

**UNIT – III**

- 6 Design and draw the logic diagram of full subtractor using two half subtractors.

**OR**

- 7 Using 8 to 1 multiplexer, realize the Boolean function:  
 $T = f(w, x, y, z) = \sum(0, 1, 2, 4, 5, 7, 8, 9, 12, 13)$

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**UNIT – IV**

8 Design a mod-10 synchronous counter using JK flip flops. Write excitation table and state table.

**OR**

9 A sequential circuit with two D flip flops A and B, input X and output Y is specified by the following next state and output equations:

$$A(t + 1) = AX + BX$$

$$B(t + 1) = A'X$$

$$Y = (A + B)X'$$

Draw the logic diagram, derive state table and state diagram.

**UNIT – V**

10 Implement the following functions using PLA.

$$A(x, y, z) = \Sigma m(1, 2, 4, 6)$$

$$B(x, y, z) = \Sigma m(0, 1, 6, 7)$$

$$C(x, y, z) = \Sigma m(2, 6)$$

**OR**

11 Draw and explain the circuit diagram of the CMOS NOR gate.

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