Code: 15A04306 **R15**

B.Tech II Year I Semester (R15) Supplementary Examinations June 2018

DIGITAL LOGIC DESIGN

(Common to CSE and IT)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) Perform subtraction $(1110)_2$- $(1010)_2$ using 2' complement method.

(b) Find the compliment of the following expression (AB' + C) D' + E.

(c) What are the limitations of K-maps?

(d) What is meant by 'Don't care' conditions? What are its uses?

(e) Write the differences between serial adder and parallel adder.

(f) What is meant by encoder? Write its functions.

(g) What is the difference between synchronous and asynchronous counter?

(h) List the applications of Flip-Flops.

(i) What is programmable logic array? How it differs from ROM.

(j) Write the characteristics of Transistor-transistor logic.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) Convert the following:

(i) $(163.789)_{10}$ = ($)_8$.

(ii) $(101101110001.00101)_2$ = ($)_8$.

(iii) $(292)_{16}$ = ($)_2$.

(b) Prove that AND - OR network is equivalent to NAND-NAND network.

OR

3 (a) The solution to the quadratic equation $x^2 - 11x + 22 = 0$ is x = 3 and x = 6. What is the base of numbers?

(b) Find the complement of the following and show that F.F' = 0 and F + F' = 1.

(i) F = xy' + x'y.

(ii) F = (x + y' + z)(x' + z')(x + y).

UNIT – II

4 (a) Simplify the following function using K- map and implement the same using NAND gates:

F(A,B,C)=∑ (0,2,4,5,6,7)

(b) Obtain the simplified POS and SOP expressions for the function using K-Map:

F(A,B,C,D)= ∑(1,3,5,8,9,13)+∑d (0,7,12,14).

OR

5 (a) Simplify the following Boolean functions, using four variable maps:

(i) F(W, X, Y, Z) = ∑(1,4,5,6,12,14,15).

(ii) F(A, B, C, D) = ∑(1,5,9,10,11,14,15).

(b) Use the tabular procedure to simplify the given expression:

F(A,B,C,D) = Σm (0,4,12,16,19,24,27,28,29,31) in SOP form.

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UNIT – III

6 (a) Draw and explain the operation of 3 to 8 decoder.

(b) Design and draw a logic circuit diagram for full adder / subtractor. Let us consider a control variable *w* and the designed circuit that functions as a full adder when *w* = 0, as a full subtractor when *w* = 1.

OR

7 (a) Design a full subtractor and implement it using NAND gates. Explain its operation with the help of truth table.

(b) Draw the schematic diagram and truth table for full adder. Explain the design approach for full adder using universal gates. Draw the relevant logic diagrams with necessary expressions.

UNIT – IV

8 (a) Explain the working of a master-slave JK flip flop. State its advantages.

(b) Draw the logic diagram of a 4 bit shift resister. Explain how shift-left and shift-right operations are performed.

OR

9 (a) Design modulo -12 up synchronous counter using T- flip flops and draw circuit diagram.

(b) Convert T-Flip Flop to D-Flip Flop and D-Flip Flop to T-Flip Flop, with relevant truth tables and expressions. Also draw the logic diagrams.

UNIT – V

10 (a) Design the logic diagram using PLA with following functions:

(i) Y_1 = AB+A'C+ABCD.

(ii) Y_2 = AB'C +ABC' +AC'.

(iii) Y_3 = AB.

(iv) Y_4 = 0.

(b) Give the comparison between TTL, RTL and DTL.

OR

11 (a) Design a PAL for the following logical functions:

(i) Y_1 = AB+A'CB'.

(ii) Y_2 = AB'C+AB+AC'.

(iii) Y_3 = AB+BC+CA.

(b) Explain the operation and characteristics of resistor–transistor logic.

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