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Code: 15A04301

B.Tech II Year I Semester (R15) Supplementary Examinations June 2018

## **ELECTRONIC DEVICES & CIRCUITS**

(Common to EEE, ECE and EIE)

Time: 3 hours Max. Marks: 70

## PART – A

(Compulsory Question)

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- 1 Answer the following:  $(10 \times 02 = 20 \text{ Marks})$ 
  - (a) What are the parameters on which the depletion layer is capacitance depends?
  - (b) Distinguish between SCR and TRIAC.
  - (c) A full wave rectifier, using a capacitor filter has to supply 30 V DC to a load resistance of 1 kΩ. Assuming the diode and transformer winding resistance to be negligible, estimate the value of capacitor filter for a ripple factor of 0.01.
  - (d) Define ripple factor.
  - (e) A transistor has CE current gain of 100. If the collector is 40mA, what is the value of emitter current?
  - (f) Distinguish between FET and BJT.
  - (g) Define stability factor of transistor.
  - (h) What is the advantage of using potential divider bias?
  - (i) Why hybrid parameters are called so?
  - (j) Write the approximate conversion formulae for current gain and voltage gain of CB configuration from CE configuration.

## PART - B

(Answer all five units,  $5 \times 10 = 50 \text{ Marks}$ )

UNIT - I

With a neat diagram, explain the energy band diagram of PN junction diode.

OR

3 Explain the construction, operation and characteristics of Tunnel diode.

[ UNIT – II ]

With neat circuit diagram and waveforms, explain the working of full wave bridge rectifier with capacitor filter.

OR

A 230 V, 50 Hz ac signal is given as input to a centre tapped full wave rectifier through a 5:1 step down transformer. The load resistance is found to be 100  $\Omega$ . Determine the dc output voltage, peak inverse voltage and rectification efficiency.

(UNIT – III

With a neat circuit diagram, explain the CE configuration of BJT. Also draw and explain its input and output characteristics.

**OR** 

With neat diagrams, explain the construction and operating characteristics of EMOSFET.

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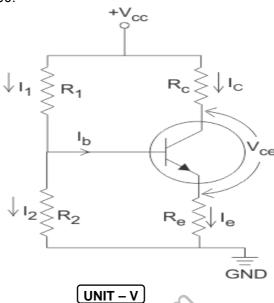
UNIT – IV

8 What is a biasing circuit? Explain the fixed bias and collector to base bias circuits in detail.

OF

9 Determine the value of collector current and collector to emitter voltage for the voltage divider bias circuit shown below.

 $V_{CC}=10~V;~~R_1=10~k\Omega;~~R_2=5~k\Omega;~~R_C=1~k\Omega;~~R_e=500~\Omega.$  Assume  $V_{BE}$  = 0.7V and  $\beta$  = 100.



A transistor used in a common base configuration has the following h-parameters:

$$h_{ib} = 28\Omega;$$
  $h_{fb} = -0.98;$   $h_{rb} = 5 \times 10^{-4}$   $h_{ob} = 0.34 \,\mu\text{J}$ 

Calculate the values of input resistance, output resistance, current gain and voltage gain, if the load resistance is  $1.2 \text{ k}\Omega$ . Assume source resistance as zero.

OR

- 11 (a) Find the values of  $h_{fb}$  and  $h_{fc}$  if the values of  $h_{fe}$  of a transistor is 50.
  - (b) Write the conversion formulae for common base configuration from the common emitter h-parameter values.

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