

Code: 15A04302

B.Tech II Year I Semester (R15) Supplementary Examinations June 2018

SWITCHING THEORY & LOGIC DESIGN

(Common to ECE & EIE)

Time: 3 hours

Max. Marks: 70

PART – A
(Compulsory Question)

1 Answer the following: (10 X 02 = 20 Marks)

- (a) Converting the following to decimal and then to octal:
(i) $(4243)_{16}$. (ii) $(125F)_{16}$.
- (b) Write are the steps for tabular method-simplification of Boolean function?
- (c) Design procedure for combinational logic circuits.
- (d) Write the differences between Latches and Flip-Flops.
- (e) Give design procedure for asynchronous sequential circuits.
- (f) Define EPROM and EEPROM.
- (g) Write the basic definition for Boolean algebra.
- (h) Give comparison between POS and SOP.
- (i) What is multiplexer with example?
- (j) Briefly explain about D-flip-flop.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

- 2 (a) Explain Logic Operations and logic gates with examples.
- (b) Perform the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend: (i) $11010-10000$. (ii) $11010-1101$. (iii) $1010100-1010100$.

OR

- 3 (a) Why the binary number system is used in computer design? And what is the necessity of binary codes?
- (b) Perform the following using BCD arithmetic. Verify the result:
(i) $1273_{10} + 9587_{10}$. (ii) $7762_{10} + 3838_{10}$. (iii) $7842_{10} + 4956_{10}$.

UNIT – II

- 4 Implement the function F with the following two level forms:
(i) NAND-AND. (ii) AND-NOR. (iii) OR-NAND. (iv) NOR-OR.
 $F(A,B,C,D) = \pi (0,1,2,3,4,8,9,12)$

OR

- 5 Minimize following function using Tabular minimization:
 $F(A,B,C,D) = \pi M (6,7,8,9) + d(10,11,12,13,14,15)$

UNIT – III

- 6 (a) What is decoder? Construct 3*8 decoder Using logic gates and truth table.
- (b) Implement the following multiple output combinational logic using 4 line to 16 line decoder?

OR

- 7 (a) Design a combinational logic to subtract one bit from the other. Draw the logic diagram using NAND and NOR gates.
- (b) Explain the function of Digital magnitude comparator using a neat diagram.

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UNIT – IV

- 8 (a) Convert the following: (i) JK flip-flop to T flip-flop. (ii) RS flip-flop to D flip-flop.
(b) Draw the circuit diagram of 4-bit Ring Counter D flip-flop and explain its Operation with the help of bit pattern.

OR

- 9 (a) Compare synchronous and asynchronous Sequential circuits with examples.
(b) Design a Mod-6 synchronous counter using JK flip-flops? With state Table and K-map simplification.

UNIT – V

- 10 (a) Derive the PLA programming table for the combinational circuit that squares a 3-bit number.
(b) Design a BCD to excess-3 code convert using: (i) ROM. (ii) PAL.

OR

- 11 (a) A combinational circuit is defined by the functions:
 $F_1 = (A, B, C) = \pi m(3, 5, 6, 7)$
 $F_2 = (A, B, C) = \pi m(0, 2, 4, 7)$
Implement the circuit with a PAL having three inputs, four product terms and two outputs.
(b) Explain the field programmable gate array (FPGA) with suitable block diagram.

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