

B.Tech II Year II Semester (R15) Supplementary Examinations December 2018

COMPUTER ORGANIZATION

(Common to CSE and IT)

Time: 3 hours

Max. Marks: 70

PART – A

(Compulsory Question)

1 Answer the following: (10 X 02 = 20 Marks)

- (a) Registers R_1 and R_2 contain data values 1800 and 3800 respectively in decimal and the word length of the processor is 4 bytes. What is the effective address of the memory operand for the instruction $ADD\ 100(R_2), R_6$?
- (b) What is the use of buffer register?
- (c) State the principle of operation of a carry look-ahead adder.
- (d) Write the Add/subtract rule for floating point numbers.
- (e) What will be the width of address and data buses for a $512K \times 8$ memory chip?
- (f) Differentiate static RAM and dynamic RAM.
- (g) Why does DMA have priority over the CPU when both request a memory transfer?
- (h) What is bus arbitration?
- (i) Is register renaming is done in pipelined processor to handle certain kinds of hazard? Justify your answer.
- (j) How an array processor helps to improve the performance in arithmetic operations?

PART – B(Answer all five units, $5 \times 10 = 50$ Marks)**UNIT – I**

- 2 (a) List the steps needed to execute the machine instruction $add\ LOC, R0$ in terms of transfers between memory and processor and some simple control commands. Assume that the instruction itself is stored in the memory at location INSTR and that this address is initially in register PC.
- (b) How the addresses can be assigned across the words by using the big-endian and the little-endian representations?

OR

- 3 Exemplify different functional units of a digital computer. Mention the functions of different processor registers such as IR, MAR and PC.

UNIT – II

- 4 Compare the restoring and non-restoring division algorithm. Perform the division using the restoring division algorithm. Dividend = 1000, Divisor = 11.

OR

- 5 With a neat block diagram, explain about the micro programmed control unit and its operations in detail?

UNIT – III

- 6 A computer system has a main memory consisting of 16 M words. It also has a 32K word cache organized in the block-set-associative manner, with 4 blocks per set and 128 words per block.
 - (a) Calculate the number of bits in each of the TAG, SET and WORD fields of the main memory address format.
 - (b) How will the main memory address look like for a fully associative mapped cache?

OR

- 7 Discuss the operation of memory hierarchy with a neat sketch.

Contd. in page 2

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UNIT – IV

8 Identify and explain the various methods available to handle multiple devices using interrupts.

OR

9 With a neat sketch, discuss various standard I/O interfaces in detail?

UNIT – V

10 Why the data hazards occur in the pipelining process? Explain the methods for dealing with data hazard using your own example.

OR

11 Categorize and discuss various forms of parallel processing based on Flynn's taxonomy with a neat sketch.

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