Code: 15A04511 **R15**

B.Tech III Year I Semester (R15) Supplementary Examinations June 2018

COMPUTER ORGANIZATION

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) When an interrupt signal is raised?
(b) What is a subroutine?
(c) Draw the graphical symbol for three-state buffer.
(d) What is stack pointer?
(e) What is the use of control address register and control data register?
(f) Describe dividend alignment.
(g) What is handshaking?
(h) Define virtual memory.
(i) When data dependency conflicts arise.
(j) Describe polling in a bus system.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) Draw and explain the functional unit of a computer system.
(b) With suitable example, explain assembly language notation.

OR

3 (a) List and explain various types of computers in detail.
(b) Explain register mode and absolute mode with suitable examples.

UNIT – II

4 (a) What are the various shift micro operations? Explain about them in detail.
(b) Perform the logic AND, OR and XOR with the two binary strings 10011100 and 10101010.

OR

5 Design the common bus system for four registers with a neat diagram.

UNIT – III

6 Illustrate Booth algorithm and show the step-by-step multiplication process using Booth algorithm to multiply the following number. Assume 5-bit registers that hold signed numbers. The multiplicand is +15.
(+15) X(+13)

OR

7 Illustrate addition and subtraction of two floating point binary numbers with a flow chart.

UNIT – IV

8 (a) How many characters per second can be transmitted over a 1200-baud line in each of the following modes? (Assume a character code of eight bits). (i) Synchronous serial transmission. (ii) Asynchronous serial transmission with two stop bits. (iii) Asynchronous serial transmission with one stop bit.
(b) Explain the memory hierarchy of a computer system with a neat diagram.

OR

9 What is the use of DMA? Explain about the DMA controller with a block diagram.

UNIT – V

10 (a) A non-pipeline system takes 50ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speed up that can be achieved?
(b) What is Interprocessor synchronization? Explain briefly about it.

OR

11 (a) What are the various fields in instruction format of a vector processor? Explain.
(b) Describe briefly about the Hypercube interconnection.