Code: 15A04504 **R15**

B.Tech III Year I Semester (R15) Supplementary Examinations June 2018

DIGITAL SYSTEM DESIGN

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) Why commercial ECL families are not as popular as CMOS and TTL?

(b) Define speed-power product. What is its significance?

(c) Write the syntax for VHDL function declaration.

(d) Sketch the VHDL program file structure.

(e) Write the expressions for AGTBOUT and ALTBOUT of a 74x85 comparator.

(f) Interpret 74x999 as a full subtractor.

(g) Define a twisted ring counter.

(h) What is the significance of RCO pin in 74x163 MSI counter?

(i) What is positive and negative triggering in flip-flops?

(j) What is a barrel shifter and how is it different from other shift registers?

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 Design logic diagram for AND-OR-INVERT gate. Construct the same using CMOS logic and analyze the circuit with the help of function table.

OR

3 Design and summarize the internal 3 sections of LS-TTL NAND gate and analyze the circuit with the help of function table.

UNIT – II

4 Model the design flow of VHDL program with front-end and back-end steps.

OR

5 Develop a structural VHDL program for a 4-bit prime number detector.

UNIT – III

6 Design a 5-to-32 decoder using 74x138's.

OR

7 Construct 12-bit comparator using 74x85's and write a VHDL program for comparing 8-bit unsigned integers.

UNIT – IV

8 Model the MIS device IC 74x163 in free running mode. Analyze with the help of functional table. Develop VHDL program for a 74x163 like 4-bit binary counter.

OR

9 Sketch the logic diagram of 74x194 4-bit universal shift register and develop a VHDL module for the same.

UNIT – V

10 Design a 16-bit barrel shifter using 74x151 that performs right circular shift operation. Demonstrate the circuit using VHDL program.

OR

11 Design positive edge triggered D flip-flop and explain its functional and timing behaviour. Also develop a VHDL program.

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