

Code: 15A04509

B.Tech III Year I Semester (R15) Supplementary Examinations June 2018

**LINEAR & DIGITAL IC APPLICATIONS**

(Electrical &amp; Electronics Engineering)

Time: 3 hours

Max. Marks: 70

**PART – A**  
(Compulsory Question)

\*\*\*\*\*

- 1 Answer the following: (10 X 02 = 20 Marks)
- When is an Op-Amp said to be an ideal?
  - Draw sample and hold circuit.
  - Draw the functional diagram of successive approximation ADC.
  - A 12 bit DAC has a resolution of 20m V/LSB. Find the full scale output voltage.
  - Find the order of a low pass Butterworth filter that is to provide 40dB attenuation at  $\omega/\omega_h = 2$ .
  - Design a phase shift oscillator to oscillate at 100Hz.
  - Mention the advantages of integrated circuits over discrete components.
  - What happens when excess gate voltage is given to CMOS devices?
  - Design a full adder circuit using decoder.
  - Design an 1-bit magnitude comparator.

**PART – B**  
(Answer all five units, 5 X 10 = 50 Marks)**UNIT – I**

- 2 (a) Elaborate on an Op-Amp circuit which can generate single output pulse with adjustable time duration in response to a trigger signal.
- (b) Design an amplifier with a gain of -10 and input resistance equal to 10 k $\Omega$ .

**OR**

- 3 State the need for frequency compensation technique. With neat gain  $V_s$  frequency curves elaborate and derive the necessary equations used for different compensating techniques.

**UNIT – II**

- 4 What output voltage will be produced by a D/A converter whose output range is 0 to 10 V and whose input binary number is:
- 10 (for 2-bit DAC)
  - 0110 (for 4-bit DAC)
  - 10111100 (for 8-bit DAC).

**OR**

- 5 Derive lock-in range and capture range of PLL with its neat block diagram and its explanation.

**UNIT – III**

- 6 (a) What are delay equalizers and why is it called so? With circuit diagram, derive the necessary equations to justify it.
- (b) Design a triangular wave generator using Op-Amp.

**OR**

- 7 Derive the output frequency of VCO.

**UNIT – IV**

- 8 Differentiate between MOS and CMOS. Elaborate on open drain and tristate CMOS outputs.

**OR**

- 9 Design a two input NAND gate using TTL open collector output and tristate output.

**UNIT – V**

- 10 Design a synchronous decade counter using D flip-flop.

**OR**

- 11 (a) Design a full subtractor circuit using 4x1 multiplexers.
- (b) Design a 2-bit magnitude comparator.