Code: 15A04604

R15

B.Tech III Year II Semester (R15) Regular Examinations May/June 2018

VLSI DESIGN

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) MOSFETs are said to be more efficient than BJTs. Justify the answer.

(b) Define the terms: (i) Body effect. (ii) Channel length modulation.

(c) How to evaluate routing capacitance of MOS device?

(d) What are the importance of CMOS design rules?

(e) What is the power delay product for the load capacitance C_L = 3.5μF, given the input voltage V_{DD} = 5 V?

(f) List out the steps in physical design layout.

(g) Mention about various Multiplier architectures followed for VLSI Design.

(h) Give the difference between Full-custom and Semi-custom devices.

(i) What are the special features of design verification tools?

(j) What is Built-in-self-test?

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 Explain in detail about the steps involved in CMOS IC fabrication process with essential diagrams.

OR

3 Draw the I_{ds}-V_{ds} relationship curve and discuss in detail about its role in the MOS design equations.

UNIT – II

4 (a) Derive the expression for resistance estimation in VLSI circuits.

(b) Write short notes on driving large capacitive loads.

OR

5 (a) Explain the 2μm CMOS design rules for contacts and transistors.

(b) Briefly discuss about scaling of MOS circuits and its limitations.

UNIT – III

6 With a detailed step by step process, design and draw the AND-OR-INVERT form complex gates in CMOS logic for the output equation Y = ($\overline{AB + CD}$).

OR

7 Give a detailed note on floor-planning and placement in the physical design flow of a CMOS circuit design.

UNIT – IV

8 Explain about any one multiplier architecture in VLSI design. What are the challenging issues to be considered for the same?

OR

9 Illustrate with neat architecture diagram and explain about various functional blocks of Field Programmable Gate Array (FPGAs).

UNIT – V

10 (a) Write a short note on circuit synthesis.

(b) Give comparison of design capture tools and design verification tools.

OR

11 Explain in detail about design for testability.