Code No: 115EB **R13**

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**
**B.Tech III Year I Semester Examinations, November - 2015**
**LINEAR AND DIGITAL IC APPLICATIONS**
**(Common to ECE, BME)**

**Time: 3 hours** **Max. Marks: 75**

**Note:** This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

**PART - A (25 Marks)**

1.a) Significance and definition of upper and lower threshold points of a Schmitt trigger. [2]
b) Mention the reasons why open loop is not preferred for linear applications. [3]
c) List various applications of IC 555 Timer. [2]
d) Differentiate Bessel, Butterworth and Chebyshev filters. [3]
e) Define the following terms as related to DAC: i) Linearity ii) Resolution. [2]
f) Compare R-2R and Weight Resistor types of ADC. [3]
g) What is meant by Tri-state logic? [2]
h) What is the purpose of priority encoders. [3]
i) Write the applications of shift registers. [2]
j) Differentiate Static and Dynamic RAMs. [3]

**PART - B (50 Marks)**

2.a) Explain the why emitter follower circuit is used as level shifter.
b) Design an op-amp differentiator to differentiate an input signal that varies in frequency from 10Hz to about 1 KHz. [5+5]

**OR**

3.a) What are the disadvantages of using zero crossing detector? How it can be overcome using Schmitt trigger?
b) Draw the internal architecture of IC 723 voltage regulator and explain. [5+5]

4.a) Draw the block diagram for PLL and explain in detail.
b) Explain two of the following applications for which PLL is used:
i) AM detector ii) FM demodulator. [4+6]

**OR**

5.a) An ideal low pass filter having $f_H$=5 kHz is cascaded with high pass filter having $f_L$=4.8 kHz. Sketch the frequency response of the cascaded filter.
b) Explain the monostable operation of the 555 timer and derive the expression for the period of a pulse generated by the Timer. [5+5]

6.a) Explain the operation of the fastest analog to digital converter. What is the main draw back of this converter? Compare this converter with other types.
b) Draw the circuit of a Ladder type DAC for 4 bits and derive expression for output voltage. [5+5]

**OR**

7.a) Draw a schematic diagram of a D/A converter. Use resistance values whose ratios are multiples of 2. Explain the operation of the converter.
b) Give the schematic circuit of integrating type A/D converter and explain the operation of this system and derive expression for output voltage Vo. [5+5]

8.a) List the technological hazards.
b) Taking the example of a chemical industry indicate the measures taken to avoid the threat of toxic chemicals polluting the atmosphere.
c) In such cases indicate the role of training in mitigating the effects of pollution. [3+3+4]

**OR**

9.a) Compare the disasters fire flood and tsunami with respect to magnitude of disaster.
b) Are these to be considered as disasters in their own right or should they be treated as secondary effects? Discuss.
c) If they are considered as secondary effect, identify the likely primary cause or causes. [3+4+3]

10.a) List the activities considered for post disaster rehabilitation after an earthquake.
b) Bring out the importance of reconstruction of damaged buildings and the problems associated with it to ensure the dictum " Build back better"
c) What measures are taken to rehabilitate the population in a holistic way? Discuss. [3+4+3]

**OR**

11.a) Discuss the problems associated with sedimentation processes.
b) What pre disaster measures can reduce the impact of sedimentation problem?
c) Discuss how this aspect influences soil erosion and suggest corrective measures. [3+3+4]

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8.a) Draw the resistive model of a CMOS inverter and explain its behavior for LOW and HIGH outputs.

b) Design 1:8 demultiplexer using two 1:4 demultiplexer. [6+4]

**OR**

9.a) Explain sinking current and sourcing current of TTL output. Which of the above parameters decide the fan-out and how?

b) Design a full subtractor with NAND gates. [5+5]

10.a) Design an 8-bit parallel-in and serial-out shift register. Explain the operation of the above shift register with the help of timing waveforms.

b) Explain the functional behavior of Static RAM cell? Show the internal structure of 8×4 static RAM. [5+5]

**OR**

11.a) Design a 4-bit binary synchronous counter using 74×74.

b) Draw the internal structure of synchronous SRAM and explain the operation. [5+5]

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