Code No: 124DT

R15

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year II Semester Examinations, May - 2017
SWITCHING THEORY AND LOGIC DESIGN
(Electrical and Electronics Engineering)

Time: 3 Hours   Max. Marks: 75

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

PART – A   (25 Marks)

1.a) $AB+A'C+BC = AB+A'C$ represents which theorem.   [2]
  b) How do you obtain dual of an expression?   [3]
  c) What are don't cares?   [2]
  d) Explain the wired logic.   [3]
  e) Compare latch and flip flop.   [2]
  f) Explain the timing considerations of sequential circuits.   [3]
  g) What are the drawbacks of ripple counters?   [2]
  h) Explain about state diagram.   [3]
  i) List the capabilities of finite state machine.   [2]
  j) Explain about ASM chart.   [3]

PART – B   (50 Marks)

2.a) Convert the given Gray code number to equivalent binary 0010010111110010.
  b) Convert $(A0F9.0EBA98.0DC)_{16}$ to decimal, binary, octal.   [5+5]

OR

3.a) Simplify the following Boolean expressions using the Boolean theorems.
  (i) $(A+B+C)(B'+C) + (A+D)(A'+C)$ (ii) $(A+B)(A+B')(A'+B)$
  b) Why a NAND and NOR gates are known as universal gates? Simulate all the basic Gates.   [5+5]

4.a) Minimize the following expressions using K-map and realize using NAND Gates.
  $f = \sum m (1, 3, 5, 8, 9, 11, 15) + d (2, 13)$.
  b) Simplify the following boolean function using Tabular method.
  $F(A,B,C,D)=\sum m(0,1,2,5,7,8,9,10,13,15)$ [5+5]

OR

5. With the help of Logic diagram and Truth Table, discuss 8×1 Multiplexer and then realize $f(x,y,z) = \sum m(1,2,4,7)$ using 8×1 MUX as well as using 4×1 MUX.   [10]

6.a) Explain the operation JK master slave flip flop. Explain its truth table.
  b) Explain the realization of SR flip-flop, JK flip-flop using D flip-flop.   [5+5]

OR

7.a) Realize D-FF and T-FF using JK-FF. Draw the logic diagrams with their truth tables.
  b) Deduce the design procedure for sequential logic circuits and give the classification of sequential logic circuits.   [5+5]

8.a) Design and explain a synchronous MOD-12 down-counter using j-k flipflop.
  b) Design and explain a 4-bit ring counter using D-flip flops with relevant timing diagrams.   [5+5]

OR

9.a) Design a MOD-10 ripple counter.
  b) Design and construct MOD-5 synchronous counter using JK flip flops.   [5+5]

10.a) What are the capabilities and limitations of finite state machines? Discuss.
  b) Explain the procedure for state minimization using merger graph and merger table.   [5+5]

OR

11.a) Differentiate between an ASM chart and a conventional flow chart.
  b) Explain in detail the ASM technique of designing a sequential circuit.   [5+5]

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