Code No: 123BU **R15**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech II Year I Semester Examinations, November/December - 2016
SWITCHING THEORY AND LOGIC DESIGN
(Common to ECE, EIE, ETM)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

PART- A **(25 Marks)**

1.a) What are the different illegal states of BCD and XS-3? [2]
b) State and prove the included factor theorem. [3]
c) What is the prime implicant chart? [2]
d) Draw the full subtractor using X-OR and AOI gates. [3]
e) Define the Propagation delay time. [2]
f) Draw the conversion table of SR flipflop to JK flipflop. [3]
g) Define the ring counter. [2]
h) What are the applications of Shift register? [3]
i) What are the capabilities of FSM? [2]
j) Draw the state box and Decision box diagrams of ASM Charts. [3]

PART-B **(50 Marks)**

2.a) Convert the gray number 10110101 into:
i) Decimal ii) Octal iii) Hex
b) Perform the subtraction in BCD using 9's complement method for 592.6-887.9. [5+5]

OR

3.a) Derive the Boolean expression for a two input Ex-OR gate to realize with the two input NAND gates without using complemented variables and draw the circuit.
b) Expand (A+D′)(A+C′)(A′+B)(A′+B+C) into maxterms and minterms. [5+5]

4.a) Using the QM method, obtain the simplified expression for:
F=Σm (4,5,6,7,8,9,)+d(10,11,12,13,14,15).
b) Give the limitations of K-mapping method. [5+5]

OR

5.a) Design the 8:1 MUX for the given Boolean Expression f=Σm(1,3,4,11,12,13,14,15).
b) Design a combinational circuit to detect the decimal numbers 0,2,4,6 and 8 in a 4-bit XS-3 code input. [5+5]

6.a) Explain the generation of narrow spikes in the edge triggered flip-flops.
b) Draw and explain the operation of the Master Slave SR flip-flops with block diagram. [5+5]

OR

7.a) Derive the characteristic equation of JK flip-flop from the Excitation table.
b) Explain the Race around condition in flip-flops in detail. [5+5]

8.a) Design a Ring counter using shift register.
b) Define state, state diagram. Draw state diagram taking any one as an example. [5+5]

OR

9.a) Design a counter circuit for a mod-asynchronous counter using JK flip-flops.
b) Design a 3-bit up/down counter which counts up when the control signal M=1 and counts down when M=0. [5+5]

10. Draw the merger graph and obtain the set of Maximal compatibles for the incompletely specified sequential machine for given state table. [10]

PS	NS,Z	
	I1	I2
A	E,0	B,0
B	F,0	A,0
C	E,--	C,0
D	F,1	D,0
E	C,1	B,0
F	D,--	B,0

OR

11.a) Draw and explain the data path subsystem for weighing machine.
b) Draw the State diagram, state table and ASM chart for a D flip-flop. [5+5]

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