R16

Code No: 135AY

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech III Year I Semester Examinations, November/December - 2018
LINEAR AND DIGITAL IC APPLICATIONS
(Common to ECE, EIE)

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

(25 Marks)

1.a) Define the Op-Amp parameters: (i) Input offset voltage (V_{io}) and (ii) Input bias current, I_{io}. [2]
b) Discuss the features of voltage regulator. [3]
c) List out the application of 555 timer. [2]
d) Differentiate between active and passive filters. [3]
e) Give the conversion time for: (i) Counting ADC and (ii) successive approximation ADC. [2]
f) What are the disadvantages and advantages of weighted resister DAC? [3]
g) Classify the bipolar logic family by operation and give examples for each category. [2]
h) Draw the circuit of Totem-pole TTL NAND gate. [3]
i) Compare between SRAM and DRAM. [2]
j) Design a 8-bit parallel-in and serial-out shift register. [3]

PART - B

(50 Marks)

2.a) How an op-amp is used as a differentiator? Explain.
b) Explain the following terms: (i) Slew Rate. (ii) CMRR. [6+4]

OR

3.a) With neat pin diagram, explain about 78xx series regulator.
b) The IC 741 is connected as a non-inverting amplifier for a gain of 100. Determine the stability of the amplifier at this gain. [5+5]

4. Draw the circuit of an Astable multivibrator using 555 IC Timer and derive the expression for its frequency of oscillations. [10]

OR

5.a) Why is capture range always smaller than the lock in range? Explain.
b) Explain the operation of IC555 timer in monostable mode. Also mention its applications. [5+5]

6.a) An 8-bit ADC is capable of accepting an input unipolar (positive values only) voltage 0 to 10 V. Find, what the minimum value of 1LSB is and what the digital output code is if the applied input voltage is 5.4V?

b) Explain the working of 3-bit D to A converter using R-2R ladder network. [5+5]

OR

7.a) Explain the working of A to D converter using successive approximation method.

b) The logic levels used in an 8-bit R-2R ladder type DAC are logic'1' = +5 V and logic '0' = 0V. Find the output voltage for an input of 10110111. [5+5]

8.a) Design a 4 to 16 decoder using two 74X138 IC's.

b) Compare CMOS, TTL and ECL with reference to logic levels, DC noise margin, and propagation delay and fan-out. [5+5]

OR

9.a) Design a two bit comparator circuit and explain its operation.

b) Design the Binary to Gray code converter and explain its procedure in detail. [5+5]

10.a) With the help of timing waveforms, explain read and write operations of SRAM.

b) Explain the necessity of two-dimensional decoding mechanism in memories. Draw MOS transistor memory cell in ROM and explain the operation. [5+5]

OR

11.a) Explain different types of shift registers.

b) Explain the internal structure of a 128X1 ROM using two dimensional decoding. [5+5]

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