R16

Code No: 134AK

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year II Semester Examinations, 2019
COMPUTER ORGANIZATION

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.

Q.No	Question	Bloom's Level
	PART – A (25 Marks)	
1 a	Draw the block diagram of the digital computer and explain.	**L1 / L2**
b	Explain each of the basic computer registers and memory	**L2**
c	Show the register organization of the 8086.	**L1 / L2**
d	Briefly explain how the instructions AAA, AAS and DAA work in 8086. Give an example for each.	**L2**
e	List the advantages of assembly language programming over machine language.	**L1 / L2**
f	Explain the function of the following signals of 8086. *i) ALE ii) DT/$\bar{R}$ iii) $\overline{TEST}$*	**L2**
g	List 4 peripheral devices that produce an acceptable output for a person to understand.	**L1 / L2**
h	Draw the block diagram to show the hardware for signed-magnitude addition and subtraction and explain.	**L2**
i	Illustrate memory hierarchy in a computer system using a block diagram.	**L1 / L2**
j	A nonpipelined system takes 50ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved?	**L2**
	PART – B (50 Marks)	
2	Distinguish between a direct and an indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into processor register A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers and an address part. Analyze and find how many bits are there in the operation code, the register code part and the address part? Analyze and draw the instruction word format and indicate the number of bits in each part. Analyze and find how many bits are there in the data and address inputs of the memory?	**L3 / L4**
	OR	
3	Draw the block diagram of the control unit of a basic computer. With the help of this diagram show the time relationship of the control signals assuming that SC is cleared to 0 at time T_3 if control signal C_7 is active. C_7T_3: SC←0 C_7 is activated with the positive clock transition associated with T_1	**L3 / L4**
4	With a neat diagram explain the 8086 architecture.	**L5`**

	Determine the physical address given that the segment address is 1005H and the offset is 5555H.	
	OR	
5	The contents of different registers are given below. Determine effective addresses for direct, register indirect, register relative, based indexed and relative based indexed addressing modes. Offset (displacement) = 5000H [AX]-1000H, [BX]-2000H, [SI]-3000H, [DI]-4000H, [BP]-5000H, [SP]-6000H, [CS]-0000H, [DS]-1000H, [SS]-2000H, [IP]-7000H.	**L5**
6	Develop the flowchart and an assembly language program to add the contents of the memory location 2000H:0500H to contents of 3000H:0600H and store the result in 5000H:7000H.	**L3 / L4**
	OR	
7	Develop a program to change a sequence of sixteen 2-byte numbers from ascending to descending order.The numbers are stored in the data segment. Stoe the new series at addresses starting from 6000H. Use the LIFO property of the stack.	**L3 / L4**
8	Develop an algorithm in flowchart form for addition and subtraction of fixed-point binary numbers in signed-magnitude representation with the magnitudes subtracted by the two microoperations $A \leftarrow \bar{A}$ *and* $EA \leftarrow A + B$	**L3 / L4**
	OR	
9	A commercial interface unit uses the following names for the handshake lines associated with the transfer of data from the I/O device into the interface unit. The interface input handshake line is labeled STB(strobe) and the interface output handshake line is labeled IBF (input buffer full). A low-level signal on STB loads data from the I/O bus into the interface data register. A high-level signal on IBF indicates that data item has been accepted by the interface.IBF goes low after an I/O read signal from the CPU when it reads the contents of the data register. Construct a block diagram showing the CPU, the interface and the I/O device together with interconnections among the 3 units. Construct a timing diagram for the handshaking transfer.	**L3 / L4**
10 a	Indentify whether the following constitute a control, status or data transfer commands: Skip next instruction if flag is set. Seek a given record on a magnetic disk. Check if I/O device is ready. Move printer paper to beginning of next page. Read interface status register.	**L2**
b	Construct a diagram for a 4X4 omega switching network. Show the switch setting required to connect input 3 to output 1.	**L3 / L4**
	OR	
11 a	In certain scientific computations it is necessary to perform the arithmetic operation $(A_i + B_i)(C_i + D_i)$ with a stream of numbers. Specify a pipeline configuration to carry out this task. Show the contents of all registers in pipeline for I = 1 through 6.	**L2**
b	With a neat figure show how memory is connected to the CPU to give a memory capacity of 4096 bytes of RAM and 4096 bytes of ROM. Construct the memory-address map and indicate what size decoders are needed.	**L3 / L4**