Code No: 134CC **R16**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year II Semester Examinations, May - 2019
PULSE AND DIGITAL CIRCUITS
(Common to ECE, ETM)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A

(25 marks)

1.a) Show how an RC circuit works as a high pass filter. [2]
b) Illustrate the output voltage and loop current waveform of a RC low pass circuit for a step input and indicate the time constant. [3]
c) The input to the clipper circuit is $V_m Sin\omega t$. Illustrate the input and output waveform with respect to transfer characteristics shown in figure 1. [2]

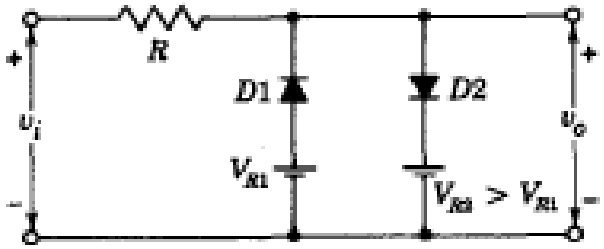

Figure: 1

d) Explain the working of an emitter coupled clipper. [3]
e) Illustrate the capacitive load transistor switch circuit and explain its working. [2]
f) Illustrate the circuit of transistor non-saturating switch and explain. [3]
g) What is bistable multivibrator? What are the different names of it? [2]
h) Define Sweep speed error and displacement error. [3]
i) Illustrate the diode OR circuit for negative logic and give its truth table. [2]
j) What is sampling gate? How it is different from logic gate? [3]

PART-B

(50 Marks)

2. A symmetrical square wave whose average value is zero has a peak to peak amplitude of 20V and a period of 2μsec. This waveform is applied to a low-pass RC circuit whose 3-dB frequency is $1/2\pi$ MHz. Determine and sketch the steady state output waveform. In particular, what is the peak-to-peak output amplitude? [10]

OR

3. A square wave whose peak-to-peak amplitude is 2V extends ±1V wrt ground. The duration of the positive section is 0.1 sec and that of the negative section is 0.2 sec. If this waveform is impressed upon an RC integrating circuit whose time constant is 0.2 sec, Evaluate the steady state maximum and minimum values of the output waveform. [10]

4. The diodes are ideal.
a) Write the transfer characteristic equation.
b) Plot v_o against v_i indicating all intercepts, slopes and voltages.
c) Determine and sketch v_o if $v_i = 40\sin\omega t$. Indicate all voltage levels. (Figure 6) [10]

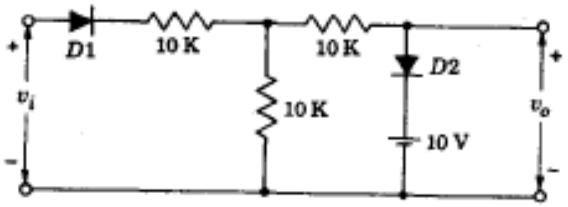

Figure: 2

OR

5. The ramp type signal is applied to the circuit shown in figure 3 which has R_f=100Ω, V_r=0, R_r=∞ and R=10KΩ. The capacitor C is arbitrarily large. Develop the output waveform, calculate all voltage levels and voltage across the capacitor, if R_s=0 and 100Ω. [10]

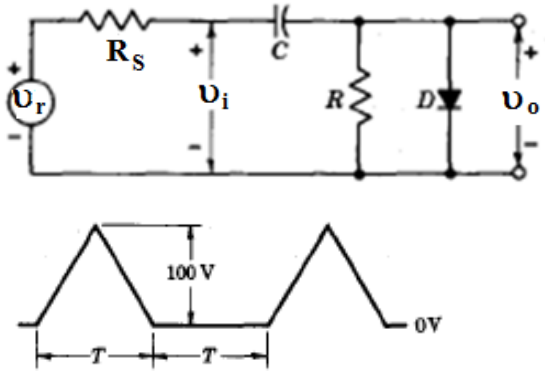

Figure: 3

6. A reverse biasing voltage of 100V is applied through a resistor R to a type of diode 1N270 diode. The diode operates at 25^0C. Determine the diode current and voltage for the cases R=10MΩ, 1MΩ and 100KΩ.(Figure 4) [10]

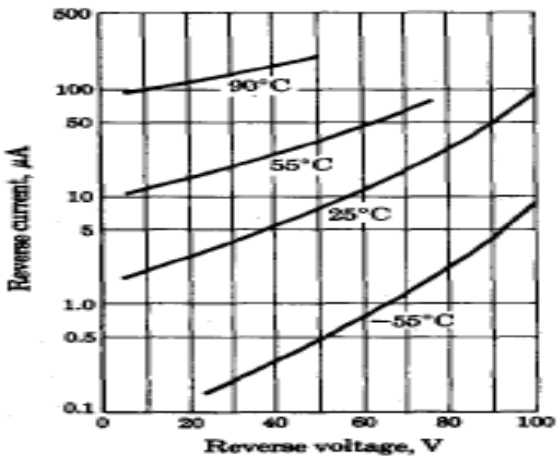

Figure: 4

OR

7. In the below circuit V_{CC}=10V, R_C=500Ω, R=40K Ω, C=0.1μF, R_{s1}=R_{s2}=10K Ω, V=10V and T_2=1.0msec. Determine the all the marked voltages assuming rbb′=100 Ω.(Figure 5) [10]

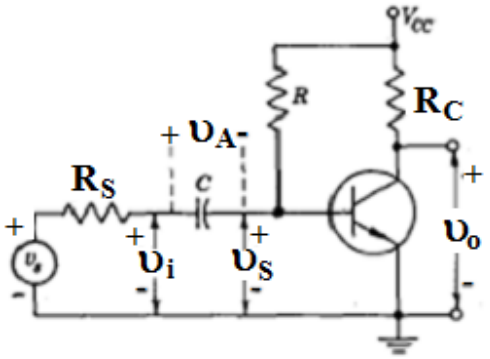

Figure: 5

8. The fixed bias binary shown below figure 6 uses npn silicon transistors with h_{FE}=20. The circuit parameters are V_{CC}=12V, V_{BB}=3V, R_C=1K, R_1=5KΩ and R_2=10KΩ. Test that one transistor is in cut-off and the other is in saturation and evaluate the stable state current and voltages if $V_{CE(sat)}$ =0.4V and $V_{BE(sat)}$=0.8V. [10]

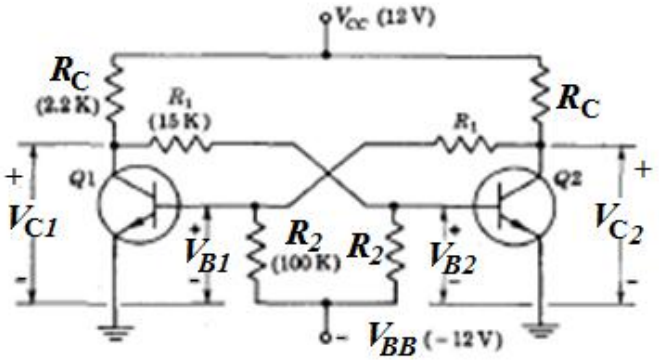

Figure: 6

OR

9. Germanium transistors with $(h_{FE})_{min}$=40 are used in the fixed bias flip-flop with collector catching diodes. The circuit parameters are V_{CC}=18V, V=V_{BB}=6V, R_C=1.5KΩ, R_i=5KΩ and R_2=25KΩ. Neglect the voltage drop across a forward biased junction. Verify that if one transistor is cut-off, the other is in saturation.(Figure 7) [10]

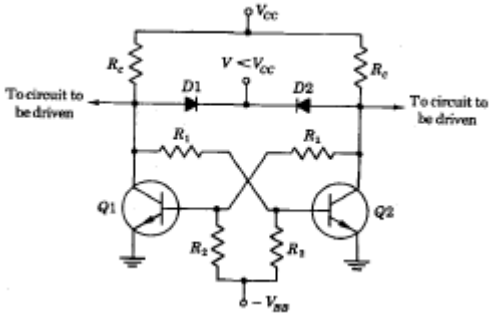

Figure: 7

10.a) Explain unidirectional sampling gate.

b) In the gate circuit shown below figure 8, R_L=10KΩ and is shunted by a capacitance C_1=10pF. The gate signal is a symmetrical square wave of frequency 1MHZ which makes excursions between -35 to 0V. The output impedance of the square wave source is 500Ω. If no more than 2V of the input signal is to be fed back into the control-signal source, what is R_1? [5+5]

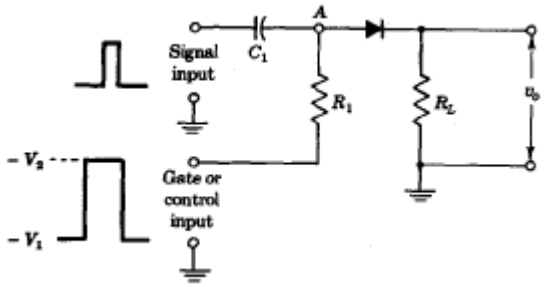

Figure: 8

OR

11.a) Design the circuit of three input positive NAND gate and explain.

b) Consider a two input positive-logic diode OR gate with the diodes reversed and V_r=0. The inputs are the square waves v_1 and v_2 indicated. Determine and sketch the output waveform if the ratio of the amplitude of v_1 and v_2 is: i) 2 ii) 0.5. Assume ideal diodes. (Figure9) [5+5]

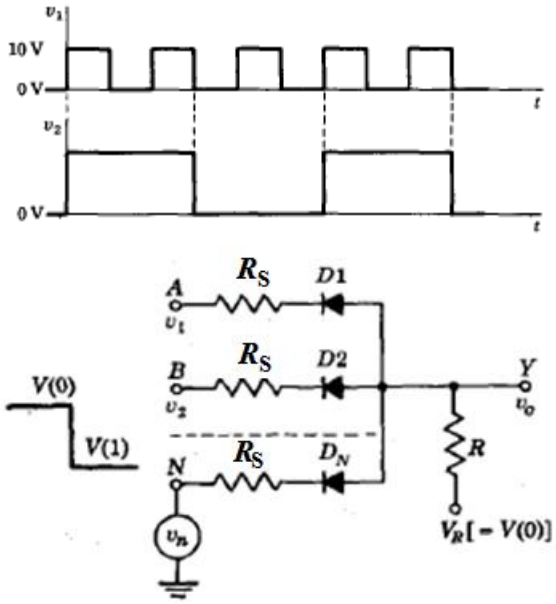

Figure: 9

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