

**R16****Code No: 134CF****JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD****B.Tech II Year II Semester Examinations, May - 2019****SWITCHING THEORY AND LOGIC DESIGN****(Common to EEE, ECE, MCT, ETM)****Time: 3 Hours****Max. Marks: 75****Note:** This question paper contains two parts A and B.

Part A is compulsory which carries 25 marks. Answer all questions in Part A.

Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

**PART - A****(25 marks)**

- 1.a) Perform the following conversions  $(476.64)_{10} = ( )_2 = ( )_8$ . [2]
- b) Perform the following operation using 2's complement method  $1111.10 - 0101.11$ . [3]
- c) Define Multiplexer. Explain in brief about 2:1 Mux. [2]
- d) Explain the procedure to construct the 3 variable K-map with an example. [3]
- e) Derive the characteristic equations of D and T flipflop. [2]
- f) Give the differences between latches and flipflops. [3]
- g) Define state diagram. [2]
- h) List the features of sequential circuits. [3]
- i) What are finite state machines? [2]
- j) List the limitations of finite state machines. [3]

**PART - B****(50 Marks)**

2. Design and realize the 3 bit binary to unit distance code using NOR gates. [10]
- OR**
3. Simplify and realize the following Boolean expression using logic gates.
    - a)  $Y = AB + A'C + BC$
    - b)  $Y = (A + B' + C')(A + B' + C)$  [5+5]
  4. Design a digital system to compare two binary numbers of 1 bit by using logic gates. [10]
- OR**
5. Realize 3:8 maxterm generator using 2:4 maxterm generators. Using the same, Design a system to provide the difference of two numbers. Use external two input gates only. [10]
  6. Explain master slave JK flipflop with neat timing diagram. [10]
- OR**
7. Explain the principle of Universal shift Register(USR). Using the same, design 4-bit, mod-8 twisted ring counter. [10]

8. Design a digital system using data flipflops to monitor the status of the bookrack of maximum occupancy 10. The number of books available in the bookrack on a daily basis for the following conditions over a week.
- a) On Monday, there were 10 books.
  - b) On Tuesday, 2 books were removed and donated to near by library.
  - c) On Wednesday, one book is added to the bookrack.
  - d) Next day, 3 books were removed from the rack and given it to neighbour.
  - e) On Friday, one book was taken out for reading.
  - f) On Saturday, neighbour returned only two books.
- All the remaining books were taken out on Sunday to clean the rack. [10]

**OR**

- 9.a) Discuss about the approaches of designing synchronous sequential finite state machines.
- b) Design a digital controller for the state table shown below using sequential component as single input data flip flop. [5+5]

| Present state | Next state, Output(z) |            |
|---------------|-----------------------|------------|
|               | Input(x)=0            | Input(x)=1 |
| A             | C,0                   | B,1        |
| B             | D,0                   | D,0        |
| C             | C,1                   | A,0        |
| D             | A,1                   | A,0        |

10. Draw the state diagram of a Mealy machine that produces a 1 output if there have been four or more consecutive 1 inputs or two or more consecutive 0 inputs. [10]

**OR**

- 11.a) With a neat block diagram, explain the moore model of a clocked synchronous sequential circuit.
- b) Illustrate partition techniques in sequential circuits. [5+5]

---ooOoo---