JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. TECH IN DIGITAL ELECTRONICS AND COMMUNICATION ENGINEERING/ DIGITAL ELECTRONICS AND COMMUNICATION SYSTEMS

EFFECTIVE FROM ACADEMIC YEAR 2017- 18 ADMITTED BATCH

COURSE STRUCTURE AND SYLLABUS

I Semester

Category	Course Title	Int. marks	Ext. marks	L	T	P	C
PC-1	Advanced Digital System Design	25	75	4	0	0	4
PC-2	Coding Theory and Techniques	25	75	4	0	0	4
PC-3	Broadband Communications	25	75	4	0	0	4
PE-1	Real Time Operating Systems Image and Video Processing Spread Spectrum Communications	25	75	**3**	0	0	3
PE-2	Advanced Computer Architecture Advanced Digital Signal Processing Optical Communications and Networks	25	75	**3**	0	0	3
OE-1	***Open Elective – I**	25	75	3	0	0	3
Laboratory I	Digital System Design Lab	25	75	0	0	3	2
Seminar I	Seminar	100	0	0	0	3	2
Total		**275**	**525**	**21**	**0**	**6**	**25**

II Semester

Category	Course Title	Int. marks	Ext. marks	L	T	P	C
PC-4	Design of Fault Tolerant Systems	25	75	4	0	0	4
PC-5	Detection and Estimation Theory	25	75	4	0	0	4
PC-6	Wireless Communications and Networks	25	75	4	0	0	4
PE-3	System on Chip Architecture Software Defined Radio Cellular and Mobile Communications	25	75	**3**	0	0	3
PE4	Network Security And Cryptography Digital Signal Processors and Architectures EMI / EMC	25	75	**3**	0	0	3
OE-2	***Open Elective – II**	25	75	3	0	0	3
Laboratory II	Wireless Communications and Networks Lab	25	75	0	0	3	2
Seminar II	Seminar	100	0	0	0	3	2
Total		**275**	**525**	**21**	**0**	**6**	**25**

III Semester

Course Title	Int. marks	Ext. marks	L	T	P	C
Technical Paper Writing	100	0	0	3	0	2
Comprehensive Viva-Voce	0	100	0	0	0	4
Project work Review II	100	0	0	0	22	8
Total	**200**	**100**	0	**3**	22	**14**

IV Semester

Course Title	Int. marks	Ext. marks	L	T	P	C
Project work Review III	100	0	0	0	24	8
Project Evaluation (Viva-Voce)	0	100	0	0	0	16
Total	**100**	**100**	**0**	**0**	**24**	**24**

***Open Elective subjects must be chosen from the list of open electives offered by OTHER departments.**

 # For Project review I, please refer 7.10 in R17 Academic Regulations.

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M. TECH. I YEAR I SEMESTER
DIGITAL ELECTRONICS AND COMMUNICATION ENGINEERING/ DIGITAL ELECTRONICS AND COMMUNICATION SYSTEMS

ADVANCED DIGITAL SYSTEM DESIGN (PC-1)

UNIT - I
Processor Arithmetic: Two's Complement Number System - Arithmetic Operations; Fixed point Number System; Floating Point Number system - IEEE 754 format, Basic binary codes.

UNIT - II
Combinational circuits: CMOS logic design, Static and dynamic analysis of Combinational circuits, timing hazards. Functional blocks: Decoders, Encoders, Three-state devices, Multiplexers, Parity circuits, Comparators, Adders, Subtractors, Carry look-ahead adder – timing analysis. Combinational multiplier structures.

UNIT - III
Sequential Logic - Latches and Flip-Flops, Sequential logic circuits - timing analysis (Set up and hold times), State machines - Mealy & Moore machines, Analysis, FSM design using D Flip-Flops, FSM optimization and partitioning; Synchronizers and metastability. FSM Design examples: Vending machine, Traffic light controller, Washing machine.

UNIT - IV
Subsystem Design using Functional Blocks (1) - Design (including Timing Analysis) of different logical blocks of varying complexities involving mostly combinational circuits:

- ALU
- 4-bit combinational multiplier
- Barrel shifter
- Simple fixed point to floating point encoder
- Dual Priority encoder
- Cascading comparators

UNIT - V
Subsystem Design using Functional Blocks (2) - Design, (including Timing Analysis) of different logical blocks of different complexities involving mostly sequential circuits:

- Pattern (sequence) detector
- Programmable Up-down counter
- Round robin arbiter with 3 requesters
- Process Controller
- FIFO

TEXT BOOKS:

1. John F. Wakerly, “Digital Design”, Prentice Hall, 3rd Edition, 2002

*Note1: VHDL and ABEL are not part of this course.
*Note2: SSI & MSI ICs listed in data books are not part of this course.

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M. TECH. I YEAR I SEMESTER
DIGITAL ELECTRONICS AND COMMUNICATION ENGINEERING/ DIGITAL ELECTRONICS AND COMMUNICATION SYSTEMS

CODING THEORY AND TECHNIQUES (PC-2)

UNIT – I

Coding for Reliable Digital Transmission and storage: Mathematical model of Information, A Logarithmic Measure of Information, Average and Mutual Information and Entropy, Types of Errors, Error Control Strategies.

Linear Block Codes: Introduction to Linear Block Codes, Syndrome and Error Detection, Minimum Distance of a Block code, Error-Detecting and Error-correcting Capabilities of a Block code, Standard array and Syndrome Decoding, Probability of an undetected error for Linear Codes over a BSC, Hamming Codes. Applications of Block codes for Error control in data storage system

UNIT - II

Cyclic Codes : Description, Generator and Parity-check Matrices, Encoding, Syndrome Computation and Error Detection, Decoding ,Cyclic Hamming Codes, Shortened cyclic codes, Error-trapping decoding for cyclic codes, Majority logic decoding for cyclic codes.

UNIT – III

Convolutional Codes: Encoding of Convolutional Codes, Structural and Distance Properties, maximum likelihood decoding, Sequential decoding, Majority- logic decoding of Convolution codes. Application of Viterbi Decoding and Sequential Decoding, Applications of Convolutional codes in ARQ system.

UNIT – IV

Turbo Codes: LDPC Codes- Codes based on sparse graphs, Decoding for binary erasure channel, Log-likelihood algebra, Brief propagation, Product codes, Iterative decoding of product codes, Concatenated convolutional codes- Parallel concatenation, The UMTS Turbo code, Serial concatenation, Parallel concatenation, Turbo decoding

UNIT - V

Space-Time Codes: Introduction, Digital modulation schemes, Diversity, Orthogonal space- Time Block codes, Alamouti's schemes, Extension to more than Two Transmit Antennas, Simulation Results, Spatial Multiplexing : General Concept, Iterative APP Preprocessing and Per-layer Decoding, Linear Multilayer Detection, Original BLAST Detection, QL Decomposition and Interface Cancellation, Performance of Multi – Layer Detection Schemes, Unified Description by Linear Dispersion Codes.

TEXT BOOKS:

1. Shu Lin, Daniel J.Costello,Jr, "Error Control Coding- Fundamentals and Applications", Prentice Hall.
2. Man Young Rhee, "Error Correcting Coding Theory", 1989, McGraw-Hill Publishing.

REFERENCE BOOKS:

1. Bernard Sklar, "Digital Communications-Fundamental and Application", PE.
2. John G. Proakis, "Digital Communications", 5th ed., 2008, TMH.
3. Salvatore Gravano, "Introduction to Error Control Codes", Oxford

4. Todd K.Moon, “Error Correction Coding-Mathematical Methods and Algorithms”, 2006, Wiley India.
5. Ranjan Bose, “Information Theory, Coding and Cryptography”, 2nd Edition, 2009, TMH.

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M. TECH. I YEAR I SEMESTER
DIGITAL ELECTRONICS AND COMMUNICATION ENGINEERING/ DIGITAL ELECTRONICS AND COMMUNICATION SYSTEMS

BROADBAND COMMUNICATIONS (PC-3)

UNIT – I
ISDN: Switching Techniques, Principles of ISDN, Architecture, ISDN standards, I-series, Recommendations, Transmission structure, User network interface, ISDN protocol, architecture, ISDN connections, Addressing, Interworking

UNIT – II
B-ISDN: Architecture and standards, B-ISDN Services, Conversational, Messaging, Retrieval, Distribution, Business and Residential requirements, B-ISDN protocols User plane, Control plane, Physical layer, Line coding, Transmission structure, SONET- Requirement, Signal Hierarchy, System Hierarchy.

UNIT – III
ATM: Overview, Virtual channels, Virtual paths, VP and VC switching, ATM cells, Header format, Generic flow control, Header error control, Transmission of ATM cells, Adaptation layer, AAL services and protocols.

UNIT – IV
ATM switching: ATM switching building blocks, ATM cell processing in a switch, Matrix type switch, Input, Output buffering, Central buffering, Performance aspects of buffering switching networks.

UNIT – V
ATM Traffic and congestion Control: Requirements for ATM Traffic and Congestion Control, Cell-Delay Variation, ATM Service Categories, Traffic and Congestion Control Framework, Traffic Control, Congestion Control

Text Book:

1. William Stallings, “ISDN and Broadband ISDN with Frame Relay and ATM Prentice”, Hall, 4th Edition

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DIGITAL ELECTRONICS AND COMMUNICATION ENGINEERING/ DIGITAL ELECTRONICS AND COMMUNICATION SYSTEMS

REAL TIME OPERATING SYSTEMS (PE-1)

UNIT – I
Introduction: Introduction to UNIX/LINUX, Overview of Commands, File I/O, (open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT -II
Real Time Operating Systems: Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency.
Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

UNIT -III
Objects, Services and I/O: Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

UNIT -IV
Exceptions, Interrupts and Timers: Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT -V
Case Studies of RTOS: RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, and Tiny OS, and Android OS.

TEXT BOOKS:
1. Qing Li, “Real Time Concepts for Embedded Systems”, 2011, Elsevier.

REFERENCE BOOKS
1. Rajkamal, “Embedded Systems- Architecture, Programming, and Design”, 2007, TMH.
2. W. Richard Stevens, Stephan A. Rago, “Advanced UNIX Programming”, 2006, 2nd Edition, Pearson.
3. Dr. Craig Hollabaugh, “Embedded Linux: Hardware, Software and Interfacing”, 2008, 1st Edition, Pearson.

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DIGITAL ELECTRONICS AND COMMUNICATION ENGINEERING/ DIGITAL ELECTRONICS AND COMMUNICATION SYSTEMS

IMAGE AND VIDEO PROCESSING (PE-1)

UNIT –I

Fundamentals of Image Processing and Image Transforms: Basic steps of Image Processing System Sampling and Quantization of an image, Basic relationship between pixels.

Image Segmentation: Segmentation concepts, Point, Line and Edge Detection, Thresholding, Region based segmentation.

UNIT –II

Image Enhancement: Spatial domain methods: Histogram processing, Fundamentals of Spatial filtering, Smoothing spatial filters, Sharpening spatial filters.

Frequency domain methods: Basics of filtering in frequency domain, Image smoothing, Image sharpening, Selective filtering.

UNIT –III

Image Compression: Image compression fundamentals - Coding Redundancy, Spatial and Temporal redundancy, Compression models: Lossy & Lossless, Huffman coding, Bit plane coding, Transform coding, Predictive coding, Wavelet coding, Lossy Predictive coding, JPEG Standards.

UNIT -IV

Basic Steps of Video Processing: Analog Video, Digital Video. Time-Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video signals, Filtering operations.

UNIT –V

2-D Motion Estimation: Optical flow, General Methodologies, Pixel Based Motion Estimation, Block-Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi resolution motion estimation, Waveform based coding, Block based transform coding, Predictive coding, Application of motion estimation in Video coding.

TEXT BOOKS:

1. Gonzaleze and Woods, “Digital Image Processing”, 3rd Edition, Pearson.
2. Yao Wang, Joem Ostermann and Ya–quin Zhang, “Video Processing and Communication”, 1st Edition, PH Int.

REFRENCE BOOKS:

1. Gonzaleze and Woods,” Digital Image Processing using MATLAB”, 2nd Edition, Mc Graw Hill Education, 2010
2. Milan Sonka, Vaclan Hlavac, “Image Processing Analysis, and Machine Vision”, 3rd Edition, CENGAGE, 2008
3. A Murat Tekalp, “Digital Video Processing “, Person, 2010
4. S.Jayaraman, S.Esakkirajan, T.Veera Kumar, “Digital Image Processing”, TMH, 2009

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DIGITAL ELECTRONICS AND COMMUNICATION ENGINEERING/ DIGITAL ELECTRONICS AND COMMUNICATION SYSTEMS

SPREAD SPECTRUM COMMUNICATIONS (PE-1)

UNIT -I

Introduction to Spread Spectrum Systems: Fundamental Concepts of Spread Spectrum Systems, Pseudo Noise Sequences, Direct Sequence Spread Spectrum, Frequency Hop Spread Spectrum, Hybrid Direct Sequence Frequency Hop Spread Spectrum, Code Division Multiple Access.

Binary Shift Register Sequences for Spread Spectrum Systems: Introduction, Definitions, Mathematical Background and Sequence Generator Fundamentals, Maximal Length Sequences, Gold Codes.

UNIT -II

Code Tracking Loops: Introduction, Optimum Tracking of Wideband Signals, Base Band Delay-Lock Tracking Loop, Tau-Dither Non- Coherent Tracking Loop, Double Dither Non-Coherent Tracking Loop.

UNIT -III

Initial Synchronization of the Receiver Spreading Code: Introduction, Problem Definition and the Optimum Synchronizer, Serial Search Synchronization Techniques, Synchronization using a Matched Filter, Synchronization by Estimated the Received Spreading Code.

UNIT -IV

Cellular Code Division Multiple Access (CDMA) Principles: Introduction, Wide Band Mobile Channel, The Cellular CDMA System, Single User Receiver in a Multi User Channel, CDMA System Capacity,

Multi-User Detection in CDMA Cellular Radio: Optimal Multi-User Detection, Linear Suboptimal Detectors, Interference Combat Detection Schemes, Interference Cancellation Techniques.

UNIT -V

Performance of Spread Spectrum Systems in Jamming Environments: Spread Spectrum Communication System Model, Performance of Spread Spectrum Systems without Coding.

Performance of Spread Spectrum Systems with Forward Error Correction: Elementary Block Coding Concepts, Optimum Decoding Rule, Calculation of Error Probability, Elementary Convolution Coding Concepts, Viterbi Algorithm, Decoding and Bit-Error Rate.

TEXT BOOKS:

1. Rodger E Ziemer, Roger L. Peterson and David E Borth, “Introduction to Spread Spectrum Communication”, Pearson, 1st Edition, 1995.
2. Mosa Ali Abu-Rgheff – “Introduction to CDMA Wireless Communications”, Elsevier Publications, 2008.

REFERENCE BOOKS:

1. George R. Cooper, Clare D. Mc Gillem, “Modern Communication and Spread Spectrum”, McGraw Hill, 1986.
2. Andrew j. Viterbi - “CDMA: Principles of spread spectrum communication”, Pearson Education, 1st Edition, 1995.
3. Kamilo Feher, “Wireless Digital Communications”, PHI, 2009.

4. Andrew Richardson, “WCDMA Design Handbook”, Cambridge University Press, 2005.
5. Steve Lee, “Spread Spectrum CDMA”, McGraw Hill, 2002.

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M. TECH. I YEAR I SEMESTER
DIGITAL ELECTRONICS AND COMMUNICATION ENGINEERING/ DIGITAL ELECTRONICS AND COMMUNICATION SYSTEMS

ADVANCED COMPUTER ARCHITECTURE (PE-2)

UNIT -I

Fundamentals of Computer Design: Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, Measuring and reporting performance, Quantitative principles of computer design, Amdahl's law.

Instruction set principles and examples- Introduction, Classifying instruction set- Memory addressing-type and size of operands, Operations in the instruction set.

UNIT –II

Pipelines: Introduction, Basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe lined RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.

Memory Hierarchy Design: Introduction, Review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT -III

Instruction Level Parallelism the Hardware Approach: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.

ILP Software Approach: Basic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT –IV

Multi Processors and Thread Level Parallelism: Multi Processors and Thread level Parallelism-Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT –V

Inter Connection and Networks: Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

Intel Architecture: Intel IA-64 ILP in embedded and mobile markets Fallacies and pit falls.

TEXT BOOKS:

1. John L. Hennessy, David A. Patterson - Computer Architecture: A Quantitative Approach, 3rd Edition, an Imprint of Elsevier.

REFERENCE BOOKS:

1. John P. Shen and Miikko H. Lipasti, "Modern Processor Design : Fundamentals of Super Scalar Processors", 2002, Beta Edition, McGrawHill
2. Kai Hwang, Faye A.Brigs., "Computer Architecture, and Parallel Processing", Mc Graw Hill.
3. Dezso Sima, Terence Fountain, Peter Kacsuk , "Advanced Computer Architecture - A Design Space Approach", Pearson Education.

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ADVANCED DIGITAL SIGNAL PROCESSING (PE-2)

UNIT –I

Review of DFT, FFT, IIR Filters and FIR Filters: Multi Rate Signal Processing: Introduction, Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Multistage Implementation of Sampling Rate Conversion, Filter design & Implementation for sampling rate conversion.

UNIT –II

Applications of Multi Rate Signal Processing: Design of Phase Shifters, Interfacing of Digital Systems with Different Sampling Rates, Implementation of Narrow Band Low Pass Filters, Implementation of Digital Filter Banks, Sub-band Coding of Speech Signals, Quadrature Mirror Filters, Trans-multiplexers, Over Sampling A/D and D/A Conversion.

UNIT -III

Non-Parametric Methods of Power Spectral Estimation: Estimation of spectra from finite duration observation of signals, Non-parametric Methods: Bartlett, Welch & Blackman-Tukey methods, Comparison of all Non-Parametric methods

UNIT –IV

Implementation of Digital Filters: Introduction to filter structures (IIR & FIR), Frequency sampling structures of FIR, Lattice structures, Forward prediction error, Backward prediction error, Reflection coefficients for lattice realization, Implementation of lattice structures for IIR filters, Advantages of lattice structures.

UNIT –V

Parametric Methods of Power Spectrum Estimation: Autocorrelation & Its Properties, Relation between auto correlation & model parameters, AR Models - Yule-Walker & Burg Methods, MA & ARMA models for power spectrum estimation, Finite word length effect in IIR digital Filters – Finite word-length effects in FFT algorithms.

TEXT BOOKS:

1. J.G.Proakis & D. G. Manolakis," Digital Signal Processing: Principles, Algorithms & Applications", 4th Edition, PHI.
2. Alan V Oppenheim & R. W Schaffer," Discrete Time Signal Processing", PHI.
3. Emmanuel C. Ifeacher, Barrie. W. Jervis, "DSP – A Practical Approach", 2nd Edition, Pearson Education.

REFERENCE BOOKS:

1. S. M .Kay," Modern Spectral Estimation: Theory & Application", 1988, PHI.
2. P.P. Vaidyanathan "Multi Rate Systems and Filter Banks", Pearson Education.
3. S. Salivahanan, A. Vallavaraj, C. Gnanapriya, "Digital Signal Processing", 2000,TMH
4. S. Lawrence Marple, Jr. "Digital Spectral Analysis: with Applications", 1987, Prentice Hall.

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OPTICAL COMMUNICATIONS AND NETWORKS (PE-2)

UNIT I
Optical Fibers: Structures, waveguiding and Fabrication: Nature of Light, Basic optical laws and definitions, Single mode fibers, Graded index fiber structure, Attenuation, Signal Dispersion in fibers.
Optical Sources- LEDs, Laser Diodes, Line Coding.

UNIT II
Photo detectors: Photo detector Noise, Detector Response Time, Avalanche Multiplication Noise.
Optical Receiver Operation: Fundamental receiver operation, Digital receiver performance, Eye diagrams.
WDM Concepts and Components: Passive optical Couplers, Isolators and Circulators

UNIT III
Digital Links: Point to point links, power penalties, error control, Coherent detection, Differential Quadrature Phase Shift Keying.
Analog Links: Carrier to noise ration, Multichannel Transmission Techniques, RF over Fiber, Radio over fiber links, Microwave Photonics.

UNIT IV
Optical Networks: Network Concepts, Network Topologies, SONET/SDH, High speed lightwave links, Optical add/ Drop Multiplexing, Optical Switching, WDM Network, Passive Optical Networks, IP Over DWDM, Optical Ethernet, Mitigation of Transmission Impairments

UNIT V
Performance Measurement and Monitoring: Measurement standards, Basic Test Equipment, Optical power measurement, Optical fiber characterization, Eye diagram tests, optical time domain reflectometer, optical performance monitoring, optical fiber system performance measurements.

TEXTBOOKS:
1. Gerd Keiser, “Optical Fiber Communications”, 5th Edition, Mc Graw Hill.
2. Rajeev Ramaswamy and Kumar N Sivarajan, “Optical Networks: A Practical Perspective”, 2nd Ed., 2004, Elsevier Morgan Kaufmann Publishers (An imprint of Elsevier).

REFERENCE BOOKS:
1. John. M. Senior, “Optical Fiber Communications: Principles and Practice”, 2nd Ed, 2000, PE.
2. Harold Kolimbris, “Fiber Optic Communication”, 2nd Ed, 2004, PEI
3. Uyless Black, “Optical Networks: Third Generation Transport Systems”, 2nd Ed, 2009, PEI
4. Govind Agarwal, “Optical Fiber Communications”, 2nd Ed, 2004, TMH.
5. S. C. Gupta, “Optical Fiber Communications and its Applications”, 2004, PHI

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DIGITAL SYSTEM DESIGN LAB

Part –I

Programming can be done using any complier. Down load the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels) and logic analyzer apart from verification by simulation with any of the front end tools.

1. HDL code to realize all the logic gates
2. Design and Simulation of adder, Serial Binary Adder, Multi Precession Adder, Carry
3. Look Ahead Adder.
4. Design of 2-to-4 decoder
5. Design of 8-to-3 encoder (without and with parity)
6. Design of 8-to-1 multiplexer
7. Design of 4 bit binary to gray converter
8. Design of Multiplexer/ Demultiplexer, comparator
9. Design of Full adder using 3 modeling styles
10. Design of flip flops: SR, D, JK, T
11. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset) or any sequence counter
12. Design of a N- bit Register of Serial- in Serial –out, Serial in parallel out, Parallel in
13. Serial out and Parallel in Parallel Out.
14. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
15. Design of 4- Bit Multiplier, Divider.
16. Design of ALU to Perform – ADD, SUB, AND-OR, 1's and 2's Compliment,
17. Multiplication, and Division.
18. Design of Finite State Machine.
19. Implementing the above designs on Xilinx/Altera/Cypress/equivalent based FPGA/CPLD kits .

Part –II

1. Static and Dynamic Characteristics of CMOS Inverter
2. Implementation of EX-OR gate using complementary CMOS, Psedo-NMOS, Dynamic and domino logic style
3. Implementation of Full Adder using Transmission Gates