**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**

**M. TECH IN DIGITAL SYSTEMS & COMPUTER ELECTRONICS.**
**EFFECTIVE FROM ACADEMIC YEAR 2017- 18 ADMITTED BATCH**

**COURSE STRUCTURE AND SYLLABUS**

**I Semester**

| Category | Course Title | Int. marks | Ext. marks | L | T | P | C |
|---|---|---|---|---|---|---|---|
| PC-1 | Advanced Digital System Design | 25 | 75 | 4 | 0 | 0 | 4 |
| PC-2 | CMOS VLSI Design | 25 | 75 | 4 | 0 | 0 | 4 |
| PC-3 | Real Time Operating Systems | 25 | 75 | 4 | 0 | 0 | 4 |
| PE-1 | Advanced Data Communications<br>Image and Video Processing<br>Digital Signal Processors and Architectures | 25 | 75 | **3** | 0 | 0 | 3 |
| PE-2 | CPLD and FPGA Architectures and Applications<br>TCP/IP Internetworking<br>Wireless Communications and Networks | 25 | 75 | **3** | 0 | 0 | 3 |
| OE-1 | ***Open Elective – I** | 25 | 75 | 3 | 0 | 0 | 3 |
| Laboratory I | Digital System Design Lab | 25 | 75 | 0 | 0 | 3 | 2 |
| Seminar I | Seminar | 100 | 0 | 0 | 0 | 3 | 2 |
| **Total** | | **275** | **525** | **21** | **0** | **6** | **25** |

**II Semester**

| Category | Course Title | Int. marks | Ext. marks | L | T | P | C |
|---|---|---|---|---|---|---|---|
| PC-4 | Advanced Computer Architecture | 25 | 75 | 4 | 0 | 0 | 4 |
| PC-5 | Design of Fault Tolerant Systems | 25 | 75 | 4 | 0 | 0 | 4 |
| PC-6 | Embedded System Design | 25 | 75 | 4 | 0 | 0 | 4 |
| PE-3 | Virtual Instrumentation<br>Network Security and Cryptography<br>Scripting Languages | 25 | 75 | **3** | 0 | 0 | 3 |
| PE4 | Verilog Hardware Description Language<br>Adhoc Wireless Networks<br>System On Chip Architectures | 25 | 75 | **3** | 0 | 0 | 3 |
| OE-2 | ***Open Elective – II** | 25 | 75 | 3 | 0 | 0 | 3 |
| Laboratory II | Embedded System Design Lab | 25 | 75 | 0 | 0 | 3 | 2 |
| Seminar II | Seminar | 100 | 0 | 0 | 0 | 3 | 2 |
| **Total** | | **275** | **525** | **21** | **0** | **6** | **25** |

**III Semester**

| Course Title | Int. marks | Ext. marks | L | T | P | C |
|---|---|---|---|---|---|---|
| Technical Paper Writing | 100 | 0 | 0 | 3 | 0 | 2 |
| Comprehensive Viva-Voce | 0 | 100 | 0 | 0 | 0 | 4 |
| Project work Review II | 100 | 0 | 0 | 0 | 22 | 8 |
| **Total** | **200** | **100** | 0 | **3** | 22 | **14** |

**IV Semester**

| Course Title | Int. marks | Ext. marks | L | T | P | C |
|---|---|---|---|---|---|---|
| Project work Review III | 100 | 0 | 0 | 0 | 24 | 8 |
| Project Evaluation (Viva-Voce) | 0 | 100 | 0 | 0 | 0 | 16 |
| **Total** | **100** | **100** | **0** | **0** | **24** | **24** |

***Open Elective subjects must be chosen from the list of open electives offered by OTHER departments.**

**# For Project review I, please refer 7.10 in R17 Academic Regulations.**

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**M. TECH. I YEAR I SEMESTER**
**DIGITAL SYSTEMS & COMPUTER ELECTRONICS**

**ADVANCED DIGITAL SYSTEM DESIGN (PC-1)**

**UNIT- I**

**Processor Arithmetic:** Two's Complement Number System - Arithmetic Operations; Fixed point Number System; Floating Point Number system - IEEE 754 format, Basic binary codes.

**UNIT - II**

**Combinational circuits:** CMOS logic design, Static and dynamic analysis of Combinational circuits, timing hazards. Functional blocks - Decoders, Encoders, Three-state devices, Multiplexers, Parity circuits, Comparators, Adders, Subtractors, Carrylook- ahead adder – timing analysis. Combinational multiplier structures.

**UNIT - III**

**Sequential Logic:** Latches and Flip-Flops, Sequential logic circuits - timing analysis (Set up and hold times), State machines - Mealy & Moore machines, Analysis, FSM design using D Flip-Flops, FSM optimization and partitioning; Synchronizers and metastability. FSM Design examples: Vending machine, Traffic light controller, Washing machine.

**UNIT - IV**

**Subsystem Design using Functional Blocks (1):** Design (including Timing Analysis) of different logical blocks of varying complexities involving mostly combinational circuits:

- ALU
- 4-bit combinational multiplier
- Barrel shifter
- Simple fixed point to floating point encoder
- Dual Priority encoder
- Cascading comparators



**UNIT - V**

**Subsystem Design using Functional Blocks (2):** Design, (including Timing Analysis) of different logical blocks of different complexities involving mostly sequential circuits:

- Pattern (sequence) detector
- Programmable Up-down counter
- Round robin arbiter with 3 requesters
- Process Controller
- FIFO

**TEXT BOOKS:**

1. John F. Wakerly, “Digital Design”, Prentice Hall, 3rd Edition, 2002.

*Note1: VHDL and ABEL are not part of this course.
*Note2: SSI & MSI ICs listed in data books are not part of this course.

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**CMOS VLSI DESIGN (PC-2)**

**UNIT-I**

**MOS Transistor:** Introduction, Ideal I-V Characteristics, C-V Characteristics, Nonideal I-V Effects, DC Transfer Characteristics.

**CMOS Process Technology:** CMOS Technologies, Layout Design Rules, CMOS Process Enhancements, Technology related CAD Issues.

**UNIT-II**

**Circuit Characterization:** Delay Estimation, Logical effort and Transistor Sizing, Power Dissipation, Interconnect, Design Margin, Reliability, Scaling.

**UNIT-III**

**Combinational and Sequential Circuit Design:** Circuit Families, More circuit families, Low power Logic Design, Comparison of Circuit Families, Sequencing Static Circuits, Circuit Design of Latches and Flip-Flops, Static Sequencing Element Methodology, Sequencing Dynamic Circuits, Synchronizers.

**UNIT-IV**

**Datapath Subsystems:** Addition, Subtraction, Comparators, Counters, Boolean Logical Operations, Coding, Shifters, Multiplication, Division.

**Array Subsystems:** SRAM, DRAM, Read-only Memory, Serial Access Memories, Content addressable Memory, PLAs, Array Yield, Reliability and Self-tast.

**UNIT-V**

**Design Methodology and Tools:** Design Methodology, Design Flows, Design Economics, Data Sheets and Documentation, CMOS Physical Design Styles, Interchange Formats. Special Purpose Subsystem- Packaging.



**TEXTBOOKS:**

1. Neil Weste, David Harris, Ayan Banerjee, “CMOS VLSI DESIGN”, 3rd Edition, Pearson.

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**REAL TIME OPERATING SYSTEMS (PC-3)**

**UNIT – I**
**Introduction:** Introduction to UNIX/LINUX, Overview of Commands, File I/O,( open, create, close, lseek, read, write), Process Control ( fork, vfork, exit, wait, waitpid, exec).

**UNIT -II**
**Real Time Operating Systems:** Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency.
Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

**UNIT -III**
**Objects, Services and I/O:** Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

**UNIT - IV**
**Exceptions, Interrupts and Timers:** Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

**UNIT - V**
**Case Studies of RTOS:** RT Linux, Micro C/OS-II, Vx Works, Embedded Linux, and Tiny OS, and Android OS.

**TEXT BOOKS:**
1. Qing Li, “Real Time Concepts for Embedded Systems”, Elsevier, 2011

**REFERENCE BOOKS:**
1. Rajkamal, “Embedded Systems- Architecture, Programming and Design”, 2007, TMH.
2. W. Richard Stevens, Stephan A. Rago, “Advanced UNIX Programming”, 2006, 2nd Edition, Pearson.
3. Dr. Craig Hollabaugh, “Embedded Linux: Hardware, Software and Interfacing”, 2008, 1st Edition, Pearson.

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**ADVANCED DATA COMMUNICATIONS (PE-1)**

**UNIT -I**

Data Communications, Networks and Network Types, Internet History, Standards and Administration, Protocol Layering, TCP/IP protocol suite, OSI Model. Digital Data Transmission, DTE-DCE interface.
**Data Link Layer:** Introduction, Data Link Layer, Nodes and Links, Services, Categories of Links, sub layers, Link Layer Addressing, Address Resolution Protocol.

**UNIT -II**

**Error Detection and Correction**: Types of Errors, Redundancy, detection versus correction, Coding Block Coding: Error Detection, Vertical redundancy cheeks, longitudinal redundancy cheeks, Error Correction, Error correction single bit, Hamming code.
**Cyclic Codes**: Cyclic Redundancy Check, Polynomials, Cyclic Code Encoder Using Polynomials, Cyclic Code Analysis, Advantage of Cyclic Codes, Checksum.
**Data Link Control**: DLC Services, Data Link Layer Protocols, HDLC, Point to Point Protocol.

**UNIT -III**

**Switching:** Introduction to Switching, Circuit Switched Networks, Packet Switching, Structure of switch
**Multiplexing:** Multiplexing, Frequency Division Multiplexing, Time Division Multiplexing.
**Connecting devices:** Passive Hubs, Repeaters, Active Hubs, Bridges, Two Layer Switches, Routers, Three Layer Switches, Gateway, and Backbone Networks.
**Wired LANS:** Ethernet Protocol, Standard Ethernet, Fast Ethernet, Gigabit Ethernet, 10 Giga bit Ethernet



**UNIT -IV**

**Media Access Control (MAC) Sub Layer:** Random Access, ALOHA, Carrier Sense Multiple Access (CSMA), Carrier Sense Multiple Access with Collision Detection (CSMA/CD), Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA),Controlled Access- Reservation, Polling- Token Passing, Channelization - Frequency Division Multiple Access (FDMA), Time - Division Multiple Access (TDMA), Code - Division Multiple Access (CDMA).
**Spectrum Spreading:** Spread Spectrum-Frequency Hopping Spread Spectrum and Direct Sequence Spread Spectrum.

**UNIT -V**

**Networks Layer:** Packetizing, Routing and Forwarding, Packet Switching, Network Layer Performance, IPv4 Address, Address Space, Classful Addressing, Classless Addressing, Dynamic Host Configuration Protocol (DHCP), Network Address Resolution(NATF), Forwarding of IP Packets, Forwarding based on Destination Address, Forwarding based on Label, Routing as Packet Switches.
**Unicast Routing**: Introduction, **Routing Algorithms**-Distance Vector Routing, Link State Routing, Path Vector Routing, **Unicast Routing Protocols**- Routing Information Protocol(RIP), Open Short Path First Version 4.

**TEXT BOOKS:**

1. B. A. Forouzan, “Data Communications and Networking”, 5th Edition, 2013, TMH.
2. William Stallings, “Data and Computer Communications”, 8th Edition, 2007, PHI.

**REFERENCE BOOKS:**

1. Prakash C. Gupta, “Data Communications and Computer Networks”, 2006, PHI.
2. B. A. Forouzan, “Data Communications and Networking”, 2nd Edition, 2013, TMH.
3. Brijendra Singh, “Data Communications and Computer Networks”, 2nd Edition, 2005, PHI.

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**DIGITAL SYSTEMS & COMPUTER ELECTRONICS**

**IMAGE AND VIDEO PROCESSING (PE-1)**

**UNIT – I**

**Fundamentals of Image Processing and Image Transforms:** Basic steps of Image Processing System Sampling and Quantization of an image, Basic relationship between pixels.

**Image Segmentation:** Segmentation concepts, Point, Line and Edge Detection, Thresholding, Region based segmentation.

**UNIT – II**

**Image Enhancement:** Spatial domain methods: Histogram processing, Fundamentals of Spatial filtering, Smoothing spatial filters, Sharpening spatial filters.

Frequency domain methods: Basics of filtering in frequency domain, image smoothing, image sharpening, Selective filtering.

**UNIT – III**

**Image Compression:** Image compression fundamentals - Coding Redundancy, Spatial and Temporal redundancy, Compression models: Lossy & Lossless, Huffman coding, , Bit plane coding, Transform coding, Predictive coding, Wavelet coding, Lossy Predictive coding, JPEG Standards.

**UNIT - IV**

**Basic Steps of Video Processing:** Analog Video, Digital Video. Time-Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video signals, filtering operations.

**UNIT – V**

**2-D Motion Estimation:** Optical flow, General Methodologies, Pixel Based Motion Estimation, Block-Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi resolution motion estimation, Waveform based coding, Block based transform coding, Predictive coding, Application of motion estimation in Video coding.

**TEXT BOOKS:**

1. Gonzalez and Woods, “Digital Image Processing”, 3rd Edition. Pearson.
2. Yao Wang, Joem Ostermann and Ya–quin Zhang, “Video Processing and Communication”, 1st Edition. PH Int.

**REFRENCE BOOKS:**

1. Gonzalez and Woods, “Digital Image Processing using MATLAB”, 2nd Edition., Mc Graw Hill, 2010
2. Milan Sonka, Vaclan Hlavac, “Image Processing Analysis and Machine Vision”, 3rd Edition., CENGAGE, 2008
3. A Murat Tekalp, “Digital Video Processing”, PERSON, 2010
4. S.Jayaraman, S.Esakkirajan, T.Veera Kumar, “Digital Image Processing ”, TMH, 2009

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## DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES (PE-1)

**UNIT-I**

**Introduction to Digital Signal Processing:** Introduction, A digital Signal – Processing system, the sampling process, Discrete time sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), linear time-invariant systems, Digital filters, Decimation and interpolation.

**Architectures for Programmable DSP devices:** Basic Architectural features, DSP computational building blocks, Bus Architecture and Memory, Data addressing capabilities, Address generation UNIT, programmability and program execution, speed issues, features for external interfacing.

**UNIT-II**

**Programmable Digital Signal Processors:** Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX processors, memory space of TMS320C54XX processors, program control, TMS320C54XX instructions and programming, On-Chip peripherals, Interrupts of TMS320C54XX processors, Pipeline operation of TMS320C54XX processors.

**UNIT-III**

**Architecture of ARM Processors:** Introduction to the architecture, Programmer's model- operation modes and states, registers, special registers, floating point registers, Behavior of the application program status register(APSR)-Integer status flags, Q status flag, GE bits, Memory system-Memory system features, memory map, stack memory, memory protection unit (MPU), Exceptions and Interrupts-what are exceptions?, nested vectored interrupt controller(NVIC), vector table, Fault handling, System control block (SCB), Debug, Reset and reset sequence.

**Technical Details of ARM Processors:** General information about Cortex-M3 and cortex M4 processors-Processor type, processor architecture, instruction set, block diagram, memory system, interrupt and exception support, Features of the cortex-M3 and Cortex-M4 Processors-Performance, code density, low power, memory system, memory protection unit, interrupt handling, OS support and system level features, Cortex-M4 specific features, Ease of use, Debug support, Scalability, Compatibility.



**UNIT-IV**

**Instruction SET:** Background to the instruction set in ARM Cortex-M Processors, Comparison of the instruction set in ARM Cortex-M Processors, understanding the assembly language syntax, Use of a suffix in instructions, Unified assembly Language (UAL), Instruction set, Cortex-M4-specific instructions, Barrel shifter, Accessing special instructions and special registers in Programming.

**UNIT-V**

**Floating Point Operations:** About Floating Point Data,Cortex-M4 Floating Point Unit (FPU)-overview, FP registers overview, CPACR register, Floating point register bank, FPSCR, FPU->FPCCR, FPU-> FPCAR, FPU->FPDSCR, FPU->MVFR0, FPU->MVFR1.

**TEXTBOOKS:**

1. Avtar Singh and S. Srinivasan, "Digital Signal Processing", CENGAGE Learning, 2004.
2. Joseph Yiu, "The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors", Elsevier Publications, Third edition.

**REFERENCES:**

1. Andrew N. SLOSS, Dominic SYMES, Chris WRIGHT, "ARM System Developer's Guide Designing and Optimizing System Software", Elsevier Publications, 2004.

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**CPLD AND FPGA ARCHITECTURES AND APPLICATIONS (PE-2)**

**UNIT-I**

**Introduction to Programmable Logic Devices:** Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

**UNIT-II**

**Field Programmable Gate Arrays:** Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, and Applications of FPGAs.

**UNIT -III**

**SRAM Programmable FPGAs:** Introduction, Programming Technology, Device Architecture, the Xilinx XC2000, XC3000 and XC4000 Architectures.

**UNIT -IV**

**Anti-Fuse Programmed FPGAs:** Introduction, Programming Technology, Device Architecture, the Actel ACT1, ACT2 and ACT3 Architectures.

**UNIT -V**

**Design Applications:** General Design Issues, Counter Examples, A Fast Video Controller, and A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

**TEXT BOOKS:**

1. Stephen M. Trimberger, “Field Programmable Gate Array Technology”, Springer International Edition.
2. Charles H. Roth Jr, Lizy Kurian John, “Digital Systems Design”, Cengage Learning.

**REFERENCE BOOKS:**

1. John V. Oldfield, Richard C. Dorf, “Field Programmable Gate Arrays”, Wiley India.
2. Pak K. Chan/Samiha Mourad, “Digital Design Using Field Programmable Gate Arrays”, Pearson Low Price Edition.
3. Ian Grout, “Digital Systems Design with FPGAs and CPLDs”, Elsevier, Newnes.
4. Wayne Wolf, “FPGA based System Design”, Prentice Hall Modern Semiconductor Design Series.

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**DIGITAL SYSTEMS & COMPUTER ELECTRONICS**

**TCP/IP INTERNETWORKING (PE-2)**

**UNIT - I**

**Network Models:** Layered Tasks, The OSI Model, Layers in OSI Model, TCP/IP Protocol suite, Addressing.

**Connecting devices:** Passive Hubs, Repeaters, Active Hubs, Bridges, Two Layer Switches, Routers, Three Layer Switches, Gateway, Backbone Networks.

**UNIT - II**

**Internetworking Concepts:** Principles of Internetworking, Connectionless Interconnection, Application Level Interconnection, Network Level Interconnection, Properties of the Internet, Internet Architecture, Interconnection through IP Routers

**TCP, UDP & IP:** TCP Services, TCP Features, Segment, A TCP Connection, Flow Control, Error Control, Congestion Control, Process to Process Communication, User Datagram, Checksum, UDP Operation, IP Datagram, Fragmentation, Options, IP Addressing: Classful Addressing, IPV6.

**UNIT - III**

**Congestion and Quality of Service:** Data Traffic, Congestion, Congestion Control, Congestion Control in TCP, Congestion Control in Frame Relay, Source Based Congestion Avoidance, DEC Bit Scheme, Quality of Service, Techniques to Improve QOS: Scheduling, Traffic Shaping, Admission Control, Resource Reservation, Integrated Services and Differentiated Services.

**UNIT - IV**

**Queue Management:** Concepts of Buffer Management, Drop Tail, Drop Front, Random Drop, Passive Buffer Management Schemes, Drawbacks of PQM, Active Queue Management: Early Random Drop, RED Algorithm.

**UNIT - V**

**Stream Control Transmission Protocol:** SCTP Services, SCTP Features, Packet Format, Flow Control, Error Control, Congestion Control.

**Mobile Network Layer:** Entities and Terminology, IP Packet Delivery, Agents, Addressing, Agent Discovery, Registration, Tunneling and Encapsulating, Inefficiency in Mobile IP.

**Mobile Transport Layer:** Classical TCP Improvements, Indirect TCP, Snooping TCP, Mobile TCP, Fast Retransmit/Fast Recovery, Transmission, Timeout Freezing, Selective Retransmission, Transaction Oriented TCP.

**TEXT BOOKS:**

1. Behrouz A Forouzan, “TCP/IP Protocol Suite”, TMH, 3rd Edition
2. B.A. Forouzan, “Data communication & Networking”, TMH, 4th Edition.

**REFERENCES:**

1. Mahbub Hasan & Raj Jain, ” High performance TCP/IP Networking”, PHI -2005
2. Douglas. E.Comer, “Internetworking with TCP/IP “, Volume I PHI
3. Larry L. Perterson and Bruce S.Davie , “Computer Networks- A Systems Approach”, 2011, Morgan Kaufmann
4. Jochen Schiiler, “Mobile Communications”, Pearson, 2nd Edition.

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**WIRELESS COMMUNICATIONS AND NETWORKS (PE-2)**

**UNIT -I**

**The Cellular Concept-System Design Fundamentals:** Introduction, Frequency Reuse, Channel Assignment Strategies, Handoff Strategies- Prioritizing Handoffs, Practical Handoff Considerations, Interference and system capacity – Co channel Interference and system capacity, Channel planning for Wireless Systems, Adjacent Channel interference , Power Control for Reducing interference, Trunking and Grade of Service, Improving Coverage & Capacity in Cellular Systems- Cell Splitting, Sectoring .

**UNIT –II**

**Mobile Radio Propagation: Large-Scale Path Loss:** Introduction to Radio Wave Propagation, Free Space Propagation Model, Relating Power to Electric Field, The Three Basic Propagation Mechanisms, Reflection-Reflection from Dielectrics, Brewster Angle, Reflection from prefect conductors, Ground Reflection (Two-Ray) Model, Diffraction-Fresnel Zone Geometry, Knife-edge Diffraction Model, Multiple knife-edge Diffraction, Scattering, Outdoor Propagation Models- Longley-Ryce Model, Okumura Model, Hata Model, PCS Extension to Hata Model, Walfisch and Bertoni Model, Wideband PCS Microcell Model, Indoor Propagation Models-Partition losses (Same Floor), Partition losses between Floors, Log-distance path loss model, Ericsson Multiple Breakpoint Model, Attenuation Factor Model, Signal penetration into buildings, Ray Tracing and Site Specific Modeling.

**UNIT –III**

**Mobile Radio Propagation: Small –Scale Fading and Multipath:** Small Scale Multipath propagation-Factors influencing small scale fading, Doppler shift, Impulse Response Model of a multipath channel- Relationship between Bandwidth and Received power, Small-Scale Multipath Measurements-Direct RF Pulse System, Spread Spectrum Sliding Correlator Channel Sounding, Frequency Domain Channels Sounding, Parameters of Mobile Multipath Channels-Time Dispersion Parameters, Coherence Bandwidth, Doppler Spread and Coherence Time, Types of Small-Scale Fading-Fading effects Due to Multipath Time Delay Spread, Flat fading, Frequency selective fading, Fading effects Due to Doppler Spread-Fast fading, slow fading, Statistical Models for multipath Fading Channels-Clarke's model for flat fading, spectral shape due to Doppler spread in Clarke's model, Simulation of Clarke and Gans Fading Model, Level crossing and fading statistics, Two-ray Rayleigh Fading Model.



**UNIT -IV**

**Equalization and Diversity:** Introduction, Fundamentals of Equalization, Training A Generic Adaptive Equalizer, Equalizers in a communication Receiver, Linear Equalizers, Non linear Equalization-Decision Feedback Equalization (DFE), Maximum Likelihood Sequence Estimation (MLSE) Equalizer, Algorithms for adaptive equalization-Zero Forcing Algorithm, Least Mean Square Algorithm, Recursive least squares algorithm. Diversity Techniques-Derivation of selection Diversity improvement, Derivation of Maximal Ratio Combining improvement, Practical Space Diversity Consideration-Selection Diversity, Feedback or Scanning Diversity, Maximal Ratio Combining, Equal Gain Combining, Polarization Diversity, Frequency Diversity, Time Diversity, RAKE Receiver.

**UNIT -V**

**Wireless Networks:** Introduction to wireless Networks, Advantages and disadvantages of Wireless Local Area Networks, WLAN Topologies, WLAN Standard IEEE 802.11,IEEE 802.11 Medium Access

Control, Comparison of IEEE 802.11 a,b,g and n standards, IEEE 802.16 and its enhancements, Wireless PANs, Hyper LAN, WLL.

**TEXT BOOKS:**

1. Theodore, S. Rappaport, "Wireless Communications, Principles, Practice", 2nd Edition, 2002, PHI.
2. Andrea Goldsmith, "Wireless Communications", 2005 Cambridge University Press.
3. Kaveh Pah Laven and P. Krishna Murthy, "Principles of Wireless Networks", 2002, PE
4. Gottapu Sasibhushana Rao, "Mobile Cellular Communication", Pearson Education, 2012.

**REFERENCE BOOKS:**

1. Kamilo Feher, "Wireless Digital Communications", 1999, PHI.
2. William Stallings, "Wireless Communication and Networking", 2003, PHI.

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**DIGITAL SYSTEMS & COMPUTER ELECTRONICS**

**DIGITAL SYSTEM DESIGN LAB (Laboratory I)**

**Part –I**

Programming can be done using any complier. Down load the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels) and logic analyzer apart from verification by simulation with any of the front end tools.

1. HDL code to realize all the logic gates
2. Design and Simulation of adder, Serial Binary Adder, Multi Precession Adder, Carry
3. Look Ahead Adder.
4. Design of 2-to-4 decoder
5. Design of 8-to-3 encoder (without and with parity)
6. Design of 8-to-1 multiplexer
7. Design of 4 bit binary to gray converter
8. Design of Multiplexer/ Demultiplexer, comparator
9. Design of Full adder using 3 modeling styles
10. Design of flip flops: SR, D, JK, T
11. Design of 4-bit binary, BCD counters ( synchronous/ asynchronous reset) or any sequence counter
12. Design of a N- bit Register of Serial- in Serial –out, Serial in parallel out, Parallel in
13. Serial out and Parallel in Parallel Out.
14. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
15. Design of 4- Bit Multiplier, Divider.
16. Design of ALU to Perform – ADD, SUB, AND-OR, 1's and 2's Compliment,
17. Multiplication and Division.
18. Design of Finite State Machine.
19. Implementing the above designs on Xilinx/Altera/Cypress/equivalent based FPGA/CPLD kits .



**Part –II**

1. Static and Dynamic Characteristics of CMOS Inverter
2. Implementation of EX-OR gate using complementary CMOS, Psedo-NMOS, Dynamic and domino logic style
3. Implementation of Full Adder using Transmission Gates