JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH IN EMBEDDED SYSTEMS & VLSI DESIGN/VLSI AND EMBEDDED SYSTEMS/ ELECTRONICS DESIGN TECHNOLOGY.

EFFECTIVE FROM ACADEMIC YEAR 2017- 18 ADMITTED BATCH

COURSE STRUCTURE AND SYLLABUS

I Semester

Category	Course Title	Int. marks	Ext. marks	L	T	P	C
PC-1	Embedded System Design	25	75	4	0	0	4
PC-2	VLSI Technology	25	75	4	0	0	4
PC-3	CMOS Analog Integrated Circuit Design	25	75	4	0	0	4
PE-1	Hardware Software Co-Design Digital System Design Advanced Computer Architecture	25	75	**3**	0	0	3
PE-2	VLSI DSP Architectures CMOS Digital Integrated Circuit Design CPLD and FPGA Architectures and Applicat	25	75	**3**	0	0	3
OE-1	***Open Elective – I**	25	75	3	0	0	3
Laboratory I	VLSI Laboratory	25	75	0	0	3	2
Seminar I	Seminar	100	0	0	0	3	2
Total		**275**	**525**	**21**	**0**	**6**	**25**

II Semester

Category	Course Title	Int. marks	Ext. marks	L	T	P	C
PC-4	Low Power VLSI Design	25	75	4	0	0	4
PC-5	CMOS Mixed Signal Circuit Design	25	75	4	0	0	4
PC-6	Real Time Operating Systems	25	75	4	0	0	4
PE-3	Advanced Digital Signal Processing System On Chip Architecture Embedded Networking	25	75	**3**	0	0	3
PE4	Design for Testability Physical Design Automation Scripting Languages	25	75	**3**	0	0	3
OE-2	***Open Elective – II**	25	75	3	0	0	3
Laboratory II	Embedded Systems Laboratory	25	75	0	0	3	2
Seminar II	Seminar	100	0	0	0	3	2
Total		**275**	**525**	**21**	**0**	**6**	**25**

III Semester

Course Title	Int. marks	Ext. marks	L	T	P	C
Technical Paper Writing	100	0	0	3	0	2
Comprehensive Viva-Voce	0	100	0	0	0	4
Project work Review II	100	0	0	0	22	8
Total	**200**	**100**	0	**3**	22	**14**

IV Semester

Course Title	Int. marks	Ext. marks	L	T	P	C
Project work Review III	100	0	0	0	24	8
Project Evaluation (Viva-Voce)	0	100	0	0	0	16
Total	**100**	**100**	**0**	**0**	**24**	**24**

***Open Elective subjects must be chosen from the list of open electives offered by OTHER departments.**

 # For Project review I, please refer 7.10 in R17 Academic Regulations.

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EMBEDDED SYSTEM DESIGN (PC-1)

UNIT -I

Introduction to Embedded Systems: Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

UNIT -II

Typical Embedded System: Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT -III

Embedded Firmware: Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT –IV

RTOS Based Embedded System Design: Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT -V

Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

TEXT BOOKS:

1. Shibu K.V, “Introduction to Embedded Systems”, McGraw Hill.

REFERENCE BOOKS:

1. Raj Kamal, “Embedded Systems”, TMH.
2. Frank Vahid, Tony Givargis, “Embedded System Design”, John Wiley.
3. Lyla, “Embedded Systems”, Pearson, 2013
4. David E. Simon, “An Embedded Software Primer”, Pearson Education.

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VLSI TECHNOLOGY (PC-2)

UNIT –I

Review of Microelectronics and Introduction to MOS Technologies: MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: Ids – Vds relationships, Threshold Voltage VT, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT –II

Layout Design and Tools: Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

Logic Gates & Layouts: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT –III

Overview of semiconductor industry: Stages of Manufacturing, Process and product trends, Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Basic wafer fabrication operations, Yield measurement, Contamination sources, Clean room construction, Oxidation and Photolithography, Doping and Depositions, Metallization.Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hard bake, develop inspect, Dry etching Wet etching, resist stripping

UNIT –IV

Doping and depositions: Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2, CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapor phase epitoxy, molecular beam epitaxy.

UNIT –V

Design rules and Scaling, BICMOS ICs: Choice of transistor types, pnp transistors, Resistors, capacitors,
Packaging: Chip characteristics, package functions, package operations

TEXT BOOKS:

1. Peter Van Zant, “Microchip fabrication”, McGraw Hill, 1997.
2. C.Y. Chang and S.M. Sze, “ULSI technology”, McGraw Hill, 2000

REFERENCE BOOKS:

1. Muhammad H Rashid, “Micro Electronics circuits Analysis and Design”, 2nd Edition, CENAGE Learning2011.
2. Eugene D. Fabricius, “Introduction to VLSI design”, McGraw Hill, 1999
3. Wani-Kai Chen (editor), “The VLSI Hand book”, CRI/IEEE press, 2000
4. S.K. Gandhi, “VLSI Fabrication principles”, John Wiley and Sons, NY, 1994

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CMOS ANALOG INTEGRATED CIRCUIT DESIGN (PC-3)

UNIT -I

MOS Devices and Modeling: The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT -II

Analog CMOS Sub-Circuits:MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT -III

CMOS Amplifiers: Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT -IV

CMOS Operational Amplifiers: Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power- Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT -V

Comparators: Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:

1. Philip E. Allen and Douglas R. Holberg, “CMOS Analog Circuit Design”, Oxford University Press, International 2nd Edition/Indian Edition, 2010.
2. Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, “Analysis and Design of Analog Integrated Circuits”, Wiley India, Fifth Edition, 2010.

REFERENCE BOOKS:

1. David A. Johns, Ken Martin, “Analog Integrated Circuit Design”, Wiley Student Edn, 2013.
2. Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, TMH Edition.
3. Baker, Li and Boyce, “CMOS: Circuit Design, Layout and Simulation”, PHI.

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HARDWARE SOFTWARE CO-DESIGN (PE-1)

UNIT –I

Co- Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT –II

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), and Mixed Systems.

UNIT –III

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT –IV

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT –V

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

TEXT BOOKS:

1. Jorgen Staunstrup, Wayne Wolf, “Hardware / Software Co- Design Principles and Practice”, 2009, Springer.
2. Giovanni De Micheli, Mariagiovanna Sami, “Hardware / Software Co- Design”, 2002, Kluwer Academic Publishers

REFERENCE BOOKS:

1. Patrick R. Schaumont, “A Practical Introduction to Hardware/Software Co-design”, 2010, Springer

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DIGITAL SYSTEM DESIGN (PE-1)

UNIT –I

Minimization and Transformation of Sequential Machines: The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines.Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

UNIT –II

Digital Design: Digital Design Using ROMs, PALs and PLAs, BCD Adder, 32 – bit adder, State graphs for control circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner, Binary divider.

UNIT –III

SM Charts: State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier, dice game controller.

UNIT –IV

Fault Modeling & Test Pattern Generation: Logic Fault model – Fault detection & Redundancy-Fault equivalence and fault location –Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model.

Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults.

UNIT –V

Fault Diagnosis in Sequential Circuits: Circuit Test Approach, Transition Check Approach – State identification and fault detection experiment, Machine identification, Design of fault detection experiment

TEXT BOOKS:

1. Charles H. Roth, “Fundamentals of Logic Design”, 5th Ed., Cengage Learning.
2. Miron Abramovici, Melvin A Breuer and Arthur D. Friedman, “Digital Systems Testing and Testable Design”, John Wiley & Sons Inc.
3. N. N. Biswas, “Logic Design Theory”, PHI

REFERENCE BOOKS:

1. Z. Kohavi , “Switching and Finite Automata Theory”, 2nd Ed., 2001, TMH
2. Morris Mano, M.D. Ciletti, “Digital Design”, 4th Edition, PHI.
3. Samuel C. Lee , “Digital Circuits and Logic Design”, PHI

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ADVANCED COMPUTER ARCHITECTURE (PE-1)

UNIT- I

Fundamentals of Computer Design: Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law.
Instruction set principles and examples- Introduction, classifying instruction set- memory addressing-type and size of operands, operations in the instruction set.

UNIT – II

Pipelines: Introduction ,basic RISC instruction set ,Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining , Pipeline hazards, Reducing pipeline branch penalties.
Memory Hierarchy Design: Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT - III

Instruction Level Parallelism the Hardware Approach: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.
ILP Software Approach: Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT – IV

Multi Processors and Thread Level Parallelism: Multi Processors and Thread level Parallelism-Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT – V

Inter Connection and Networks: Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.
Intel Architecture: Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls

TEXT BOOKS:

1. John L. Hennessy, David A. Patterson, "Computer Architecture: A Quantitative Approach", 3rd Edition, An Imprint of Elsevier.

REFERENCE BOOKS:

1. John P. Shen and Miikko H. Lipasti, "Modern Processor Design: Fundamentals of Super Scalar Processors", 2002, Beta Edition, McGrawHill.
2. Kai Hwang, Faye A.Brigs., "Computer Architecture, and Parallel Processing", McGraw Hill.,
3. Dezso Sima, Terence Fountain, Peter Kacsuk, "Advanced Computer Architecture - A Design Space Approach", Pearson Education.

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VLSI DSP ARCHITECTURES (PE-2)

UNIT - I
Essential feature of Instruction set architectures of CISC, RISC and DSP processors and their implications for implementation as VLSI Chips, Micro programming approaches for implementation of control part of the processor. Assessing understanding performance, Introduction, CPU performance and its factors, evaluating performance, real stuff: Two spec bench marks and performance of recent INTEL processors, fallacies and pitfalls

UNIT - II
Data Path and Control: Introduction, logic design conventions, building a data path, a simple implementation scheme, a multi cycle implementation, exceptions, micro programming: simplifying control design, an introduction to digital design using hardware description language, fallacies and pitfalls

UNIT - III
Enhancing performance with pipeline: An overview of pipelining, a pipe lined data path. Pipe lined control, data hazards and forwarding, data hazards and stalls, branch hazards using a hard ware description language to describe and model a pipe line, exceptions, advanced pipelining: extracting more performance, fallacies and pitfalls

UNIT - IV
Computational Accuracy in DSP implementations: Introduction, number formats for signals and coefficients in DSP system, dynamic range and precision, sources of errors in DSP implementations, A/D conversion errors, DSP computational errors, D /A conversion errors

UNIT - V
Architectures for programmable digital signal processing devices: introduction, basic architectural features, DSP Computational building blocks, bus architecture and memory, data addressing capabilities, address generation unit, programmability, and program execution, speed issues, features for external interfacing.

TEXT BOOKS:
1. D.A, Patterson and J.L Hennessy, “Computer Organization and Design: Hard ware/ Software Interface”, 4th Edition, Elsevier, 2011
2. A.S Tannenbaum, “Structural Computer organization”, 4th Edition, Prentice-Hall, 1999

REFERENCE BOOKS:
1. W. Wolf, “Modern VLSI Design: System on Silicon”, 2nd Edition, Person Education,1998
2. Keshab Parhi, “VLSI Digital Signal Processing system design and implementations”, Wiley 1999
3. Avatar sign, Srinivasan S, “Digital Signal Processing implementations using DSP microprocessors with examples”, Thomson 4th reprint, 2004.

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CMOS DIGITAL INTEGRATED CIRCUIT DESIGN (PE-2)

UNIT –I

MOS Design: Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT –II

Combinational MOS Logic Circuits:MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT –III

Sequential MOS Logic Circuits: Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch, and edge triggered flip-flop.

UNIT –IV

Dynamic Logic Circuits: Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT –V

Semiconductor Memories: Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash and NAND flash.

TEXT BOOKS:

1. Ken Martin, “Digital Integrated Circuit Design”, Oxford University Press, 2011.
2. Sung-Mo Kang, Yusuf Leblebici, “CMOS Digital Integrated Circuits Analysis and Design”, TMH, 3rd Edition, 2011.

REFERENCE BOOKS:

1. Ming-BO Lin, “Introduction to VLSI Systems: A Logic, Circuit and System Perspective”, CRC Press, 2011
2. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, “Digital Integrated Circuits – A Design Perspective”, 2nd Edition, PHI.

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CPLD AND FPGA ARCHITECTURES AND APPLICATIONS (PE-2)

UNIT-I

Introduction to Programmable Logic Devices: Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT-II

Field Programmable Gate Arrays: Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT –III

SRAM Programmable FPGAs: Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT –IV

Anti-Fuse Programmed FPGAs: Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT –V

Design Applications: General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:

1. Stephen M. Trimberger, “Field Programmable Gate Array Technology”, Springer International Edition.
2. Charles H. Roth Jr, Lizy Kurian John, “Digital Systems Design”, Cengage Learning.

REFERENCE BOOKS:

1. John V. Oldfield, Richard C. Dorf, “Field Programmable Gate Arrays”, Wiley India.
2. Pak K. Chan/Samiha Mourad, “Digital Design Using Field Programmable Gate Arrays”, Pearson Low Price Edition.
3. Ian Grout, “Digital Systems Design with FPGAs and CPLDs”, Elsevier, Newnes.
4. Wayne Wolf, “FPGA based System Design”, Prentice Hall Modern Semiconductor Design Series.

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VLSI LAB

Note:

- Minimum of 10 programs from Part –I and 2 programs from Part -II are to be conducted.

Design and implementation of the following CMOS digital/analog circuits must be carried out using **Cadence / Mentor Graphics / Synopsys / Equivalent** CAD tools. The design shall include Gate-level design, Transistor-level design, Hierarchical design, Verilog HDL/VHDL design, Logic synthesis, Simulation and verification.

Part –I: VLSI Front End Design programs:

Programming can be done using any complier. Down load the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels) and logic analyzer apart from verification by simulation with any of the front end tools.

1. HDL code to realize all the logic gates
2. Design and Simulation of adder, Serial Binary Adder, Multi Precession Adder, Carry
3. Look Ahead Adder.
4. Design of 2-to-4 decoder
5. Design of 8-to-3 encoder (without and with parity)
6. Design of 8-to-1 multiplexer
7. Design of 4 bit binary to gray converter
8. Design of Multiplexer/ Demultiplexer, comparator
9. Design of Full adder using 3 modeling styles
10. Design of flip flops: SR, D, JK, T
11. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset) or any sequence counter
12. Design of a N- bit Register of Serial- in Serial –out, Serial in parallel out, Parallel in
13. Serial out and Parallel in Parallel Out.
14. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
15. Design of 4- Bit Multiplier, Divider.
16. Design of ALU to Perform – ADD, SUB, AND-OR, 1's and 2's Compliment, Multiplication and Division.
17. Design of Finite State Machine.
18. Implementing the above designs on Xilinx/Altera/Cypress/equivalent based FPGA/CPLD kits.

Part –II: VLSI Back End Design programs:

Design and implementation of the following CMOS digital/analog circuits using **Cadence / Mentor Graphics / Synopsys / Equivalent** CAD tools. The design shall include Gate-level design/Transistor-level design/Hierarchical design/Verilog HDL or VHDL design, Logic synthesis, Simulation and verification, Scaling of CMOS Inverter for different technologies, study of secondary effects (temperature, power supply and process corners), Circuit optimization with respect to area, performance and/or power, Layout, Extraction of parasitic and back annotation, modifications in circuit parameters and layout consumption, DC/transient analysis, Verification of layouts (DRC, LVS).

1. Introduction to layout design rules
2. Layout, physical verification, placement & route for complex design, static timing analysis, IR drop analysis and crosstalk analysis of the following:
    - Basic logic gates
    - CMOS inverter
    - CMOS NOR/ NAND gates
    - CMOS XOR and MUX gates
    - CMOS 1-bit full adder
    - Static / Dynamic logic circuit (register cell)
    - Latch
    - Pass transistor
3. Layout of any combinational circuit (complex CMOS logic gate)- Learning about data paths