JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. TECH IN EMBEDDED SYSTEMS.
EFFECTIVE FROM ACADEMIC YEAR 2017- 18 ADMITTED BATCH

COURSE STRUCTURE AND SYLLABUS

I Semester

Category	Course Title	Int. marks	Ext. marks	L	T	P	C
PC-1	Embedded System Design	25	75	4	0	0	4
PC-2	ARM Processor Architectures	25	75	4	0	0	4
PC-3	Real Time Operating Systems	25	75	4	0	0	4
PE-1	Advanced Computer Architecture CMOS VLSI Design CPLD and FPGA Architectures and Applications	25	75	**3**	0	0	3
PE-2	Digital System Design Embedded C TCP / IP Internetworking	25	75	**3**	0	0	3
OE-1	***Open Elective – I**	25	75	3	0	0	3
Laboratory I	Embedded Systems Laboratory	25	75	0	0	3	2
Seminar I	Seminar	100	0	0	0	3	2
Total		**275**	**525**	**21**	**0**	**6**	**25**

II Semester

Category	Course Title	Int. marks	Ext. marks	L	T	P	C
PC-4	Embedded Computing	25	75	4	0	0	4
PC-5	System On Chip Architecture	25	75	4	0	0	4
PC-6	Sensors and Actuators	25	75	4	0	0	4
PE-3	Design for Testability Wireless Communication and Networks Scripting Languages	25	75	**3**	0	0	3
PE4	Advanced Digital Signal Processors Network Security and Cryptography Hardware Software Co-Design	25	75	**3**	0	0	3
OE-2	***Open Elective – II**	25	75	3	0	0	3
Laboratory II	Advanced Embedded Systems Laboratory	25	75	0	0	3	2
Seminar II	Seminar	100	0	0	0	3	2
Total		**275**	**525**	**21**	**0**	**6**	**25**

III Semester

Course Title	Int. marks	Ext. marks	L	T	P	C
Technical Paper Writing	100	0	0	3	0	2
Comprehensive Viva-Voce	0	100	0	0	0	4
Project work Review II	100	0	0	0	22	8
Total	**200**	**100**	0	**3**	22	**14**

IV Semester

Course Title	Int. marks	Ext. marks	L	T	P	C
Project work Review III	100	0	0	0	24	8
Project Evaluation (Viva-Voce)	0	100	0	0	0	16
Total	**100**	**100**	**0**	**0**	**24**	**24**

***Open Elective subjects must be chosen from the list of open electives offered by OTHER departments.**

 # For Project review I, please refer 7.10 in R17 Academic Regulations.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. TECH. I YEAR I SEMESTER
EMBEDDED SYSTEMS

EMBEDDED SYSTEM DESIGN (PC-1)

UNIT -I

Introduction to Embedded Systems: Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

UNIT -II

Typical Embedded System: Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT -III

Embedded Firmware: Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT -IV

RTOS Based Embedded System Design: Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT -V

Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

TEXT BOOKS:

1. Shibu K.V, “Introduction to Embedded Systems”, McGraw Hill.

REFERENCE BOOKS:

1. Raj Kamal, “Embedded Systems”, TMH.
2. Frank Vahid, Tony Givargis, “Embedded System Design”, John Wiley.
3. Lyla, “Embedded Systems”, Pearson, 2013
4. David E. Simon, “An Embedded Software Primer”, Pearson Education.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. TECH. I YEAR I SEMESTER
EMBEDDED SYSTEMS

ARM PROCESSOR ARCHITECTURES (PC-2)

UNIT – I

ARM Architecture and Instruction Set: ARM Design Philosophy, Registers, PSR, Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families. Instruction Set: Data Processing Instructions, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

UNIT – II

ARM Programming Model: Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Interrupts, Software Interrupt Instructions, Exception handling

UNIT – III

ARM Programming using High Level Language: Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

UNIT – IV

Memory Management: Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Content Switch.

UNIT – V

Integer and Floating Point Arithmetic on ARM: Double precision Integer Multiplication, Division, Square roots, Endian Reversal and Bit Operations, Random Number Generation, DSP on ARM – FIR filters, IIR filters.

TEXT BOOKS:

1. Andrew N. Sloss, Dominic Symes, Chris Wright, “ARM Systems Developer’s Guides- Designing & Optimizing System Software”, 2008, Elsevier.

REFERENCE BOOKS:

1. Jonathan W. Valvano – Brookes / Cole, “Embedded Microcomputer Systems, Real Time Interfacing”, 1999, Thomas Learning.

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M. TECH. I YEAR I SEMESTER
EMBEDDED SYSTEMS

REAL TIME OPERATING SYSTEMS (PC-3)

UNIT – I
Introduction: Introduction to UNIX/LINUX, Overview of Commands, File I/O,(open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT - II
Real Time Operating Systems: Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency.
Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

UNIT - III
Objects, Services and I/O: Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

UNIT - IV
Exceptions, Interrupts and Timers: Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT - V
Case Studies of RTOS: RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, and Tiny OS.

TEXT BOOKS:
1. Qing Li, “Real Time Concepts for Embedded Systems”, Elsevier, 2011

REFERENCE BOOKS:
1. Rajkamal, “Embedded Systems- Architecture, Programming, and Design”, 2007, TMH.
2. W. Richard Stevens, Stephan A. Rago, “Advanced UNIX Programming”, 2006, 2nd Edition, Pearson.
3. Dr. Craig Hollabaugh, “Embedded Linux: Hardware, Software and Interfacing”, 2008, 1st Edition, Pearson.

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M. TECH. I YEAR I SEMESTER
EMBEDDED SYSTEMS

ADVANCED COMPUTER ARCHITECTURE (PE-1)

UNIT- I

Fundamentals of Computer Design: Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law.
Instruction set principles and examples- Introduction, classifying instruction set- memory addressing-type and size of operands, operations in the instruction set.

UNIT – II

Pipelines: Introduction ,basic RISC instruction set ,Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining , Pipeline hazards, Reducing pipeline branch penalties.
Memory Hierarchy Design: Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT - III

Instruction Level Parallelism the Hardware Approach: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.
ILP Software Approach: Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT – IV

Multi Processors and Thread Level Parallelism: Multi Processors and Thread level Parallelism-Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT – V

Inter Connection and Networks: Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.
Intel Architecture: Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls

TEXT BOOKS:

1. John L. Hennessy, David A. Patterson, "Computer Architecture: A Quantitative Approach", 3rd Edition, An Imprint of Elsevier.

REFERENCE BOOKS:

1. John P. Shen and Miikko H. Lipasti, "Modern Processor Design : Fundamentals of Super Scalar Processors", 2002, Beta Edition, McGrawHill
2. Kai Hwang, Faye A.Brigs., "Computer Architecture, and Parallel Processing", McGraw Hill.,
3. Dezso Sima, Terence Fountain, Peter Kacsuk , "Advanced Computer Architecture - A Design Space Approach", Pearson Education.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. TECH. I YEAR I SEMESTER
EMBEDDED SYSTEMS

CMOS VLSI DESIGN (PE-1)

UNIT-I

MOS Transistor: Introduction, Ideal I-V Characteristics, C-V Characteristics, Non ideal I-V Effects, DC Transfer Characteristics.

CMOS Process Technology: CMOS Technologies, Layout Design Rules, CMOS Process Enhancements, Technology related CAD Issues.

UNIT-II

Circuit Characterization: Delay Estimation, Logical effort and Transistor Sizing, Power Dissipation, Interconnect, Design Margin, Reliability, Scaling.

UNIT-III

Combinational and Sequential Circuit Design: Circuit Families, More circuit families, Low power Logic Design, Comparison of Circuit Families, Sequencing Static Circuits, Circuit Design of Latches and Flip-Flops, Static Sequencing Element Methodology, Sequencing Dynamic Circuits, Synchronizers.

UNIT-IV

Datapath Subsystems: Addition, Subtraction, Comparators, Counters, Boolean Logical Operations, Coding, Shifters, Multiplication, Division.

Array Subsystems: SRAM, DRAM, Read-only Memory, Serial Access Memories, Content addressable Memory, PLAs, Array Yield, Reliability and Self-Test.

UNIT-V

Design Methodology and Tools: Design Methodology, Design Flows, Design Economics, Data Sheets and Documentation, CMOS Physical Design Styles, Interchange Formats.

Special Purpose Subsystem: Packaging.

TEXTBOOKS:

1. Neil Weste, David Harris, Ayan Banerjee, “CMOS VLSI DESIGN”, 3rd Edition, Pearson.

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M. TECH. I YEAR I SEMESTER
EMBEDDED SYSTEMS

CPLD AND FPGA ARCHITECTURES AND APPLICATIONS (PE-1)

UNIT-I

Introduction to Programmable Logic Devices: Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT-II

Field Programmable Gate Arrays: Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT -III

SRAM Programmable FPGAs: Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT -IV

Anti-Fuse Programmed FPGAs: Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT -V

Design Applications: General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:

1. Stephen M. Trimberger, "Field Programmable Gate Array Technology", Springer International Edition.
2. Charles H. Roth Jr, LizyKurian John, "Digital Systems Design", Cengage Learning.

REFERENCE BOOKS:

1. John V. Oldfield, Richard C. Dorf, "Field Programmable Gate Arrays", Wiley India.
2. Pak K. Chan/Samiha Mourad, "Digital Design Using Field Programmable Gate Arrays", Pearson Low Price Edition.
3. Ian Grout, "Digital Systems Design with FPGAs and CPLDs", Elsevier, Newnes.
4. Wayne Wolf, "FPGA based System Design", Prentice Hall Modern Semiconductor Design Series.

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M. TECH. I YEAR I SEMESTER
EMBEDDED SYSTEMS

DIGITAL SYSTEM DESIGN (PE-2)

UNIT -I

Minimization and Transformation of Sequential Machines: The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines. Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

UNIT -II

Digital Design: Digital Design Using ROMs, PALs and PLAs, BCD Adder, 32 – bit adder, State graphs for control circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner, Binary divider.

UNIT -III

SM Charts: State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier, dice game controller.

UNIT -IV

Fault Modeling & Test Pattern Generation: Logic Fault model – Fault detection & Redundancy-Fault equivalence and fault location –Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model. Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults.

UNIT -V

Fault Diagnosis in Sequential Circuits: Circuit Test Approach, Transition Check Approach – State identification and fault detection experiment, Machine identification, Design of fault detection experiment

TEXT BOOKS:

1. Charles H. Roth, “Fundamentals of Logic Design”, 5th Edition, Cengage Learning.
2. Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman, “Digital Systems Testing and Testable Design”, John Wiley & Sons Inc.
3. N. N. Biswas, “Logic Design Theory”, PHI

REFERENCE BOOKS:

1. Z. Kohavi , “Switching and Finite Automata Theory”, 2nd Edition, 2001, TMH
2. Morris Mano, M.D.Ciletti, “Digital Design”, 4th Edition, PHI.
3. Samuel C. Lee , “Digital Circuits and Logic Design”, PHI

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. TECH. I YEAR I SEMESTER
EMBEDDED SYSTEMS

EMBEDDED C (PE-2)

UNIT – I

Programming Embedded Systems in C: Introduction ,What is an embedded system, Which processor should you use, Which programming language should you use, Which operating system should you use, How do you develop embedded software, Conclusions.

Introducing the 8051 Microcontroller Family: Introduction, What's in a name, The external interface of the Standard 8051, Reset requirements ,Clock frequency and performance, Memory issues, I/O pins, Timers, Interrupts, Serial interface, Power consumption ,Conclusions.

UNIT – II

Reading Switches: Introduction, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version), Example: Reading and writing bits (generic version), The need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs (basic code), Example: Counting goats, Conclusions.

UNIT – III

Adding Structure to the Code: Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the 'Hello Embedded World' example, Example: Restructuring the goat-counting example, Further examples, Conclusions.

UNIT – IV

Meeting Real-Time Constraints: Introduction, Creating 'hardware delays' using Timer 0 and Timer 1, Example: Generating a precise 50 ms delay, Example: Creating a portable hardware delay, Why not use Timer 2?, The need for 'timeout' mechanisms, Creating loop timeouts, Example: Testing loop timeouts, Example: A more reliable switch interface, Creating hardware timeouts, Example: Testing a hardware timeout, Conclusions.

UNIT – V

Case Study: Intruder Alarm System: Introduction, The software architecture, Key software components used in this example, running the program, the software, Conclusions.

TEXT BOOKS:

1. Michael J. Pont, "Embedded C", 2nd Edition, Pearson Education, 2008

REFERENCE BOOKS:

1. Nigel Gardner, "PIC micro MCU C-An introduction to programming", The Microchip PIC in CCS C -

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. TECH. I YEAR I SEMESTER
EMBEDDED SYSTEMS

TCP / IP INTERNETWORKING (PE-2)

UNIT - I

Network Models: Layered Tasks, The OSI Model, Layers in OSI Model, TCP/IP Protocol suite, Addressing.

Connecting devices: Passive Hubs, Repeaters, Active Hubs, Bridges, Two Layer Switches, Routers, Three Layer Switches, Gateway, Backbone Networks.

UNIT - II

Internetworking Concepts: Principles of Internetworking, Connectionless Interconnection, Application Level Interconnection, Network Level Interconnection, Properties of the Internet, Internet Architecture, Interconnection through IP Routers

TCP, UDP & IP: TCP Services, TCP Features, Segment, A TCP Connection, Flow Control, Error Control, Congestion Control, Process to Process Communication, User Datagram, Checksum, UDP Operation, IP Datagram, Fragmentation, Options, IP Addressing: Classful Addressing, IPV6.

UNIT - III

Congestion and Quality of Service: Data Traffic, Congestion, Congestion Control, Congestion Control in TCP, Congestion Control in Frame Relay, Source Based Congestion Avoidance, DEC Bit Scheme, Quality of Service, Techniques to Improve QOS: Scheduling, Traffic Shaping, Admission Control, Resource Reservation, Integrated Services and Differentiated Services.

UNIT - IV

Queue Management: Concepts of Buffer Management, Drop Tail, Drop Front, Random Drop, Passive Buffer Management Schemes, Drawbacks of PQM, Active Queue Management: Early Random Drop, RED Algorithm.

UNIT - V

Stream Control Transmission Protocol: SCTP Services, SCTP Features, Packet Format, Flow Control, Error Control, Congestion Control.

Mobile Network Layer: Entities and Terminology, IP Packet Delivery, Agents, Addressing, Agent Discovery, Registration, Tunneling and Encapsulating, Inefficiency in Mobile IP.

Mobile Transport Layer: Classical TCP Improvements, Indirect TCP, Snooping TCP, Mobile TCP, Fast Retransmit/Fast Recovery, Transmission, Timeout Freezing, Selective Retransmission, Transaction Oriented TCP.

TEXT BOOKS:

1. Behrouz A Forouzan, “TCP/IP Protocol Suite”, 3rd Edition, TMH.
2. B.A. Forouzan, “Data communication & Networking”, 4th Edition, TMH.

REFERENCES:

1. Mahbub Hasan & Raj Jain, ” High performance TCP/IP Networking”, PHI -2005
2. Douglas. E.Comer, “Internetworking with TCP/IP “, Volume I PHI
3. Larry L. Perterson and Bruce S. Davie , “Computer Networks- A Systems Approach”, 2011, Morgan Kaufmann
4. Jochen Schiiler, “Mobile Communications” , Pearson , 2nd Edition.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. TECH. I YEAR I SEMESTER
EMBEDDED SYSTEMS

EMBEDDED SYSTEMS LABORATORY

Note: Minimum of 10 Experiments have to be conducted

Part-I

A. Write a program
   i. Write a simple program to print "hello world"
   ii. Write a simple program to show a delay.
   iii. Write a program for counting the number of times that a switch is pressed & released.
   iv. Write a c program to test loop time outs.
   v. Write a c program to test hardware based timeout loops.
   vi. Illustrate the use of port header file (port M) using an interface consisting of a keypad and liquid crystal display.
B. Write a program to create a portable hardware delay.
C. Write a loop application to copy values from P1 to P2
D. Develop a simple EOS showing traffic light sequencing.
E. Write a program to drive SEOS using Timer 0.

Part-II

The following programs are to be implemented on ARM Processor

1. Simple assembly program for addition, Subtraction, Multiplication, Division, Operating Modes, System Calls and Interrupts, Loops, Branches.
2. Write an Assembly program to configure and control general purpose input/output (GPIO) port pins
3. To read digital values from external peripherals and execute them with the target board
4. Program for reading and writing of a file
5. To demonstrate time delay program using built in timer / counter feature on IDE environment
6. To demonstrate a simple interrupt handler and setting up a timer
7. Program to demonstrate a simple interrupt handlers. Press button to generate an interrupt and trace the program flow with debug terminal
8. Program to interface 8 Bit LED and Switch Interface
9. Program to implement Buzzer Interface on IDE environment