JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. TECH. IN ELECTRONICS AND COMMUNICATION ENGINEERING.

EFFECTIVE FROM ACADEMIC YEAR 2017- 18 ADMITTED BATCH

COURSE STRUCTURE AND SYLLABUS

I Semester

Category	Course Title	Int. marks	Ext. marks	L	T	P	C
PC-1	Digital System Design	25	75	4	0	0	4
PC-2	Coding Theory and Techniques	25	75	4	0	0	4
PC-3	Advanced Digital Signal Processing	25	75	4	0	0	4
PE-1	Detection and Estimation Theory Digital Signal Processors and Architectures Speech Signal Processing	25	75	**3**	0	0	3
PE-2	Advanced Computer Architecture Real Time Operating Systems Adhoc Wireless Sensor Networks	25	75	**3**	0	0	3
OE-1	***Open Elective – I**	25	75	3	0	0	3
Laboratory I	Digital System Design Lab	25	75	0	0	3	2
Seminar I	Seminar	100	0	0	0	3	2
Total		**275**	**525**	**21**	**0**	**6**	**25**

II Semester

Category	Course Title	Int. marks	Ext. marks	L	T	P	C
PC-4	Embedded System Design	25	75	4	0	1	4
PC-5	System on Chip Architectures	25	75	4	0	1	4
PC-6	Wireless Communications and Networks	25	75	4	0	1	4
PE-3	Spread Spectrum Communications Network Security And Cryptography Adaptive Signal Processing	25	75	**3**	0	0	3
PE4	Design of Fault Tolerant Systems Image and Video Processing Optical Communications and Networks	25	75	**3**	0	0	3
OE-2	***Open Elective – II**	25	75	3	0	0	3
Laboratory II	Wireless Communications and Networks Lab	25	75	0	0	3	2
Seminar II	Seminar	100	0	0	0	3	2
Total		**275**	**525**	**21**	**0**	**6**	**25**

III Semester

Course Title	Int. marks	Ext. marks	L	T	P	C
Technical Paper Writing	100	0	0	3	0	2
Comprehensive Viva-Voce	0	100	0	0	0	4
Project work Review I	100	0	0	0	22	8
Total	**200**	**100**	0	**3**	22	**14**

IV Semester

Course Title	Int. marks	Ext. marks	L	T	P	C
Project work Review II	100	0	0	0	24	8
Project Evaluation (Viva-Voce)	0	200	0	0	0	16
Total	**100**	**200**	**0**	**0**	**24**	**24**

***Open Elective subjects must be chosen from the list of open electives offered by various departments.**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. TECH. I YEAR I SEMESTER
ELECTRONICS AND COMMUNICATION ENGINEERING

DIGITAL SYSTEM DESIGN (PC-1)

UNIT - I

Minimization and Transformation of Sequential Machines: The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines. Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

UNIT -II

Digital Design: Digital Design Using ROMs, PALs and PLAs, BCD Adder, 32 – bit adder, State graphs for control circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner, Binary divider.

UNIT -III

SM Charts: State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier, dice game controller.

UNIT -IV

Fault Modeling & Test Pattern Generation: Logic Fault model – Fault detection & Redundancy-Fault equivalence and fault location –Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model. Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults.

UNIT - V

Fault Diagnosis in Sequential Circuits: Circuit Test Approach, Transition Check Approach – State identification and fault detection experiment, Machine identification, Design of fault detection experiment

TEXT BOOKS:

1. Charles H. Roth, “Fundamentals of Logic Design”, 5th Edition, Cengage Learning.
2. Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman, “Digital Systems Testing and Testable Design”, John Wiley & Sons Inc.
3. N. N. Biswas, “Logic Design Theory”, PHI

REFERENCE BOOKS:

1. Z. Kohavi , “Switching and Finite Automata Theory”, 2nd Edition, 2001, TMH
2. Morris Mano, M.D.Ciletti, “Digital Design”, 4th Edition, PHI.
3. Samuel C. Lee , “Digital Circuits and Logic Design”, PHI

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. TECH. I YEAR I SEMESTER
ELECTRONICS AND COMMUNICATION ENGINEERING

CODING THEORY AND TECHNIQUES (PC-2)

UNIT – I

Coding for Reliable Digital Transmission and storage: Mathematical model of Information, A Logarithmic Measure of Information, Average and Mutual Information and Entropy, Types of Errors, Error Control Strategies.

Linear Block Codes: Introduction to Linear Block Codes, Syndrome and Error Detection, Minimum Distance of a Block code, Error-Detecting and Error-correcting Capabilities of a Block code, Standard array and Syndrome Decoding, Probability of an undetected error for Linear Codes over a BSC, Hamming Codes. Applications of Block codes for Error control in data storage system

UNIT - II

Cyclic Codes : Description, Generator and Parity-check Matrices, Encoding, Syndrome Computation and Error Detection, Decoding ,Cyclic Hamming Codes, Shortened cyclic codes, Error-trapping decoding for cyclic codes, Majority logic decoding for cyclic codes.

UNIT – III

Convolutional Codes: Encoding of Convolutional Codes, Structural and Distance Properties, maximum likelihood decoding, Sequential decoding, Majority- logic decoding of Convolution codes. Application of Viterbi Decoding and Sequential Decoding, Applications of Convolutional codes in ARQ system.

UNIT – IV

Turbo Codes: LDPC Codes- Codes based on sparse graphs, Decoding for binary erasure channel, Log-likelihood algebra, Brief propagation, Product codes, Iterative decoding of product codes, Concatenated convolutional codes- Parallel concatenation, The UMTS Turbo code, Serial concatenation, Parallel concatenation, Turbo decoding

UNIT - V

Space-Time Codes: Introduction, Digital modulation schemes, Diversity, Orthogonal space- Time Block codes, Alamouti's schemes, Extension to more than Two Transmit Antennas, Simulation Results, Spatial Multiplexing : General Concept, Iterative APP Preprocessing and Per-layer Decoding, Linear Multilayer Detection, Original BLAST Detection, QL Decomposition and Interface Cancellation, Performance of Multi – Layer Detection Schemes, Unified Description by Linear Dispersion Codes.

TEXT BOOKS:

1. Shu Lin, Daniel J.Costello,Jr, "Error Control Coding- Fundamentals and Applications", Prentice Hall, Inc.
2. Man Young Rhee, "Error Correcting Coding Theory", 1989, McGraw-Hill

REFERENCE BOOKS:

1. Bernard Sklar, "Digital Communications-Fundamental and Application", PE.
2. John G. Proakis, "Digital Communications", 5th Edition, 2008, TMH.
3. Salvatore Gravano, "Introduction to Error Control Codes", Oxford
4. Todd K.Moon, "Error Correction Coding – Mathematical Methods and Algorithms", 2006, Wiley India.
5. Ranjan Bose, "Information Theory, Coding and Cryptography", 2nd Edition, 2009, TMH.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. TECH. I YEAR I SEMESTER
ELECTRONICS AND COMMUNICATION ENGINEERING

ADVANCED DIGITAL SIGNAL PROCESSING (PC-3)

UNIT –I

Review of DFT, FFT, IIR Filters, and FIR Filters: Introduction to filter structures (IIR & FIR).Implementation of Digital Filters, specifically 2nd Order Narrow Band Filter and 1st Order All Pass Filter. Frequency sampling structures of FIR, Lattice structures, Forward prediction error, Backward prediction error, Reflection coefficients for lattice realization, Implementation of lattice structures for IIR filters, Advantages of lattice structures.

UNIT -II

Non-Parametric Methods: Estimation of spectra from finite duration observation of signals, Non-parametric Methods: Bartlett, Welch & Blackman-Tukey methods, Comparison of all Non-Parametric methods

UNIT - III

Parametric Methods: Autocorrelation & Its Properties, Relation between auto correlation & model parameters, AR Models - Yule-Walker & Burg Methods, MA & ARMA models for power spectrum estimation, Finite word length effect in IIR digital Filters – Finite word-length effects in FFT algorithms.

UNIT –IV

Multi Rate Signal Processing: Introduction, Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Multistage Implementation of Sampling Rate Conversion, Filter design & Implementation for sampling rate conversion. Examples of up-sampling using an All Pass Filter.

UNIT –V

Applications of Multi Rate Signal Processing: Design of Phase Shifters, Interfacing of Digital Systems with Different Sampling Rates, Implementation of Narrow Band Low Pass Filters, Implementation of Digital Filter Banks, Sub band Coding of Speech Signals, Quadrature Mirror Filters, Trans multiplexers, Over Sampling A/D and D/A Conversion.

TEXT BOOKS:

1. J.G.Proakis & D. G. Manolakis, “Digital Signal Processing: Principles, Algorithms & Applications”, 4th Edition, PHI.
2. Alan V Oppenheim & Ronald W Schaffer, “Discrete Time signal processing”, PHI.
3. Emmanuel C. Ifeacher, Barrie. W. Jervis, “DSP A Practical Approach”, 2nd Edition. Pearson Education.

REFERENCE BOOKS:

1. S. M .Kay, “Modern spectral Estimation: Theory & Application”, 1988, PHI.
2. P. P. Vaidyanathan, “Multi Rate Systems and Filter Banks”, Pearson Education.
3. Kaluri V. Rangarao, Ranjan K. Mallik, “Digital Signal Processing: A Practitioner's Approach”, ISBN: 978-0-470-01769-2, 210 pages, November 2006 John Wiley.
4. S. Salivahanan, A. Vallavaraj, C.Gnanapriya, “Digital Signal Processing”, 2000,TMH

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. TECH. I YEAR I SEMESTER
ELECTRONICS AND COMMUNICATION ENGINEERING

DETECTION AND ESTIMATION THEORY (PE-1)

UNIT –I
Random Processes: Discrete Linear Models, Markov Sequences and Processes, Point Processes, and Gaussian Processes.

UNIT –II
Detection Theory: Basic Detection Problem, Maximum A posteriori Decision Rule, Minimum Probability of Error Classifier, Bayes Decision Rule, Multiple-Class Problem (Bayes)- minimum probability error with and without equal a priori probabilities, Neyman-Pearson Classifier, General Calculation of Probability of Error, General Gaussian Problem, Composite Hypotheses.

UNIT –III:
Linear Minimum Mean-Square Error Filtering: Linear Minimum Mean Squared Error Estimators, Nonlinear Minimum Mean Squared Error Estimators. Innovations, Digital Wiener Filters with Stored Data, Real-time Digital Wiener Filters, Kalman Filters.

UNIT –IV
Statistics: Measurements, Nonparametric Estimators of Probability Distribution and Density Functions, Point Estimators of Parameters, Measures of the Quality of Estimators, Introduction to Interval Estimates, Distribution of Estimators, Tests of Hypotheses, Simple Linear Regression, Multiple Linear Regression.

UNIT –V
Estimating the Parameters of Random Processes from Data: Tests for Stationarity and Ergodicity, Model-free Estimation, Model-based Estimation of Autocorrelation Functions, Power Special Density Functions.

TEXT BOOKS:

1. K. Sam Shanmugan & A.M. Breipohl, “Random Signals: Detection, Estimation and Data Analysis”, Wiley India Pvt. Ltd, 2011.
2. Lonnie C. Ludeman, “Random Processes: Filtering, Estimation and Detection”, Wiley India Pvt. Ltd., 2010.

REFERENCE BOOKS:

1. Steven.M.Kay, “Fundamentals of Statistical Signal Processing: Volume I Estimation Theory”, Prentice Hall, USA, 1998.
2. Steven.M.Kay, “Fundamentals of Statistical Signal Processing: Volume I Detection Theory Prentice”, Hall, USA, 1998.
3. Srinath, Rajasekaran, Viswanathan, “Introduction to Statistical Signal Processing with Applications”, 2003, PHI.
4. Louis L.Scharf, “Statistical Signal Processing: Detection, Estimation and Time Series Analysis”, 1991, Addison Wesley.
5. Harry L. Van Trees, “Detection, Estimation and Modulation Theory: Part – I”, 2001, John Wiley & Sons, USA.
6. Mischa Schwartz, Leonard Shaw, “Signal Processing: Discrete Spectral Analysis – Detection & Estimation”, 1975, Mc Graw Hill.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. TECH. I YEAR I SEMESTER
ELECTRONICS AND COMMUNICATION ENGINEERING

DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES (PE-1)

UNIT-I

Introduction to Digital Signal Processing: Introduction, A digital Signal – Processing system, the sampling process, discrete time sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), linear time-invariant systems, Digital filters, Decimation and interpolation.

Architectures for Programmable DSP devices: Basic Architectural features, DSP computational building blocks, Bus Architecture and Memory, Data addressing capabilities, Address generation UNIT, programmability and program execution, speed issues, features for external interfacing.

UNIT-II

Programmable Digital Signal Processors: Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX processors, memory space of TMS320C54XX processors, program control, TMS320C54XX instructions and programming, On-Chip peripherals, Interrupts of TMS320C54XX processors, Pipeline operation of TMS320C54XX processors.

UNIT-III

Architecture of ARM Processors: Introduction to the architecture, Programmer's model- operation modes and states, registers, special registers, floating point registers, Behavior of the application program status register(APSR)-Integer status flags, Q status flag, GE bits, Memory system-Memory system features, memory map, stack memory, memory protection unit (MPU), Exceptions and Interrupts-what are exceptions?, nested vectored interrupt controller(NVIC), vector table, Fault handling, System control block (SCB), Debug, Reset and reset sequence.

Technical Details of ARM Processors: General information about Cortex-M3 and cortex M4 processors-Processor type, processor architecture, instruction set, block diagram, memory system, interrupt and exception support, Features of the cortex-M3 and Cortex-M4 Processors-Performance, code density, low power, memory system, memory protection unit, interrupt handling, OS support and system level features, Cortex-M4 specific features, Ease of use, Debug support, Scalability, Compatibility.

UNIT-IV

Instruction SET: Background to the instruction set in ARM Cortex-M Processors, Comparison of the instruction set in ARM Cortex-M Processors, understanding the assembly language syntax, Use of a suffix in instructions, Unified assembly Language (UAL), Instruction set, Cortex-M4-specific instructions, Barrel shifter, Accessing special instructions and special registers in Programming.

UNIT-V

Floating Point Operations: About Floating Point Data,Cortex-M4 Floating Point Unit (FPU)-overview, FP registers overview, CPACR register, Floating point register bank, FPSCR, FPU->FPCCR, FPU-> FPCAR, FPU->FPDSCR, FPU->MVFR0, FPU->MVFR1.

TEXTBOOKS:

1. Avtar Singh and S. Srinivasan, "Digital Signal Processing", CENGAGE Learning, 2004.
2. Joseph Yiu, "The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors", Elsevier Publications, 3rd Edition.

REFERENCES:

1. Andrew N. SLOSS, Dominic SYMES, Chris WRIGHT, “ARM System Developer’s Guide Designing and Optimizing System Software”, Elsevier Publications, 2004.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. TECH. I YEAR I SEMESTER
ELECTRONICS AND COMMUNICATION ENGINEERING

SPEECH SIGNAL PROCESSING (PE-1)

UNIT –I

Fundamentals of Digital Speech Processing: Anatomy & Physiology of Speech Organs, The process of Speech Production, Acoustic Phonetics, Articulatory Phonetics, The Acoustic Theory of Speech Production- Uniform lossless tube model, effect of losses in vocal tract, effect of radiation at lips, Digital models for speech signals.

UNIT –II

Time Domain Models for Speech Processing: Introduction- Window considerations, Short time energy and average magnitude Short time average zero crossing rate, Speech Vs Silence discrimination using energy and zero crossing, Pitch period estimation using a parallel processing approach, The short time autocorrelation function, The short time average magnitude difference function, Pitch period estimation using the autocorrelation function.

UNIT –III

Linear Predictive Coding (LPC) Analysis: Basic principles of Linear Predictive Analysis: The Autocorrelation Method, The Covariance Method, Solution of LPC Equations: Cholesky Decomposition Solution for Covariance Method, Durbin's Recursive Solution for the Autocorrelation Equations, Comparison between the Methods of Solution of the LPC Analysis Equations, Applications of LPC Parameters: Pitch Detection using LPC Parameters, Formant Analysis using LPC Parameters.

UNIT –IV

Homomorphic Speech Processing: Introduction, Homomorphic Systems for Convolution: Properties of the Complex Cepstrum, Computational Considerations, The Complex Cepstrum of Speech, Pitch Detection, Formant Estimation, The Homomorphic Vocoder.

Speech Enhancement: Nature of interfering sounds, Speech enhancement techniques: Single Microphone Approach : spectral subtraction, Enhancement by re-synthesis, Comb filter, Wiener filter, Multi microphone Approach.

UNIT-V

Automatic Speech & Speaker Recognition: Basic pattern recognition approaches, Parametric representation of speech, Evaluating the similarity of speech patterns, Isolated digit Recognition System, Continuous digit Recognition System.

Hidden Markov Model (HMM) for Speech: Hidden Markov Model (HMM) for speech recognition, Viterbi algorithm, Training and testing using HMMS.

Speaker Recognition: Recognition techniques, Features that distinguish speakers, Speaker Recognition Systems: Speaker Verification System, Speaker Identification System.

TEXT BOOKS:

1. L.R. Rabiner and S. W. Schafer, "Digital Processing of Speech Signals", Pearson Education.
2. Douglas O'Shaughnessy, "Speech Communications: Human & Machine", 2nd Ed., Wiley India, 2000.
3. L.R Rabinar and R W Jhaung, "Digital Processing of Speech Signals", 1978, Pearson Education.

REFERENCE BOOKS:

1. Thomas F. Quateri, “Discrete Time Speech Signal Processing: Principles and Practice”, 1st Edition., PE.
2. Ben Gold & Nelson Morgan, “Speech & Audio Signal Processing”, 1st Edition, Wiley.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. TECH. I YEAR I SEMESTER
ELECTRONICS AND COMMUNICATION ENGINEERING

ADVANCED COMPUTER ARCHITECTURE (PE-2)

UNIT- I

Fundamentals of Computer Design: Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law. Instruction set principles and examples- Introduction, classifying instruction set- memory addressing- type and size of operands, operations in the instruction set.

UNIT – II

Pipelines: Introduction ,basic RISC instruction set ,Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining , Pipeline hazards, Reducing pipeline branch penalties.

Memory Hierarchy Design: Introduction, review of ABC of cache, Cache performance , Reducing cache miss penalty, Virtual memory.

UNIT - III

Instruction Level Parallelism the Hardware Approach: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.

ILP Software Approach: Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT – IV

Multi Processors and Thread Level Parallelism: Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT – V

Inter Connection and Networks: Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

Intel Architecture: Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls

TEXT BOOKS:

1. John L. Hennessy, David A. Patterson, "Computer Architecture: A Quantitative Approach", 3rd Edition, An Imprint of Elsevier.

REFERENCE BOOKS:

1. John P. Shen and Miikko H. Lipasti, "Modern Processor Design: Fundamentals of Super Scalar Processors", 2002, Beta Edition, McGraw Hill.
2. Kai Hwang, Faye A.Brigs., "Computer Architecture, and Parallel Processing", MC Graw Hill.,
3. Dezso Sima, Terence Fountain, Peter Kacsuk , "Advanced Computer Architecture - A Design Space Approach", Pearson Education.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. TECH. I YEAR I SEMESTER
ELECTRONICS AND COMMUNICATION ENGINEERING

REAL TIME OPERATING SYSTEMS (PE-2)

UNIT – I

Introduction: Introduction to UNIX/LINUX, Overview of Commands, File I/O,(open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT - II

Real Time Operating Systems: Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency. Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

UNIT - III

Objects, Services and I/O: Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

UNIT - IV

Exceptions, Interrupts and Timers: Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT - V

Case Studies of RTOS: RT Linux, Micro C/OS-II, Vx Works, Embedded Linux, and Tiny OS.

TEXT BOOK:

1. Qing Li, “Real Time Concepts for Embedded Systems”, 2011, Elsevier.

REFERENCE BOOKS:

1. Rajkamal, “Embedded Systems- Architecture, Programming, and Design”, 2007, TMH.
2. W. Richard Stevens, Stephan A. Rago, “Advanced UNIX Programming”, 2006, 2nd Edition, Pearson.
3. Dr. Craig Hollabaugh, “Embedded Linux: Hardware, Software and Interfacing”, 2008, 1st Edition, Pearson.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. TECH. I YEAR I SEMESTER
ELECTRONICS AND COMMUNICATION ENGINEERING

ADHOC WIRELESS SENSOR NETWORKS (PE-2)

UNIT –I

Wireless Local Area Networks: Introduction, wireless LAN Topologies, Wireless LAN Requirements, Physical Layer- Infrared Physical Layer, Microwave based Physical Layer Alternatives, Medium Access Control Layer- HIPERLAN 1 Sublayer, IEEE 802.11 MAC Sublayer and Latest Developments- 802.11a, 802.11b, 802.11g

Personal Area Networks: Introduction to PAN technology and Applications, Bluetooth - specifications, Radio Channel, Piconets and Scatternets, Inquiry, Paging and Link Establishment, Packet Format, Link Types, Power Management, Security, Home RF -Physical and MAC Layer

UNIT -II

Ad-Hoc Wireless Networks: Introduction; Cellular and Ad-Hoc Wireless Networks; Issues in Ad-Hoc Wireless Networks: Medium Access Scheme, Routing, Multicasting, Transport Layer Protocols, Quality of Service Provisioning, Energy Management, Scalability

UNIT -III

Medium Access Control Protocols: Introduction; Issues in Designing a MAC protocol: Bandwidth efficiency, Quality of Service support, Synchronization, Hidden and exposed terminal problems, Error prone shared broadcast channel, mobility nodes; Design goals of a MAC protocol; Classification of MAC protocols; Contention-based protocols: MACAW, Floor acquisition multiple access protocol, Busy tone multiple access protocols, MACA by invitation, Media access with reduced handshake; Contention-based protocols with reservation mechanisms; Contention-based MAC protocols with scheduling mechanisms; MAC protocols that use directional antennas

UNIT -IV

Routing and Transport Layer Protocols: Introduction, issues in designing a routing protocol, Classification of routing protocols, Table-driven protocols, On-demand routing protocols, Hybrid routing protocols, Routing with efficient flooding mechanisms, Hierarchical routing protocols, Power-aware routing protocols; Introduction to transport layer protocols, design issues and goals of transport layer protocol, Classification of transport layer solutions

UNIT -V

Wireless Sensor Networks: Introduction, Sensor Network Architecture, Data Dissemination, Data gathering, MAC protocols for Sensor Networks, Location Discovery, Quality of a Sensor Network

TEXT BOOKS:

1. C. Siva Ram Murthy, “Ad Hoc Wireless Networks”, 2004, Pearson Education.
2. P Nicopolitidis and M S Obaidat, “Wireless Networks”, Wiley India Edition 2003.

REFERENCE BOOKS:

1. C.K. Toh, “Ad-Hoc Mobile Wireless Networks: Protocols and Systems”, 1st Edition, Pearson Education.
2. Carlos de Morais Cordeiro and Dharma Prakash Agrawal, “Ad Hoc and Sensor Networks”, 2011, World Scientific.
3. Kazen Sohraby, Daniel Minoli, Taieb Znati, “Wireless Sensor Networks”, 1991, Wiley Student Edition

4. C.S. Raghavendra, Krishna M. SivaLingam, “Wireless Sensor Networks”, 2004, Springer.
5. Jagannathan Sarangapani, “Wireless Ad- hoc and Sensor Networks: Protocols, Performance and Control”, CRC Press

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. TECH. I YEAR I SEMESTER
ELECTRONICS AND COMMUNICATION ENGINEERING

DIGITAL SYSTEM DESIGN LAB

Part –I

Programming can be done using any complier. Down load the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels) and logic analyzer apart from verification by simulation with any of the front end tools.

1. HDL code to realize all the logic gates
2. Design and Simulation of adder, Serial Binary Adder, Multi Precession Adder, Carry
3. Look Ahead Adder.
4. Design of 2-to-4 decoder
5. Design of 8-to-3 encoder (without and with parity)
6. Design of 8-to-1 multiplexer
7. Design of 4 bit binary to gray converter
8. Design of Multiplexer/ Demultiplexer, comparator
9. Design of Full adder using 3 modeling styles
10. Design of flip flops: SR, D, JK, T
11. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset) or any sequence counter
12. Design of a N- bit Register of Serial- in Serial –out, Serial in parallel out, Parallel in
13. Serial out and Parallel in Parallel Out.
14. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
15. Design of 4- Bit Multiplier, Divider.
16. Design of ALU to Perform – ADD, SUB, AND-OR, 1's and 2's Compliment,
17. Multiplication and Division.
18. Design of Finite State Machine.
19. Implementing the above designs on Xilinx/Altera/Cypress/equivalent based FPGA/CPLD kits .

Part –II

1. Static and Dynamic Characteristics of CMOS Inverter
2. Implementation of EX-OR gate using complementary CMOS, Psuedo-NMOS, Dynamic and domino logic style
3. Implementation of Full Adder using Transmission Gates