JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. TECH IN VLSI/ VLSI DESIGN/VLSI SYSTEM DESIGN.
EFFECTIVE FROM ACADEMIC YEAR 2017- 18 ADMITTED BATCH

COURSE STRUCTURE AND SYLLABUS

I Semester

Category	Course Title	Int. marks	Ext. marks	L	T	P	C
PC-1	Advanced Digital System Design	25	75	4	0	0	4
PC-2	Device Modeling	25	75	4	0	0	4
PC-3	CMOS Analog Integrated Circuit Design	25	75	4	0	0	4
PE-1	VLSI Technology Hardware Software Co-Design CPLD and FPGA Architectures and Applications	25	75	**3**	0	0	3
PE-2	Algorithms for VLSI Design Automation Embedded System Design Advanced Computer Architecture	25	75	**3**	0	0	3
OE-1	***Open Elective – I**	25	75	3	0	0	3
Laboratory I	Digital IC Design Lab	25	75	0	0	3	2
Seminar I	Seminar	100	0	0	0	3	2
Total		**275**	**525**	**21**	**0**	**6**	**25**

II Semester

Category	Course Title	Int. marks	Ext. marks	L	T	P	C
PC-4	Low Power VLSI Design	25	75	4	0	0	4
PC-5	Design for Testability	25	75	4	0	0	4
PC-6	CMOS Mixed Signal Circuit Design	25	75	4	0	0	4
PE-3	VLSI and DSP Architectures Full custom IC Design Verilog Hardware Description Language	25	75	**3**	0	0	3
PE4	RF IC Design System On Chip Architecture Scripting Languages	25	75	**3**	0	0	3
OE-2	***Open Elective – II**	25	75	3	0	0	3
Laboratory II	Analog IC Design Lab	25	75	0	0	3	2
Seminar II	Seminar	100	0	0	0	3	2
Total		**275**	**525**	**21**	**0**	**6**	**25**

III Semester

Course Title	Int. marks	Ext. marks	L	T	P	C
Technical Paper Writing	100	0	0	3	0	2
Comprehensive Viva-Voce	0	100	0	0	0	4
Project work Review II	100	0	0	0	22	8
Total	**200**	**100**	0	**3**	22	**14**

IV Semester

Course Title	Int. marks	Ext. marks	L	T	P	C
Project work Review III	100	0	0	0	24	8
Project Evaluation (Viva-Voce)	0	100	0	0	0	16
Total	**100**	**100**	**0**	**0**	**24**	**24**

***Open Elective subjects must be chosen from the list of open electives offered by OTHER departments.**

 # For Project review I, please refer 7.10 in R17 Academic Regulations.

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M. TECH. – I YEAR – I SEMESTER
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ADVANCED DIGITAL SYSTEM DESIGN (PC-1)

UNIT - I
Processor Arithmetic: Two's Complement Number System - Arithmetic Operations; Fixed point Number System; Floating Point Number system - IEEE 754 format, Basic binary codes.

UNIT - II
Combinational circuits: CMOS logic design, Static and dynamic analysis of Combinational circuits, timing hazards. Functional blocks - Decoders, Encoders, Three-state devices, Multiplexers, Parity circuits, Comparators, Adders, Subtractors, Carrylook- ahead adder – timing analysis.Combinational multiplier structures.

UNIT - III
Sequential Logic: Latches and Flip-Flops, Sequential logic circuits - timing analysis (Set up and hold times), State machines - Mealy & Moore machines, Analysis, FSM design using D Flip-Flops, FSM optimization and partitioning; Synchronizers and metastability. FSM Design examples: Vending machine, Traffic light controller, Washing machine.

UNIT - IV
Subsystem Design using Functional Blocks (1): Design (including Timing Analysis) of different logical blocks of varying complexities involving mostly combinational circuits:

- ALU
- 4-bit combinational multiplier
- Barrel shifter
- Simple fixed point to floating point encoder
- Dual Priority encoder
- Cascading comparators

UNIT - V
Subsystem Design using Functional Blocks (2): Design, (including Timing Analysis) of different logical blocks of different complexities involving mostly sequential circuits:

- Pattern (sequence) detector
- Programmable Up-down counter
- Round robin arbiter with 3 requesters
- Process Controller
- FIFO

TEXT BOOKS:

1. John F. Wakerly, “Digital Design”, Prentice Hall, 3rd Edition, 2002

*Note1: VHDL and ABEL are not part of this course.
*Note2: SSI & MSI ICs listed in data books are not part of this course.

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M. TECH. – I YEAR – I SEMESTER
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DEVICE MODELING (PC-2)

UNIT - I
MOS Capacitor: Energy band diagram of Metal-Oxide-Semiconductor contacts, Mode of Operations: Accumulation, Depletion, Mid gap, and Inversion, 1D Electrostatics of MOS, Depletion Approximation, Accurate Solution of Poisson's Equation.

UNIT - II
MOS Capacitor Characteristics and Non idealities: CV characteristics of MOS, LFCV and HFCV, Non-idealities in MOS, oxide fixed charges, interfacial charges.

UNIT - III
The MOS transistor: Small signal modeling for low frequency and High frequency, Pao-Sah and Brews models; Short channel effects in MOS transistors.

UNIT - IV
The bipolar transistor: Eber's-Moll model; charge control model; small-signal models for low and high frequency and switching characteristics.

UNIT - V
FinFETs: I-V characteristics, device capacitances, parasitic effects of extension regions, performance of simple combinational gates and amplifiers, novel circuits using FinFETs and GAA devices.

TEXT BOOKS:

1. S. M. Sze, "Physics of Semiconductor Devices", 2nd Edition, Wiley Eastern, 1981.
2. Y. P. Tsividis, "Operation and Modelling of the MOS Transistor", McGraw-Hill, 1987.
3. E. Takeda, "Hot-carrier Effects in MOS Transistors", Academic Press, 1995.
4. P. Colinge, "FinFETs and Other Multi-Gate Transistors", Springer. 2009

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M. TECH. – I YEAR – I SEMESTER
VLSI/ VLSI DESIGN/VLSI SYSTEM DESIGN

CMOS ANALOG INTEGRATED CIRCUIT DESIGN (PC-3)

UNIT -I

MOS Devices and Modeling: The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT -II

Analog CMOS Sub-Circuits: MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT -III

CMOS Amplifiers: Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT -IV

CMOS Operational Amplifiers: Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power- Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT -V

Comparators: Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:

1. Philip E. Allen and Douglas R. Holberg, “CMOS Analog Circuit Design”, Oxford University Press, International 2nd Edition/Indian Edition, 2010.
2. Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, “Analysis and Design of Analog Integrated Circuits”, Wiley India, 5th Edition, 2010.

REFERENCE BOOKS:

1. David A. Johns, Ken Martin, “Analog Integrated Circuit Design”, Wiley Student Edition, 2013.
2. Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, TMH Edition.
3. Baker, Li and Boyce, “CMOS: Circuit Design, Layout and Simulation”, PHI.

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M. TECH. – I YEAR – I SEMESTER
VLSI/ VLSI DESIGN/VLSI SYSTEM DESIGN

VLSI TECHNOLOGY (PE-1)

UNIT –I

Review of Microelectronics and Introduction to MOS Technologies: MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: Ids – Vds relationships, Threshold Voltage VT, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT –II

Layout Design and Tools: Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

Logic Gates & Layouts: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT –III

Overview of semiconductor industry, Stages of Manufacturing, Process and product trends, Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Basic wafer fabrication operations, Yield measurement, Contamination sources, Clean room construction, Oxidation and Photolithography, Doping and Depositions, Metallization.Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hard bake, develop inspect, Dry etching Wet etching, resist stripping

UNIT –IV

Doping and depositions: Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2, CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapour phase epitoxy, molecular beam epitaxy.

UNIT –V

Design rules and Scaling, BICMOS ICs: Choice of transistor types, pnp transistors, Resistors, capacitors,

Packaging: Chip characteristics, package functions, package operations

TEXT BOOKS:

1. Peter Van Zant, “Microchip fabrication”, McGraw Hill, 1997.
2. C.Y. Chang and S.M. Sze, “ULSI technology”, McGraw Hill, 2000

REFERENCE BOOKS:

1. Muhammad H Rashid, “Micro Electronics circuits Analysis and Design”, 2nd Edition, CENAGE Learning, 2011.
2. Eugene D. Fabricius, “Introduction to VLSI design”, McGraw Hill, 1999
3. Wani-Kai Chen (editor), “The VLSI Hand book”, CRI/IEEE press, 2000
4. S.K. Gandhi, “VLSI Fabrication principles”, John Wiley and Sons, NY, 1994

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M. TECH. – I YEAR – I SEMESTER
VLSI/ VLSI DESIGN/VLSI SYSTEM DESIGN

HARDWARE SOFTWARE CO-DESIGN (PE-1)

UNIT –I

Co- Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT –II

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT –III

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT –IV

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT –V

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi-language co-simulation, the cosyma system and lycos system.

TEXT BOOKS:

1. Jorgen Staunstrup, “Hardware / Software Co- Design Principles and Practice”, Wayne Wolf – 2009, Springer.
2. Giovanni De Micheli, Mariagiovanna Sami, “Hardware / Software Co- Design”, 2002, Kluwer Academic Publishers

REFERENCE BOOKS:

1. Patrick R. Schaumont, “A Practical Introduction to Hardware/Software Co-design”, 2010, Springer

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M. TECH. – I YEAR – I SEMESTER
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CPLD AND FPGA ARCHITECTURES AND APPLICATIONS (PE-1)

UNIT-I

Introduction to Programmable Logic Devices: Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT-II

Field Programmable Gate Arrays: Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT -III

SRAM Programmable FPGAs: Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT -IV

Anti-Fuse Programmed FPGAs: Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT -V

Design Applications: General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:

1. Stephen M. Trimberger, “Field Programmable Gate Array Technology”, Springer International Edition.
2. Charles H. Roth Jr, Lizy Kurian John, “Digital Systems Design”, Cengage Learning.

REFERENCE BOOKS:

1. John V. Oldfield, Richard C. Dorf, “Field Programmable Gate Arrays”, Wiley India.
2. Pak K. Chan/Samiha Mourad, “Digital Design Using Field Programmable Gate Arrays”, Pearson Low Price Edition.
3. Ian Grout, “Digital Systems Design with FPGAs and CPLDs”, Elsevier, Newnes.
4. Wayne Wolf, “Modern Semiconductor Design Series”, Prentice Hall.

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M. TECH. – I YEAR – I SEMESTER
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ALGORITHMS FOR VLSI DESIGN AUTOMATION (PE-2)

UNIT- I
PRELIMINARIES: Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems**.**

UNIT -II
GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION: Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT- III
LAYOUT COMPACTION, PLACEMENT, FLOOR PLANNING AND ROUTING: Problems, Concepts and Algorithms.
MODELLING AND SIMULATION: Gate Level Modelling and Simulation, Switch level Modelling and Simulation.

UNIT -IV
LOGIC SYNTHESIS AND VERIFICATION: Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis.
HIGH-LEVEL SYNTHESIS: Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High-level Transformations.

UNIT- V
PHYSICAL DESIGN AUTOMATION OF FPGAs: FPGA technologies, Physical Design cycle for FPGAs, partitioning and Routing for segmented and staggered Models.
PHYSICAL DESIGN AUTOMATION OF MCMs : MCM technologies, MCM physical design cycle, Partitioning, Placement - Chip Array based and Full Custom Approaches, Routing – Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, Routing and Programmable MCMs.

TEXT BOOKS:

1. S.H. Gerez, “Algorithms for VLSI Design Automation”, 1999, WILEY Student Edition, John Wiley & Sons (Asia) Pvt. Ltd.
2. Naveed Sherwani, “Algorithms for VLSI Physical Design Automation”, 3rd Edition, 2005, Springer International Edition.

REFERENCE BOOKS:

1. Hill & Peterson, “Computer Aided Logical Design with Emphasis on VLSI”, 1993, Wiley.
2. Wayne Wolf, “Modern VLSI Design: Systems on silicon”, 2nd ed., 1998, Pearson Education Asia.

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M. TECH. – I YEAR – I SEMESTER
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EMBEDDED SYSTEM DESIGN (PE-2)

UNIT -I

Introduction to Embedded Systems: Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

UNIT -II

Typical Embedded System: Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT -III

Embedded Firmware: Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT -IV

RTOS Based Embedded System Design: Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT -V

Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

TEXT BOOKS:

1. Shibu K.V, “Introduction to Embedded Systems”, McGraw Hill.

REFERENCE BOOKS:

1. Raj Kamal, “Embedded Systems”, TMH.
2. Frank Vahid, Tony Givargis, “Embedded System Design”, John Wiley.
3. Lyla, “Embedded Systems”, Pearson, 2013
4. David E. Simon, “An Embedded Software Primer”, Pearson Education.

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ADVANCED COMPUTER ARCHITECTURE (PE-2)

UNIT- I

Fundamentals of Computer Design: Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law.
Instruction set principles and examples- Introduction, classifying instruction set- memory addressing-type and size of operands, operations in the instruction set.

UNIT – II

Pipelines: Introduction ,basic RISC instruction set ,Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining , Pipeline hazards, Reducing pipeline branch penalties.
Memory Hierarchy Design: Introduction, review of ABC of cache, Cache performance , Reducing cache miss penalty, Virtual memory.

UNIT - III

Instruction Level Parallelism the Hardware Approach: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.
ILP Software Approach: Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT – IV

Multi Processors and Thread Level Parallelism: Multi Processors and Thread level Parallelism-Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT – V

Inter Connection and Networks: Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.
Intel Architecture: Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls

TEXT BOOKS:

1. John L. Hennessy, David A. Patterson, "Computer Architecture: A Quantitative Approach", 3rd Edition, An Imprint of Elsevier.

REFERENCE BOOKS:

1. John P. Shen and Miikko H. Lipasti, "Modern Processor Design : Fundamentals of Super Scalar Processors",
2. Kai Hwang, Faye A.Brigs., "Computer Architecture and Parallel Processing", McGraw Hill.,
3. DezsoSima, Terence Fountain, Peter Kacsuk , "Advanced Computer Architecture - A Design Space Approach", Pearson Education.

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DIGITAL IC DESIGN LAB

Part –I

Programming can be done using any complier. Down load the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels) and logic analyzer apart from verification by simulation with any of the front end tools.

1. HDL code to realize all the logic gates
2. Design and Simulation of adder, Serial Binary Adder, Multi Precession Adder, Carry
3. Look Ahead Adder.
4. Design of 2-to-4 decoder
5. Design of 8-to-3 encoder (without and with parity)
6. Design of 8-to-1 multiplexer
7. Design of 4 bit binary to gray converter
8. Design of Multiplexer/ Demultiplexer, comparator
9. Design of Full adder using 3 modeling styles
10. Design of flip flops: SR, D, JK, T
11. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset) or any sequence counter
12. Design of a N- bit Register of Serial- in Serial –out, Serial in parallel out, Parallel in
13. Serial out and Parallel in Parallel Out.
14. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
15. Design of 4- Bit Multiplier, Divider.
16. Design of ALU to Perform – ADD, SUB, AND-OR, 1's and 2's Compliment,
17. Multiplication, and Division.
18. Design of Finite State Machine.
19. Implementing the above designs on Xilinx/Altera/Cypress/equivalent based FPGA/CPLD kits

Part –II

1. Static and Dynamic Characteristics of CMOS Inverter
2. Implementation of EX-OR gate using complementary CMOS, Psedo-NMOS, Dynamic and domino logic style
3. Implementation of Full Adder using Transmission Gates