JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. TECH IN DIGITAL ELECTRONICS AND COMMUNICATION ENGINEERING/ DIGITAL ELECTRONICS AND COMMUNICATION SYSTEMS

EFFECTIVE FROM ACADEMIC YEAR 2017- 18 ADMITTED BATCH

COURSE STRUCTURE AND SYLLABUS

I Semester

Category	Course Title	Int. marks	Ext. marks	L	T	P	C
PC-1	Advanced Digital System Design	25	75	4	0	0	4
PC-2	Coding Theory and Techniques	25	75	4	0	0	4
PC-3	Broadband Communications	25	75	4	0	0	4
PE-1	Real Time Operating Systems Image and Video Processing Spread Spectrum Communications	25	75	**3**	0	0	3
PE-2	Advanced Computer Architecture Advanced Digital Signal Processing Optical Communications and Networks	25	75	**3**	0	0	3
OE-1	***Open Elective – I**	25	75	3	0	0	3
Laboratory I	Digital System Design Lab	25	75	0	0	3	2
Seminar I	Seminar - I	100	0	0	0	3	2
Total		**275**	**525**	**21**	**0**	**6**	**25**

II Semester

Category	Course Title	Int. marks	Ext. marks	L	T	P	C
PC-4	Design of Fault Tolerant Systems	25	75	4	0	0	4
PC-5	Detection and Estimation Theory	25	75	4	0	0	4
PC-6	Wireless Communications and Networks	25	75	4	0	0	4
PE-3	System on Chip Architecture Software Defined Radio Cellular and Mobile Communications	25	75	**3**	0	0	3
PE4	Network Security And Cryptography Digital Signal Processors and Architectures EMI / EMC	25	75	**3**	0	0	3
OE-2	***Open Elective – II**	25	75	3	0	0	3
Laboratory II	Wireless Communications and Networks Lab	25	75	0	0	3	2
Seminar II	Seminar - II	100	0	0	0	3	2
Total		**275**	**525**	**21**	**0**	**6**	**25**

III Semester

Course Title	Int. marks	Ext. marks	L	T	P	C
Technical Paper Writing	100	0	0	3	0	2
Comprehensive Viva-Voce	0	100	0	0	0	4
Project work Review II	100	0	0	0	22	8
Total	**200**	**100**	0	**3**	22	**14**

IV Semester

Course Title	Int. marks	Ext. marks	L	T	P	C
Project work Review III	100	0	0	0	24	8
Project Evaluation (Viva-Voce)	0	100	0	0	0	16
Total	**100**	**100**	**0**	**0**	**24**	**24**

***Open Elective subjects must be chosen from the list of open electives offered by OTHER departments.**

 # For Project review I, please refer 7.10 in R17 Academic Regulations.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. TECH. I YEAR II SEMESTER DECE/DECS

DESIGN OF FAULT TOLERANT SYSTEMS (PC - 4)

UNIT - I

Fault Tolerant Design: Basic concepts: Reliability concepts, Failures & faults, Reliability and Failure rate, Relation between reliability and mean time between failure, maintainability and availability, reliability of series, parallel and parallel-series combinational circuits.
Fault Tolerant Design: Basic concepts-static, dynamic, hybrid, triple modular redundant system (TMR), 5MR reconfiguration techniques, Data redundancy, Time redundancy and software Redundancy concepts. [TEXTBOOK-1]

UNIT - II

Self Checking circuits & Fail safe Design: Self Checking Circuits: Basic concepts of self checking circuits, Design of Totally self checking checker, Checkers using m out of n codes, Berger code, Low cost residue code.
Fail Safe Design: Strongly fault secure circuits, fail safe design of sequential circuits using partition theory and Berger code, totally self checking PLA design. [TEXTBOOK-1]

UNIT - III

Design for Testability: Design for testability for combinational circuits: Basic concepts of Testability, Controllability and observability, The Reed Muller's expansion technique, use of control and syndrome testable designs.
Design for testability by means of scan: Making circuits Testable, Testability Insertion, Full scan DFT technique- Full scan insertion, flip-flop Structures, Full scan design and Test, Scan Architectures-full scan design, Shadow register DFT, Partial scan methods, multiple scan design, other scan designs.[TEXTBOOK-2]

UNIT - IV

Logic Built-in-self-test: BIST Basics-Memory-based BIST,BIST effectiveness, BIST types, Designing a BIST, Test Pattern Generation-Engaging TPGs, exhaustive counters, ring counters, twisted ring counter, Linear feedback shift register, Output Response Analysis-Engaging ORA's, One's counter, transition counter, parity checking, Serial LFSRs, Parallel Signature analysis, BIST architectures-BIST related terminologies, A centralised and separate Board-level BIST architecture, Built-in evaluation and self test(BEST), Random Test socket(RTS), LSSD On-chip self test, Self – testing using MISR and SRSG, Concurrent BIST, BILBO, Enhancing coverage, RT level BIST design-CUT design, simulation and synthesis, RTS BIST insertion, Configuring the RTS BIST, incorporating configurations in BIST, Design of STUMPS, RTS and STUMPS results. [TEXTBOOK-2]

UNIT - V

Standard IEEE Test Access Methods: Boundary Scan Basics, Boundary scan architecture- Test access port, Boundary scan registers, TAP controller, the decoder unit, select and other units, Boundary scan Test Instructions-Mandatory instructions, Board level scan chain structure-One serial scan chain, multiple-scan chain with one control test port, multiple-scan chains with one TDI,TDO but multiple TMS, Multiple-scan chain, multiple access port, RT Level boundary scan-inserting boundary scan test hardware for CUT, Two module test case, virtual boundary scan tester, Boundary Scan Description language. [TEXTBOOK-2]

TEXTBOOKS:

1. Parag K. Lala, "Fault Tolerant & Fault Testable Hardware Design", 1984, PHI

2. Zainalabedin Navabi, “Digital System Test and Testable Design using HDL models and Architectures”, Springer International Edition.

REFERENCES:

1. Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman, “Digital Systems Testing and Testable Design”, Jaico Books
2. Bushnell & Vishwani D. Agarwal, “Essentials of Electronic Testing”, Springer.
3. Alfred L. Crouch, “Design for Test for Digital IC’s and Embedded Core Systems”, 2008, Pearson Education.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. TECH. I YEAR II SEMESTER DECE/DECS

DETECTION AND ESTIMATION THEORY (PC - 5)

UNIT – I

Random Processes: Discrete Linear Models, Markov Sequences and Processes, Point Processes, and Gaussian Processes.

UNIT – II

Detection Theory: Basic Detection Problem, Maximum A posteriori Decision Rule, Minimum Probability of Error Classifier, Bayes Decision Rule, Multiple-Class Problem (Bayes)- minimum probability error with and without equal a priori probabilities, Neyman-Pearson Classifier, General Calculation of Probability of Error, General Gaussian Problem, Composite Hypotheses.

UNIT – III

Linear Minimum Mean-Square Error Filtering: Linear Minimum Mean Squared Error Estimators, Nonlinear Minimum Mean Squared Error Estimators. Innovations, Digital Wiener Filters with Stored Data, Real-time Digital Wiener Filters, Kalman Filters.

UNIT – IV

Statistics: Measurements, Nonparametric Estimators of Probability Distribution and Density Functions, Point Estimators of Parameters, Measures of the Quality of Estimators, Introduction to Interval Estimates, Distribution of Estimators, Tests of Hypotheses, Simple Linear Regression, Multiple Linear Regression.

UNIT – V

Estimating the Parameters of Random Processes from Data: Tests for Stationarity and Ergodicity, Model-free Estimation, Model-based Estimation of Autocorrelation Functions, Power Special Density Functions.

TEXT BOOKS:

1. K. Sam Shanmugan & A.M. Breipohl, “Random Signals: Detection, Estimation and Data Analysis “, Wiley India Pvt. Ltd, 2011.
2. Lonnie C. Ludeman, “Random Processes: Filtering, Estimation and Detection”, Wiley India Pvt. Ltd., 2010.

REFERENCE BOOKS:

1. Steven. M. Kay, “Fundamentals of Statistical Signal Processing: Volume I Estimation Theory”, Prentice Hall, USA, 1998.
2. Steven. M. Kay, “Fundamentals of Statistical Signal Processing: Volume I Detection Theory”, Prentice Hall, USA, 1998.
3. Srinath, Rajasekaran, Viswanathan, “Introduction to Statistical Signal Processing with Applications”, 2003, PHI.
4. Louis L. Scharf, 1991, “Statistical Signal Processing: Detection, Estimation and Time Series Analysis “, Addison Wesley.
5. Harry L. Van Trees, “Detection, Estimation and Modulation Theory: Part – I “, 2001, John Wiley & Sons, USA.
6. Mischa Schwartz, Leonard Shaw, “Signal Processing: Discrete Spectral Analysis – Detection & Estimation ”, 1975, Mc Graw Hill.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. TECH. I YEAR II SEMESTER DECE/DECS

WIRELESS COMMUNICATIONS AND NETWORKS (PC - 6)

UNIT - I

The Cellular Concept-System Design Fundamentals: Introduction, Frequency Reuse, Channel Assignment Strategies, Handoff Strategies- Prioritizing Handoffs, Practical Handoff Considerations, Interference and system capacity – Co channel Interference and system capacity, Channel planning for Wireless Systems, Adjacent Channel interference , Power Control for Reducing interference, Trunking and Grade of Service, Improving Coverage & Capacity in Cellular Systems- Cell Splitting, Sectoring .

UNIT – II

Mobile Radio Propagation: Large-Scale Path Loss: Introduction to Radio Wave Propagation, Free Space Propagation Model, Relating Power to Electric Field, The Three Basic Propagation Mechanisms, Reflection-Reflection from Dielectrics, Brewster Angle, Reflection from prefect conductors, Ground Reflection (Two-Ray) Model, Diffraction-Fresnel Zone Geometry, Knife-edge Diffraction Model, Multiple knife-edge Diffraction, Scattering, Outdoor Propagation Models- Longley-Ryce Model, Okumura Model, Hata Model, PCS Extension to Hata Model, Walfisch and Bertoni Model, Wideband PCS Microcell Model, Indoor Propagation Models-Partition losses (Same Floor), Partition losses between Floors, Log-distance path loss model, Ericsson Multiple Breakpoint Model, Attenuation Factor Model, Signal penetration into buildings, Ray Tracing and Site Specific Modeling.

UNIT – III

Mobile Radio Propagation: Small –Scale Fading and Multipath: Small Scale Multipath propagation-Factors influencing small scale fading, Doppler shift, Impulse Response Model of a multipath channel- Relationship between Bandwidth and Received power, Small-Scale Multipath Measurements-Direct RF Pulse System, Spread Spectrum Sliding Correlator Channel Sounding, Frequency Domain Channels Sounding, Parameters of Mobile Multipath Channels-Time Dispersion Parameters, Coherence Bandwidth, Doppler Spread and Coherence Time, Types of Small-Scale Fading-Fading effects Due to Multipath Time Delay Spread, Flat fading, Frequency selective fading, Fading effects Due to Doppler Spread-Fast fading, slow fading, Statistical Models for multipath Fading Channels-Clarke's model for flat fading, spectral shape due to Doppler spread in Clarke's model, Simulation of Clarke and Gans Fading Model, Level crossing and fading statistics, Two-ray Rayleigh Fading Model.

UNIT - IV

Equalization and Diversity: Introduction, Fundamentals of Equalization, Training A Generic Adaptive Equalizer, Equalizers in a communication Receiver, Linear Equalizers, Non linear Equalization-Decision Feedback Equalization (DFE), Maximum Likelihood Sequence Estimation (MLSE) Equalizer, Algorithms for adaptive equalization-Zero Forcing Algorithm, Least Mean Square Algorithm, Recursive least squares algorithm. Diversity Techniques-Derivation of selection Diversity improvement, Derivation of Maximal Ratio Combining improvement, Practical Space Diversity Consideration-Selection Diversity, Feedback or Scanning Diversity, Maximal Ratio Combining, Equal Gain Combining, Polarization Diversity, Frequency Diversity, Time Diversity, RAKE Receiver.

UNIT - V

Wireless Networks: Introduction to wireless Networks, Advantages and disadvantages of Wireless Local Area Networks, WLAN Topologies, WLAN Standard IEEE 802.11,IEEE 802.11 Medium Access Control, Comparison of IEEE 802.11 a,b,g and n standards, IEEE 802.16 and its enhancements, Wireless PANs, Hiper Lan, WLL.

TEXT BOOKS:

1. Theodore, S. Rappaport, “Wireless Communications, Principles, Practice”, 2nd Edition, 2002, PHI.
2. Andrea Goldsmith, “Wireless Communications”, 2005 Cambridge University Press.
3. Kaveh Pah Laven and P. Krishna Murthy, “Principles of Wireless Networks”, 2002, PE
4. Gottapu Sasibhushana Rao, “Mobile Cellular Communication”, Pearson Education, 2012.

REFERENCE BOOKS:

1. Kamilo Feher, “Wireless Digital Communications”, 1999, PHI.
2. William Stallings, “Wireless Communication and Networking”, 2003, PHI.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. TECH. I YEAR II SEMESTER DECE/DECS

SYSTEM ON CHIP ARCHITECTURE (PE - 3)

UNIT – I

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT – II

Processors: Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT – III

Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT - IV

Interconnect Customization and Configuration: Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance-Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT – V

Application Studies / Case Studies: SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:

1. Michael J. Flynn and Wayne Luk, “Computer System Design System-on-Chip”, Wiley India Pvt. Ltd.
2. Steve Furber, “ARM System on Chip Architecture”, 2nd Edition., 2000, Addison Wesley Professional.

REFERENCE BOOKS:

1. Ricardo Reis, “Design of System on a Chip: Devices and Components”, 1st Edition., 2004, Springer
2. Jason Andrews, “Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology)”, Newnes, BK and CDROM.
3. Prakash Rashinkar, Peter Paterson and Leena Singh L, “System on Chip Verification – Methodologies and Techniques”, 2001, Kluwer Academic Publishers.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. TECH. I YEAR II SEMESTER DECE/DECS

SOFTWARE DEFINED RADIO (PE - 3)

UNIT - I

Introduction: The Need for Software Radios, What is Software Radio, Characteristics and benefits of software radio- Design Principles of Software Radio, RF Implementation issues- The Purpose of RF Front – End, Dynamic Range- The Principal Challenge of Receiver Design – RF Receiver Front- End Topologies- Enhanced Flexibility of the RF Chain with Software Radios- Importance of the Components to Overall Performance - Transmitter Architectures and Their Issues- Noise and Distortion in the RF Chain, ADC and DAC Distortion.

UNIT - II

Profile and Radio Resource Management: Communication Profiles- Introduction, Communication Profiles, Terminal Profile, Service Profile , Network Profile, User Profile, Communication Profile Architecture, Profile Data Structure, XML Structure, Distribution of Profile Data, Access to Profile Data, Management of Communication Profiles, Communication Classmarks, Dynamic Classmarks for Reconfigurable Terminals, Compression and Coding, Meta Profile Data

UNIT - III

Radio Resource Management in Heterogeneous Networks: Introduction, Definition of Radio Resource Management, Radio Resource Units over RRM Phases, RRM Challenges and Approaches, RRM Modelling and Investigation Approaches, Investigations of JRRM in Heterogeneous Networks, Measuring Gain in the Upper Bound Due to JRRM, Circuit-Switched System, Packet-Switched System, Functions and Principles of JRRM, General Architecture of JRRM, Detailed RRM Functions in Sub-Networks and Overall Systems

UNIT - IV

Reconfiguration of the Network Elements: Introduction, Reconfiguration of Base Stations and Mobile Terminals, Abstract Modelling of Reconfigurable Devices, the Role of Local Intelligence in Reconfiguration, Performance Issues, Classification and Rating of Reconfigurable Hardware, Processing Elements, Connection Elements, Global Interconnect Networks, Hierarchical Interconnect Networks, Installing a New Configuration, Applying Reconfiguration Strategies, Reconfiguration Based on Comparison, Resource Recycling, Flexible Workload Management at the Physical Layer, Optimized Reconfiguration, Optimization Parameters and Algorithms, Optimization Algorithms, Specific Reconfiguration Requirements, Reconfiguring Base Stations, Reconfiguring Mobile Terminals

UNIT - V

Object – Oriented Representation of Radios and Network Resources: Networks- Object Oriented Programming- Object Brokers- Mobile Application Environments- Joint Tactical Radio System.

Case Studies in Software Radio Design: Introduction and Historical Perspective, SPEAK easy- JTRS, Wireless Information Transfer System, SDR-3000 Digital Transceiver Subsystem, Spectrum Ware, CHARIOT.

TEXT BOOKS:

1. Markus Dillinger, Kambiz Madani, ”Software Defined Radio Architecture System and Functions”, WILEY 2003
2. Walter Tuttle Bee, “Software Defined Radio: Enabling Technologies”, 2002, Wiley Publications.

REFERENCE BOOKS:

1. Jeffrey H. Reed, “Software Radio: A Modern Approach to Radio Engineering”, 2002, PEA Publication.
2. Paul Burns, “Software Defined Radio for 3G”, 2002, Artech House.
3. Markus Dillinger, Kambiz Madani, Nancy Alonistioti, “Software Defined Radio: Architectures, Systems and Functions”, 2003, Wiley.
4. Joseph Mitola, “Software Radio Architecture: Object Oriented Approaches to wireless System Engineering “, III, 2000, John Wiley & Sons.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. TECH. I YEAR II SEMESTER DECE/DECS

CELLULAR AND MOBILE COMMUNICATIONS (PE - 3)

UNIT - I

Introduction to Cellular Mobile Radio Systems: Limitations of Conventional Mobile Telephone Systems, Basic Cellular Mobile System, First, Second, Third and Fourth Generation Cellular Wireless Systems, Uniqueness of Mobile Radio Environment- Fading -Time Dispersion Parameters, Coherence Bandwidth, Doppler Spread and Coherence Time.

Fundamentals of Cellular Radio System Design: Concept of Frequency Reuse, Co-Channel Interference, Co-Channel Interference Reduction Factor, Desired C/I From a Normal Case in a Omni Directional Antenna System, System Capacity, Trunking and Grade of Service, Improving Coverage and Capacity in Cellular Systems- Cell Splitting, Sectoring, Microcell Zone Concept.

UNIT - II

Co-Channel Interference: Measurement Of Real Time Co-Channel Interference, Design of Antenna System, Antenna Parameters and Their Effects, Diversity Techniques-Space Diversity, Polarization Diversity, Frequency Diversity, Time Diversity.

Non-Co-Channel Interference: Adjacent Channel Interference, Near End Far End Interference, Cross Talk, Effects on Coverage and Interference by Power Decrease, Antenna Height Decrease, Effects of Cell Site Components.

UNIT - III

Cell Coverage for Signal and Traffic: Signal Reflections in Flat And Hilly Terrain, Effect of Human Made Structures, Phase Difference Between Direct and Reflected Paths, Constant Standard Deviation, Straight Line Path Loss Slope, General Formula for Mobile Propagation Over Water and Flat Open Area, Near and Long Distance Propagation, Path Loss From a Point to Point Prediction Model in Different Conditions, Merits of Lee Model.

Cell Site and Mobile Antennas: Space Diversity Antennas, Umbrella Pattern Antennas, Minimum Separation of Cell Site Antennas, Mobile Antennas.

UNIT - IV

Frequency Management and Channel Assignment: Numbering And Grouping, Setup Access And Paging Channels, Channel Assignments to Cell Sites and Mobile Units, Channel Sharing and Borrowing, Sectorization, Overlaid Cells, Non Fixed Channel Assignment.

UNIT - V

Handoffs and Dropped Calls: Handoff Initiation, Types of Handoff, Delaying Handoff, Advantages of Handoff, Power Difference Handoff, Forced Handoff, Mobile Assisted and Soft Handoff, Intersystem Handoff, Introduction to Dropped Call Rates and their Evaluation.

TEXT BOOKS:

1. W.C.Y. Lee, “Mobile Cellular Telecommunications”, Mc Graw Hill, 2nd Edition. 1989.
2. Theodore. S. Rapport, “Wireless Communications”, Pearson Education, 2nd Edition., 2002.
3. Gottapu sashibhushana Rao, “Mobile Cellular Communication”, Pearson, 2012.

REFERENCE BOOKS:

1. Gordon L. Stuber, “Principles of Mobile Communications “, Springer International, 2nd Edition. 2001.
2. Simon Haykin, Michael Moher, “Modern Wireless Communications”, Pearson Education, 2005.

3. Asrar U. H .Sheikh, “Wireless Communications Theory and Techniques”, Springer, 2004.
4. Vijay Garg, “Wireless Communications and Networking”, Elsevier Publications, 2007.
5. Andrea Goldsmith, “Wireless Communications”, Cambridge University Press, 2005.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. TECH. I YEAR II SEMESTER DECE/DECS

NETWORK SECURITY AND CRYPTOGRAPHY (PE - 4)

UNIT - I

Introduction: Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internetwork security.

Classical Techniques: Conventional Encryption model, Steganography, Classical Encryption Techniques.

Modern Techniques: Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.

UNIT - II

Encryption Algorithms: Triple DES, International Data Encryption algorithm, Blowfish, RC5, CAST-128, RC2, Characteristics of Advanced Symmetric block ciphers.

Conventional Encryption: Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation.

UNIT - III

Public Key Cryptography: Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptography.

Number Theory: Prime and Relatively prime numbers, Modular arithmetic, Fermat's and Euler's theorems, Testing for primality, Euclid's Algorithm, the Chinese remainder theorem, Discrete logarithms.

UNIT - IV

Message Authentication and Hash Functions: Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs.

Hash and Mac Algorithms: MD File, Message digest Algorithm, Secure Hash Algorithm, RIPEMD-160, HMAC.

Digital signatures and Authentication protocols: Digital signatures, Authentication Protocols, Digital signature standards.

Authentication Applications: Kerberos, X.509 directory Authentication service.

Electronic Mail Security: Pretty Good Privacy, S/MIME.

UNIT – V

IP Security: Overview, Architecture, Authentication, Encapsulating Security Payload, Combining security Associations, Key Management. Web Security: Web Security requirements, Secure sockets layer and Transport layer security, Secure Electronic Transaction.

Intruders, Viruses and Worms: Intruders, Viruses and Related threats.

Fire Walls: Fire wall Design Principles, Trusted systems.

TEXT BOOKS:

1. William Stallings, "Cryptography and Network Security: Principles and Practice", Pearson Education.
2. William Stallings, "Network Security Essentials (Applications and Standards)", Pearson Education.

REFERENCE BOOKS:

1. Eric Maiwald, "Fundamentals of Network Security", Dreamtech press

2. Charlie Kaufman, Radia Perlman and Mike Speciner, “Network Security - Private Communication in a Public World”, Pearson/PHI.
3. Whitman, “Principles of Information Security”, Thomson.
4. Robert Bragg, Mark Rhodes, “Network Security: The complete reference”, TMH
5. Buchmann, “Introduction to Cryptography”, Springer.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. TECH. I YEAR II SEMESTER DECE/DECS

DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES (PE - 4)

UNIT - I

Introduction to Digital Signal Processing: Introduction, A digital Signal – Processing system, the sampling process, Discrete time sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), linear time-invariant systems, Digital filters, Decimation and interpolation.

Architectures for Programmable DSP devices: Basic Architectural features, DSP computational building blocks, Bus Architecture and Memory, Data addressing capabilities, Address generation UNIT, programmability and program execution, speed issues, features for external interfacing.

UNIT - II

Programmable Digital Signal Processors: Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX processors, memory space of TMS320C54XX processors, program control, TMS320C54XX instructions and programming, On-Chip peripherals, Interrupts of TMS320C54XX processors, Pipeline operation of TMS320C54XX processors.

UNIT - III

Architecture of ARM Processors: Introduction to the architecture, Programmer's model- operation modes and states, registers, special registers, floating point registers, Behaviour of the application program status register(APSR)-Integer status flags, Q status flag, GE bits, Memory system-Memory system features, memory map, stack memory, memory protection unit (MPU), Exceptions and Interrupts-what are exceptions?, nested vectored interrupt controller(NVIC), vector table, Fault handling, System control block (SCB), Debug, Reset and reset sequence.

Technical Details of ARM Processors: General information about Cortex-M3 and cortex M4 processors-Processor type, processor architecture, instruction set, block diagram, memory system, interrupt and exception support, Features of the cortex-M3 and Cortex-M4 Processors-Performance, code density, low power, memory system, memory protection unit, interrupt handling, OS support and system level features, Cortex-M4 specific features, Ease of use, Debug support, Scalability, Compatibility.

UNIT - IV

Instruction Set: Background to the instruction set in ARM Cortex-M Processors, Comparison of the instruction set in ARM Cortex-M Processors, understanding the assembly language syntax, Use of a suffix in instructions, Unified assembly Language (UAL), Instruction set, Cortex-M4-specific instructions, Barrel shifter, Accessing special instructions and special registers in Programming.

UNIT - V

Floating Point Operations: About Floating Point Data,Cortex-M4 Floating Point Unit (FPU)-overview, FP registers overview, CPACR register, Floating point register bank, FPSCR, FPU->FPCCR, FPU-> FPCAR, FPU->FPDSCR, FPU->MVFR0, FPU->MVFR1.

TEXTBOOKS:

1. Avtar Singh and S. Srinivasan, "Digital Signal Processing", CENGAGE Learning, 2004.
2. Joseph Yiu, "The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors", Elsevier Publications, 3rd Edition.

REFERENCES:

1. Andrew N. SLOSS, Dominic SYMES, Chris WRIGHT, "ARM System Developer's Guide Designing and Optimizing System Software", Elsevier Publications, 2004.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. TECH. I YEAR II SEMESTER DECE/DECS

EMI / EMC (PE - 4)

UNIT - I

Introduction, Natural and Nuclear Sources of EMI / EMC: Electromagnetic environment, History, Concepts, Practical experiences and concerns, frequency spectrum conservations, An overview of EMI / EMC, Natural and Nuclear sources of EMI.

UNIT - II

EMI from Apparatus, Circuits and Open Area Test Sites: Electromagnetic emissions, Noise from relays and switches, Non-linearities in circuits, passive intermodulation, Cross talk in transmission lines, Transients in power supply lines, Electromagnetic interference (EMI), Open area test sites and measurements.

UNIT - III

Radiated and Conducted Interference Measurements and ESD: Anechoic chamber, TEM cell, GH TEM Cell, Characterization of conduction currents / voltages, Conducted EM noise on power lines, Conducted EMI from equipment, Immunity to conducted EMI detectors and measurements, ESD, Electrical fast transients / bursts, Electrical surges.

UNIT - IV

Grounding, Shielding, Bonding and EMI filters: Principles and types of grounding, Shielding and bonding, Characterization of filters, Power lines filter design.

UNIT - V

Cables, Connectors, Components and EMC Standards: EMI suppression cables, EMC connectors, EMC gaskets, Isolation transformers, optoisolators, National / International EMC standards.

TEXT BOOKS:

1. Dr. V.P. Kodali, “Engineering Electromagnetic Compatibility, IEEE Publication, Printed in India by S. Chand & Co. Ltd., New Delhi, 2000.
2. IMPACT series, “Electromagnetic Interference and Compatibility”, IIT – Delhi, Modules 1 – 9.

REFERENCE BOOKS:

1. C.R. Pal, ”Introduction to Electromagnetic Compatibility “, Ny, John Wiley, 1992,

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WIRELESS COMMUNICATIONS AND NETWORKS LAB

Note:

- Minimum of 10 Experiments have to be conducted
- All the Experiments may be Conducted using Network Simulation software like NS-2/ NSG-2.1/ WireSHARK/ SDR etc..

Note:
For Experiments 1 to 7, Performance may be evaluated through simulation by using the parameters Throughput, Packet Delivery Ratio, Delay etc.

1. Evaluate the performance of various LAN Topologies
2. Evaluate the performance of Drop Tail and RED queue management schemes
3. Evaluate the performance of CBQ and FQ Scheduling Mechanisms
4. Evaluate the performance of TCP and UDP Protocols
5. Evaluate the performance of TCP, New Reno and Vegas
6. Evaluate the performance of AODV, DSR and DSDV routing protocols
7. Evaluate the performance of IEEE 802.11 and IEEE 802.15.4
8. Capturing and Analysis of TCP and IP Packets
9. Simulation and Analysis of ICMP and IGMP Packets
10. Analyze the Protocols SCTP , ARP, NetBIOS, IPX VINES
11. Analysis of HTTP ,DNS and DHCP Protocols
12. Analysis of OFDM Spectrum
13. Analysis CDMA Downlink