JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. TECH IN VLSI/ VLSI DESIGN/VLSI SYSTEM DESIGN.
EFFECTIVE FROM ACADEMIC YEAR 2017- 18 ADMITTED BATCH

COURSE STRUCTURE AND SYLLABUS

I Semester

Category	Course Title	Int. marks	Ext. marks	L	T	P	C
PC-1	Advanced Digital System Design	25	75	4	0	0	4
PC-2	Device Modeling	25	75	4	0	0	4
PC-3	CMOS Analog Integrated Circuit Design	25	75	4	0	0	4
PE-1	VLSI Technology Hardware Software Co-Design CPLD and FPGA Architectures and Applications	25	75	**3**	0	0	3
PE-2	Algorithms for VLSI Design Automation Embedded System Design Advanced Computer Architecture	25	75	**3**	0	0	3
OE-1	***Open Elective – I**	25	75	3	0	0	3
Laboratory I	Digital IC Design Lab	25	75	0	0	3	2
Seminar I	Seminar - I	100	0	0	0	3	2
Total		**275**	**525**	**21**	**0**	**6**	**25**

II Semester

Category	Course Title	Int. marks	Ext. marks	L	T	P	C
PC-4	Low Power VLSI Design	25	75	4	0	0	4
PC-5	Design for Testability	25	75	4	0	0	4
PC-6	CMOS Mixed Signal Circuit Design	25	75	4	0	0	4
PE-3	VLSI and DSP Architectures Full custom IC Design Verilog Hardware Description Language	25	75	**3**	0	0	3
PE4	RF IC Design System on Chip Architecture Scripting Languages	25	75	**3**	0	0	3
OE-2	***Open Elective – II**	25	75	3	0	0	3
Laboratory II	Analog IC Design Lab	25	75	0	0	3	2
Seminar II	Seminar - II	100	0	0	0	3	2
Total		**275**	**525**	**21**	**0**	**6**	**25**

III Semester

Course Title	Int. marks	Ext. marks	L	T	P	C
Technical Paper Writing	100	0	0	3	0	2
Comprehensive Viva-Voce	0	100	0	0	0	4
Project work Review II	100	0	0	0	22	8
Total	**200**	**100**	0	**3**	22	**14**

IV Semester

Course Title	Int. marks	Ext. marks	L	T	P	C
Project work Review III	100	0	0	0	24	8
Project Evaluation (Viva-Voce)	0	100	0	0	0	16
Total	**100**	**100**	**0**	**0**	**24**	**24**

***Open Elective subjects must be chosen from the list of open electives offered by OTHER departments.**

 # For Project review I, please refer 7.10 in R17 Academic Regulations.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. TECH. – I YEAR – II SEMESTER VLSI/ VLSI DESIGN/VLSI SYSTEM DESIGN

LOW POWER VLSI DESIGN (PC - 4)

UNIT – I

Fundamentals: Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT – II

Low-Power Design Approaches: Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches.
Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT – III

Low-Voltage Low-Power Adders: Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT – IV

Low-Voltage Low-Power Multipliers: Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT – V

Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:

1. Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits – Analysis and Design", TMH, 2011.
2. Kiat-Seng Yeo, Kaushik Roy, "Low-Voltage, Low-Power VLSI Subsystems", TMH Professional Engineering.

REFERENCE BOOKS:

1. Ming-BO Lin, "Introduction to VLSI Systems: A Logic, Circuit and System Perspective", CRC Press, 2011
2. Anantha Chandrakasan, "Low Power CMOS Design", IEEE Press/Wiley International, 1998.
3. Kaushik Roy, Sharat C. Prasad, "Low Power CMOS VLSI Circuit Design", John Wiley & Sons, 2000.
4. Gary K. Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic Press, 2002.
5. A. Bellamour, M. I. Elamasri, "Low Power CMOS VLSI Circuit Design", Kluwer Academic Press, 1995.
6. Siva G. Narendran, Anatha Chandrakasan, "Leakage in Nanometer CMOS Technologies" Springer, 2005.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. TECH. – I YEAR – II SEMESTER VLSI/ VLSI DESIGN/VLSI SYSTEM DESIGN

DESIGN FOR TESTABILITY (PC - 5)

UNIT - I

Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT - II

Logic and Fault Simulation: Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

UNIT - III

Testability Measures: SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT - IV

Built-In Self-Test: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT - V

Boundary Scan Standard: Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXT BOOK:

1. M.L. Bushnell, V. D. Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits” Kluwer Academic Publishers.

REFERENCE BOOKS:

1. M. Abramovici, M. A. Breuer and A.D Friedman, “Digital Systems and Testable Design”, Jaico Publishing House.
2. P.K. Lala, “Digital Circuits Testing and Testability”, Academic Press.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. TECH. – I YEAR – II SEMESTER VLSI/ VLSI DESIGN/VLSI SYSTEM DESIGN

CMOS MIXED SIGNAL CIRCUIT DESIGN (PC - 6)

UNIT - I

Switched Capacitor Circuits: Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT - II

Phased Lock Loop (PLL): Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

UNIT - III

Data Converter Fundamentals: DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT - IV

Nyquist Rate A/D Converters: Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT - V

Oversampling Converters: Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

TEXT BOOKS:

1. Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, TMH Edition, 2002
2. Philip E. Allen and Douglas R. Holberg, “CMOS Analog Circuit Design”, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. David A. Johns,Ken Martin, “Analog Integrated Circuit Design”, Wiley Student Edition, 2013

REFERENCE BOOKS:

1. Rudy Van De Plassche, “CMOS Integrated Analog-to- Digital and Digital-to-Analog converters”, Kluwer Academic Publishers, 2003
2. Richard Schreier, “Understanding Delta-Sigma Data converters”, Wiley Interscience, 2005.
3. R. Jacob Baker, “CMOS Mixed-Signal Circuit Design”, Wiley Interscience, 2009.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. TECH. – I YEAR – II SEMESTER VLSI/ VLSI DESIGN/VLSI SYSTEM DESIGN

VLSI AND DSP ARCHITECTURES (PE - 3)

UNIT - I

Essential feature of Instruction set architectures of CISC, RISC and DSP processors and their implications for implementation as VLSI Chips, Micro programming approaches for implementation of control part of the processor. Assessing understanding performance, Introduction, CPU performance and its factors, evaluating performance, real stuff: Two spec bench marks and performance of recent INTEL processors, fallacies and pitfalls

UNIT - II

Data Path and Control: Introduction, logic design conventions, building a data path, a simple implementation scheme, a multi cycle implementation, exceptions, micro programming: simplifying control design, an introduction to digital design using hardware description language, fallacies and pitfalls

UNIT - III

Enhancing performance with pipeline: An overview of pipelining, a pipe lined data path. Pipe lined control, data hazards and forwarding, data hazards and stalls, branch hazards using a hard ware description language to describe and model a pipe line, exceptions, advanced pipelining: extracting more performance, fallacies and pitfalls

UNIT - IV

Computational Accuracy in DSP implementations: Introduction, number formats for signals and coefficients in DSP system, dynamic range and precision, sources of errors in DSP implementations, A/D conversion errors, DSP computational errors, D /A conversion errors

UNIT - V

Architectures for programmable digital signal processing devices: Introduction, basic architectural features, DSP Computational building blocks, bus architecture and memory, data addressing capabilities, address generation unit, programmability and program execution, speed issues, features for external interfacing.

TEXT BOOKS:

1. D. A, Patterson and J.L Hennessy, “Computer Organization and Design: Hardware/ Software Interface”, 4th Ed., Elsevier, 2011
2. A. S Tannenbaum, “Structural Computer organization”, 4th Ed., Prentice-Hall, 1999

REFERENCE BOOKS:

1. W. Wolf, “Modern VLSI Design: System on Silicon”, 2nd Ed., Person Education,1998
2. Keshab Parhi, “VLSI Digital Signal Processing system design and implementations”, Wiley 1999
3. Avatar sign, Srinivasan S, “Digital Signal Processing implementations using DSP microprocessors with examples”, Thomson 4th reprint, 2004.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. TECH. – I YEAR – II SEMESTER VLSI/ VLSI DESIGN/VLSI SYSTEM DESIGN

FULL CUSTOM IC DESIGN (PE - 3)

UNIT - I
Introduction: Schematic fundamentals, Layout design, Introduction to CMOS VLSI manufacturing processes, Layers and connectivity, Process design rules Significance of full custom IC design, layout design flows.

UNIT - II
Advanced techniques for specialized building blocks Standard cell libraries, Pad cells and Laser fuse cells, Advanced techniques for building blocks, Power grid Clock signals

UNIT - III
Interconnect routing. Interconnect layout design, Special electrical requirements, Layout design techniques to address electrical characteristics.

UNIT - IV
Layout considerations due to process constraints Large metal via implementations, Step coverage rules, Special design rules, Latch-up and Guard rings, Constructing the pad ring, Minimizing Stress effects.

UNIT - V
Proper layout CAD tools for layout, Planning tools, Layout generation tools, Support tools.

TEXT BOOKS:
1. Dan Clein, “CMOS IC Layout Concepts Methodologies and Tools”, Newnes, 2000.
2. Ray Alan Hastings, “The Art of Analog Layout”, 2nd Edition, Prentice Hall, 2006

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. TECH. – I YEAR – II SEMESTER VLSI/ VLSI DESIGN/VLSI SYSTEM DESIGN

VERILOG HARDWARE DESCRIPTION LANGUAGE (PE - 3)

UNIT - I

Introduction to Verilog HDL: Verilog as HDL, Levels of Design Description, Concurrency, Simulation and Synthesis, Function Verification, Systems tasks, programming language interface, Module, Simulation and Synthesis tools.

Language Constructs and Conventions: Introduction, Keywords, Identifiers, White Space Characters, Comments, Numbers, Strings, Logic values, Strengths, Data types, Scalars and Vectors, Parameters, Operators.

UNIT - II

Gate Level Modeling: Introduction, AND Gate Primitive, Module, Structure, Other Gate Primitives, Illustrative Examples, Tristate Gates, Array of Instances of Primitives, Design of Flip – Flops with Gate Primitives, Delays, Strengths and Construction Resolution, Net Types, Design of Basic Circuit.

Modeling at Dataflow Level: Introduction, Continuous Assignment Structure, Delays and Continuous Assignments Assignment to Vectors, Operators.

UNIT - III

Behavioral Modeling: Introduction, Operations and Assignments, Functional Bifurcation, Initial Construct, Always Construct, Assignments with Delays, Wait Construct, Multiple Always Block, Designs at Behavioral Level, Blocking and Non-Blocking Assignments, The Case Statement, Simulation Flow if an if-Else Constructs, Assign- De-Assign Construct, Repeat Construct, for Loop, the Disable Construct, While Loop, For Ever Loop, Parallel Blocks, Force-Release, Construct, Event.

UNIT - IV

Switch Level Modeling: Basic Transistor Switches, CMOS Switches, Bi Directional Gates, Time Delays with Switch Primitives, Instantiation with Strengths and Delays, Strength Contention with Trireg Nets.

System Tasks, Functions and Compiler Directives: Parameters, Path Delays, Module Parameters, System Tasks and Functions, File Based Tasks and Functions, Computer Directives, Hierarchical Access, User Defined Primitives.

UNIT - V

Sequential Circuit Description: Sequential Models – Feedback Model, Capacitive Model, Implicit Model, Basic Memory Components, Functional Register, Static Machine Coding, Sequential Synthesis.

Component Test and Verification: Test Bench-Combinational Circuit Testing, Sequential Circuit Testing, Test Bench Techniques, Design Verification, Assertion Verification

TEXT BOOKS:

1. T R Padmanabhan, B.Bala Tripura Sundari, Design Through Verilog HDL,2009, Wiley.
2. Zainalabdien Navabi, Verilog Digital System Design, TMH,2nd Edition,

REFERENCES:

1. Stephen Brown, Zvonkoc Vranesic, “Fundamentals of Digital Logic with Verilog Design”, 2nd Edition, 2010, TMH
2. Sunggu Lee, “ Digital Logic Design using Verilog, State Machine & Synthesis for FPGA,” Cengage Learning 2009
3. Verilog HDL – Samir Palnitkar, 2nd Edition, Pearson Education, 2009.
4. Advanced Digital Design with verilog HDL – Michel D.Ciletti, PHI,2009

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. TECH. – I YEAR – II SEMESTER VLSI/ VLSI DESIGN/VLSI SYSTEM DESIGN

RF IC DESIGN (PE - 4)

UNIT – I: Introduction to RF and Wireless Technology: Complexity comparison, Design bottle necks, Applications, Analog and digital systems, Choice of Technology.

UNIT – II: Basic concepts in RF Design: Nonlinearity and time variance, ISI, Random process and noise, sensitivity and dynamic range, passive impedance transformation.

UNIT – III: Multiple Access: Techniques and wireless standards, mobile RF communication, FDMA, TDMA, CDMA, Wireless standards.
Transceiver Architectures: General considerations, receiver architecture, Transmitter Architecture, transceiver performance tests, case studies.

UNIT – IV: Amplifiers, Mixers and Oscillators: LNAs, down conversion mixers, Cascaded Stages, oscillators, Frequency synthesizers.

UNIT – V: Power Amplifiers: General considerations, linear and nonlinear Pas, classification, High Frequency power amplifier, large signal impedance matching, linearization techniques.

TEXT BOOKS:

1. Behzad Razavi, RF Microelectronics Prentice Hall of India, 2001.
2. Thomas H. Lee, The Design of CMOS Radio Integrated Circuits, Cambridge University Press.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. TECH. – I YEAR – II SEMESTER VLSI/ VLSI DESIGN/VLSI SYSTEM DESIGN

SYSTEM ON CHIP ARCHITECTURE (PE - 4)

UNIT – I

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory, and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT – II

Processors: Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT – III

Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT - IV

Interconnect Customization and Configuration: Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance-Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT – V

Application Studies / Case Studies: SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:

1. Michael J. Flynn and Wayne Luk, “Computer System Design System-on-Chip”, Wiely India Pvt. Ltd.
2. Steve Furber, “ARM System on Chip Architecture”, 2nd Ed., 2000, Addison Wesley Professional.

REFERENCE BOOKS:

1. Ricardo Reis, “Design of System on a Chip: Devices and Components”, 1st Ed., 2004, Springer
2. Jason Andrews, “Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology)”, Newnes, BK and CDROM.
3. Prakash Rashinkar, Peter Paterson and Leena Singh L, “System on Chip Verification – Methodologies and Techniques”, 2001, Kluwer Academic Publishers.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. TECH. – I YEAR – II SEMESTER VLSI/ VLSI DESIGN/VLSI SYSTEM DESIGN

SCRIPTING LANGUAGES (PE - 4)

UNIT - I

Introduction to Scripts and Scripting: Characteristics and uses of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

UNIT - II

Advanced PERL: Finer points of Looping, Subroutines, Using Pack and Unpack, Working with files, Navigating the file system, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects, Objects and modules in action, Tied variables, Interfacing to the operating systems, Security issues.

UNIT - III

TCL: The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

UNIT - IV

Advanced TCL: The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internet programming, Security issues, running untrusted code, The C interface.

UNIT - V

TK and JavaScript: Visual tool kits, Fundamental concepts of TK, TK by example, Events and bindings, Geometry managers, PERL-TK.
JavaScript – Object models, Design Philosophy, Versions of JavaScript, The Java Script core language, Basic concepts of Python.
Object Oriented Programming Concepts (Qualitative Concepts Only): Objects, Classes, Encapsulation, Data Hierarchy.

TEXT BOOKS:

1. David Barron, “The World of Scripting Languages”, Wiley Student Edition, 2010.
2. Brent Welch, Ken Jones and Jeff Hobbs, “Practical Programming in Tcl and Tk”, Fourth edition.
3. Herbert Schildt, “Java the Complete Reference”, 7th Edition, TMH.

REFERENCE BOOKS:

1. Clif Flynt, “Tcl/Tk: A Developer's Guide”, 2003, Morgan Kaufmann Series.
2. John Ousterhout, “Tcl and the Tk Toolkit”, 2nd Edition, 2009, Kindel Edition.
3. Wojciech Kocjan and Piotr Beltowski, “Tcl 8.5 Network Programming book”, Packt Publishing.
4. Bert Wheeler, “Tcl/Tk 8.5 Programming Cookbook”, 2011, Packt Publishing Limited.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. TECH. – I YEAR – II SEMESTER VLSI/ VLSI DESIGN/VLSI SYSTEM DESIGN

ANALOG IC DESIGN LAB

List of Experiments:

1. Lambda calculation for PMOS and NMOS
2. Transconductance plot
3. Ideal Current source PMOS & NMOS
4. NMOS saturated load
5. Single transistor amplifier
6. Cascade amplifier
7. Wilson current mirror
8. Cascade current mirror
9. Cascode current mirror
10. Regulated Cascade current mirror