Code No: R1621042 **R16** SET - 1

II B. Tech I Semester Supplementary Examinations, May - 2018
SWITCHING THEORY AND LOGIC DESIGN
(Com to ECE, EIE and ECC)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A

1. a) Subtract 27810 from 49510 using the excess-3 subtractor. (3M)
   b) Obtain complement and dual for the given expression (AB+BC+AC) (EF) (3M)
   c) Design full adder using two half adders (2M)
   d) Explain basic structure of PLA (2M)
   e) Convert JK Flip Flop to T Flip Flop (2M)
   f) Brief about Finite State Machine (2M)

PART -B

2. a) The message below has been coded in the 7 bit Hamming code and transmitted through noisy channel. Decode the message assuming that at most a single error has occurred in each code word 1001001, 0111001, 1110110, and 0011011. (7M)
   b) Generate Hamming code for a 4-bit Excess-3 message to detect and correct single bit errors. (7M)

3. a) Implement the following function using only NOR gates F=a. (b+ c.d) + (b. c). (7M)
   b) Implement the following function using only NAND gates G=(a + b).(c. d + e) (7M)

4. a) Design a full-adder with two half-adders and basic gates. (7M)
   b) Convert Excess-3 code to BCD using Full adder circuits. (7M)

5. a) Implement f (A,B,C,D) = ∑(0,1,3,5,6,8,9,11,12,13) using PAL and explain its procedure . (7M)
   b) Write the merits and demerits of PROM. (7M)

6. a) Draw the circuit diagram of J-K flip flop with NAND gates with positive edge triggering and explain its operation with the help of truth table. How race around condition is eliminated. (7M)
   b) Realize D-latch using R-S latch. How it is different from D-flip flop. Draw the circuit using NAND gates and explain. (7M)
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7. a) Convert the following Mealy machine into a corresponding Moore machine: (7M)

PS	NS,Z	
	X=0	X=1
A	C,0	B,0
B	A,1	D,0
C	B,1	A,1
D	D,1	C,0

b) Design the circuit for the above table using RS flipflops. (7M)