Code No: R21054 **R10** SET - 1

II B. Tech I Semester Regular Examinations, March – 2014
DIGITAL LOGIC DESIGN
(Com. to CSE, IT)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Covert the following decimal numbers to binary, octal and hexadecimal numbers
   i) 196 ii) 207.05
   b) Perform the following subtraction using 2's complement
   i) 19 – 37 ii) 79 – 19
   c) Find out the BCD, excess -3 and Grey code for the decimal numbers 0 to 9. (5M+5M+5M)

2. a) Find the complements of the following expressions
   i) $(x\bar{y}+x\bar{z})(yz+y\bar{z})(xyz)$ ii) $x+\bar{y}\,z\,(x+y+\bar{z})$
   b) State and explain DeMorgan's theorems. Draw the logic equivalent circuits representing the theorems using basic gates.
   c) Determine the canonical sum-of-products representation of the following functions
   i) $f(a,b,c)=a+(\bar{c}+b)(c+\bar{b})$ ii) $f(a,b,c)=c+\left(\overline{\bar{c}\bar{b}+\bar{c}a}\right)$ (5M+5M+5M)

3. a) Simplify the Boolean expression using K-map
   $F(A,B,C,D)=\bar{A}+C+AB+A\bar{B}D+AB\bar{D}$
   b) Reduce the expression $f(x,y,z,w)=\pi(0,2,7,8,9,10,11,15)+d(3,4)$ using K-map (7M+8M)

4. a) Realize a full-adder using i) only NAND gates and ii) only NOR gates
   b) With the help of a logic diagram explain a parallel adder/subtractor using 1's complement systems. (7M+8M)

5. a) Design an 8:1 multiplexer using NAND gates only
   b) Design the following code converters i) Binary to Excess-3 ii) Grey to Binary (7M+8M)

6. a) Explain the need and advantages of using programmable logic devices in digital system design
   b) Design a BCD to 7 segment decodes for common cathode display using a suitable PLA. (7M+8M)

7. a) Draw the schematic circuit of a clocked J-K Flip-Flop with active low preset and active low clear using NAND gates and explain its operation with the help of a truth table.
   b) Distinguish between combinational and sequential logic circuits. (8M+7M)

8. a) Design a 4 bit binary synchronous counter with D Flip-Flops.
   b) Design a 5 bit self-correcting ring counter (7M+8M)
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Code No: R21054 **R10** SET - 2

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1. a) Convert the following hexadecimal numbers to decimal binary, octal numbers
   i) $(357)_{16}$ ii) $(3AF.21)_{16}$
   b) Perform the following subtraction using 1's complements
   i) 28 – 78 ii) 96 – 22
   c) Generate a 4 bit Gray code directly using the mirror image property. (5M+5M+5M)

2. a) Simplify the following logic expressions using Boolean theorems.
   i) $(x+y+z)(x+\bar{y}+\bar{z}).(x+y+\bar{z}).(x+\bar{y}+z)$
   ii) $xyz+\bar{x}yz+x\bar{y}z+xy\bar{z}+x\bar{y}\ \bar{z}+\bar{x}y\bar{z}+\bar{x}\ \bar{y}\ \bar{z}.$
   b) Explain the terms
   i) Prime implicant ii) minterm and iii) maxterm
   c) Realize 2-input Ex-OR and Ex-NOR gates using (5M+5M+5M)
   i) NAND gates and ii) NOR gates only

3. a) Reduce the expression $f(x,y,z,w)=\sum(1,4,6,12,13,14)+d(2,5)$ using K-map.
   b) Simplify the Boolean expression using k-map $f(x,y,z,w)=(x+y)(x+\bar{y}+z)(x+\bar{z})$.
   (7M+8M)

4. a) Realize a full – sub tractor using i) only NAND gate and ii) only NOR gates.
   b) With the help of a basic diagram explain a parallel adder / sub tractor using 2's complement system. (7M+8M)

5. a) Design the following combinational logic circuits using a multiplexes
   i) Half – adder ii) Full – adder
   b) How does a priority encodes differ from an ordinary encodes explain with truth table and logic diagrams? (8M+7M)

6. a) Describe the differences between PLA and PAL.
   b) Derive PLA and PAL programming tables for a combinational circuit that squarer a 3 bit number. (7M+8M)

7. a) Explain the basic Flip-Flop circuit for R-S using i) NAND gates ii) NOR gates
   b) Explain how a T Flip-Flop is conversed in D Flip-Flop and J-K Flip-Flop. (8M+7M)

8. a) Design and implement a Mod – 6 synchronous counter using J-K Flip –Flop.
   b) Draw the logic diagram of a 4 bit shift resister. Explain how shift-left and shift-right operations are performed. (7M+8M)
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Code No: R21054 **R10** SET - 3

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Time: 3 hours Max. Marks: 75

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1. a) Convert the following octal numbers to binary, decimal and hexadecimal numbers.
   i) $(175)_8$ ii) $(326.04)_8$
   b) Perform the following subtraction using 2'r complement.
   i) 38 – 21 ii) 19 – 92
   c) Explain even and odd parity codes. (5M+5M+5M)

2. a) Expend $A(\overline{A}+B)\,(\overline{A}+B-\overline{C})$ to max terms and min terms
   b) Simplify the following expressions.
   i) $A\overline{B}+ABC+A(B+A\overline{B})$ ii) $A+\overline{A}B+\overline{A}\,\overline{B}C+\overline{A}\,\overline{B}\,\overline{C}D.$
   c) Implement the Boolean function F (A, B, C, D) $=\overline{A}\,\overline{B}+\overline{C}\,\overline{D}+\overline{B}\,\overline{C}$ using the following two level gates (5M+5M+5M)
   i) NAND – AND ii) NOR – OR.

3. a) Reduce the expression $f(x, y, z, w)=\sum(0, 1, 4, 5, 6, 7, 9, 11, 14)+d(10, 15)$ using K - map.
   b) Reduce the Boolean expression using K – map (7M+8M)
   $f(x, y, z, w)=x\,\overline{y}\,z+y+y\,\overline{w}+x, y, \overline{w}+\overline{x}\,z.$

4. a) Realize a half – subtractor using i) only NOR gates and ii) only NAND gates.
   b) Explain a look – ahead – carry adder in detail. (8M+7M)

5. a) Implement the following expression using a single 8:1 multiplexer
   $F(x, y, z, w)=\sum(0, 1, 2, 5, 7, 8, 9, 14, 15).$
   b) Draw the basic diagram of a 2 to 4 decodes with an ENABLE input using (7M+8M)
   i) NAND gates ii) NOR gates.

6. a) Give the comparison between PROM, PLA and PAL.
   b) Design a combinational circuit that accepts a 3 bit number and generates an output binary number equal to the require of the input number using a ROM. (7M+8M)

7. a) Draw a neat circuit diagram of locked J – K flip – flop using NAND gates and give its truth table.
   b) Give the Excitation table for T flip- flop, SR flip-flop and J-K flip- flop. (7M+8M)

8. a) Design a 4 bit binary up / down ripple counter.
   b) Draw a neat circuit diagram of a 4 bit Johnson converter and draw the relevant output wave forms. (7M+8M)
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1. a) Convert the following binary numbers to decimal, octal number and Grey code.
   i) 110101101 ii) 10010001.
   b) Perform the flowing subtraction using 1's complement.
   i) 33 – 08 ii) 28 – 71
   c) What is BCD code? What are the rules for BCD additions? (5M+5M+5M)

2. a) Show that both NAND gate and NOR gate are universal gates.
   b) Explained $x + y\bar{z} + xy\bar{w} + xyzw$ to min.terms and max.terms.
   c) Simplify the following logic expressions using Boolean theorems. (5M+5M+5M)
   i) $AB + \overline{AC} + A\bar{B}C\ CAB + C)$ ii) $\bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}\bar{C} + AB\bar{C}$.

3. a) Reduce the expression $f(x, y, z, w) = \sum(3, 5, 6, 7, 11, 13, 14, 15) + d\ (9, 10, 12)$.
   b) Reduce the following expression using K-map. (8M+7M)
   $f(x,\ y,\ z,\ w) = x(y + \bar{z})\ (x + \bar{y})\ (y + z + \bar{w})$.

4. a) Realize a half –adder using i) only NAND gates ii) only NOR gates.
   b) Give the implementation of a 4 bit ripple adder using full – adders. (8M+7M)

5. a) Design a 16:1 MUX using i) 3:1 MUX and or gate ii) 8:1 and 2:1 MUX.
   b) Implement the following function using 3 to 8 line decorous (7M+8M)
   i) $f(x,\ y,\ z) = \sum(0, 1, 5, 6)$ ii) $f(x,\ y,\ z) = \sum(0, 2, 3, 4, 6)$

6. a) Explain how to use PAL having only five product terms to realize a function having six product terms.
   b) Design a 3 bit Binary - to – Grey code converse using a suitable PLA. (8M+7M)

7. a) What is race – around condition? How does it set eliminated is a Master- slave J-K flip-flop.
   b) Convert a D flip – flop into SR flip-flop and T flip – flop. (8M+7M)

8. a) Design and implement a MOD-7 synchronous counter using T flip-flops.
   b) Design a 4 bit universal shift resister and draw the circuit with the given mode of operation table. (7M+8M)

S_1	S_0	Operation
0	0	Shift left
0	1	Shift right
1	0	Parallel
1	1	Inhibit clock
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