Code No: R21054 **R10** SET - 1

II B. Tech I Semester Supplementary Examinations, September - 2014
DIGITAL LOGIC DESIGN
(Com. to CSE, IT)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. Convert the following to decimal and then to binary
   a) 1001101_{16} b) $ABCD_{16}$ c) 7654_8 d) 4725_8

2. a) Find the complement of $f = ab + \bar{c}d + \bar{e}$
   b) Simplify the given function f = (x + y) (x + y^1)
   c) What are universal gates? Realize basic gates using universal gates.

3. Obtain minimal SOP expression for the given Boolean function using K-map.
   F(A,B,C,D) = ∑(0,1,4,6,8,9,10,12) + d(3,7,11,13,14,15) and draw the circuit using 2 input NAND gates.

4. a) Design a full adder circuit using AND, OR, and NOT gates
   b) Design BCD to Gray code converter using full adder circuits.

5. a) F (W,X,Y,Z) = ∑ m(0,1,4,7,9,12,14) realize using 1:16 de MUX.
   b) What do you mean by hazards in combinational circuits? How do you design hazard free circuit? Explain with suitable example.

6. A combinational circuit is defined by the function
   F_1 (A,B,C) = ∑ m (3,5,6,7) F_2 (A,B,C) = ∑ m (0,2,4,7)
   Implement the circuit with a PLA having three inputs, four product terms and two outputs.

7. a) Distinguish between combinational and sequential logic circuits.
   b) Convert a D flip flop into
      i) SR flip flop ii) JK flip flop iii) T- flip flop

8. a) Design a Mod -6 synchronous counter using J-K flip flops.
   b) Design a 3 stage shift register, which is a universal register.
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Code No: R21054 **R10** SET - 2

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Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
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1. a) Convert to octal i) 10101_2 ii) 110110111_2
   b) Convert the decimal number 460.8 to base 6, 8 and 12
   c) Convert to decimal i) $4CA_{16}$ ii) $3BE_{16}$

2. a) Explain the fundamental postulates of Boolean Algebra
   b) Express the Boolean function F= $(AB+A^1 B^1)(CD^1+C^1 D)$ as a sum of minterms.

3. Simplify the following using K-map method and implement the following function with NAND gates.
   F (A,B,C,D,E) = ∑ (0,2,4,6,9,13,21,23,25,29,31)

4. a) Generate 2's complement for the given 4 bit binary number using full-adders
   b) Design Octal to Binary encoder using OR gates.

5. a) Implement the following logic function using a 8 X 1 multiplexer
   F (A,B,C,D) = ∑ m(1,2,5,11,12,13,14,15)
   b) With the help of logic diagram and a truth table, explain a 3 line to 8 line decoder.

6. a) Write short notes on: i) PLA ii) PAL iii) error detection and correction.
   b) Compare PLA, PAL and PLD.

7. a) Define the following terms with respect to flip flops
   i) Hold time ii) Set-Up time iii) Propagation delay time.
   b) What is meant by race around condition? Explain how it is avoided in master and slave JK flip flop.

8. a) Show how BCD ripple counter can be implemented using flip flops
   b) When do you prefer synchronous counters?
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Code No: R21054 **R10** SET - 3

II B. Tech I Semester Supplementary Examinations, September - 2014
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Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Subtract the following numbers using 10's and 9's complement
   i) 5250-425 ii) 826-359
   b) Express the following numbers in decimal and octal number systems.
   i) $(110101.1011)_2$ ii) $CDEA_{16}$

2. a) Find the sum of min terms and product of max terms for the given function $F(x, y, z, w) = y' w + x' w + y w$. And realize the circuit using universal gates
   b) Find the dual of f = AC+BD+A

3. Obtain the simplified expressions in SOP for the following Boolean function using k-map
   i) F (A, B, C, D) = ∑ (7, 13, 14, 15)
   ii) F(W,X,Y,Z) =∑ (1,3,5,6,11,13)

4. a) Implement a full subtractor with two half subtractors and an OR gate.
   b) Design an excess-3 to BCD code convert using a 4-bit full adder circuit.

5. a) Implement the following with a multiplexer F(A,B,C,D) = ∑ (0,1,3,4,8,9,15)
   b) Design a combinational circuit for an octal to binary encoder.

6. Implement the following Boolean function with a PLA having three inputs, four product terms and two outputs.
   F_1 (X,Y,Z) = ∑ (0,1,2,4) , F_2 (X,Y,Z) = ∑ (0,5,6,7)

7. a) Realize D flip flop using JK flip flop.
   b) Give the transition Table for the following flip flops.
   i) RS flip flop ii) J-K flip flop iii) T- flip flop iv) D flip flop

8. a) Draw the circuit diagram of 4bit ring counter using T flip flop and draw the corresponding timing diagrams.
   b) Explain synchronous and ripple counters and compare them.
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Code No: R21054 **R10** SET - 4

II B. Tech I Semester Supplementary Examinations, September - 2014
DIGITAL LOGIC DESIGN
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Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Convert the following decimal numbers to binary i) 45.36 ii) 76.08
   b) Perform the following operations using 2's arithmetic
   i) 10110.1101-1010.111 ii) 111010.1101-11010.0010

2. a) List the truth tables of the function
   i) F=xy+xy^1+y^{1}z ii) F= x^{1}z+yz iii) F= x^{1}z+xy
   b) Given AB^1+A^{1}B= C, show that AC^1+A^{1}C=B

3. Simplify the following using k-map method and implement the following function with NAND gates
   i) F(A,B,C,D) = Π(0,1,3,5,6,7,10,14,15)
   ii) $Y = A' B' C' D' + A' B' C D' + A B' C' D' + A' C D + A B' C D'$

4. a) With the help of logic diagram explain a parallel adder / subtractor using 2's complement system.
   b) Design a full adder using half adders and carry look ahead adders.

5. a) A combinational circuit is defined by the following three functions
   F_1= (x y)^1 + xyz^1, F_2 = x^1 + y , F_3 = x y+(x y)^1 design the circuit with a decoder and external gates.
   b) List the applications of Multiplexer and Demultiplexer.

6. a) Write a brief notes on Architecture of PLD's.
   b) Design a BCD to excess 3 code converter using PAL.

7. a) Draw and explain the working of Master slave JK flip flop.
   b) Design a sequence detector that detects 110010. Implement the sequence detector by using D type flip-flops.

8. a) Design Mod -12 counter using S-R flip flop.
   b) Compare the merits and demerits of ripple and synchronous counters.
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