Code No: R32052 **R10** **Set No: 1**

III B.Tech. II Semester Supplementary Examinations, January -2014

COMPUTER ARCHITECTURE

(Computer Science and Engineering)

Time: 3 Hours **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. (a) Introduce briefly current state of computing.
   (b) Write about
   i. Elements of Modern Computers.
   ii. Evolution of Computer Architecture.

2. Explain in detail Pipelined cache access to increase bandwidth.

3. Write about
   (a) Coherence.
   (b) Locality

4. Explain following concepts in pipeline processors
   (a) Clocking and Timing control.
   (b) Speedup
   (c) Efficiency
   (d) Throughput.

5. Briefly characterize the multi cache coherence problem and describe various methods that have been suggested to cope with the problem. Comment on advantages and disadvantages of each method to preserve the coherence among multiple shared caches used in a multiprocessor system.

6. write about
   (a) Message Passing Mechanisms.
   (b) Message Routing Schemes.

7. Discuss in detail control processors and processing nodes.

8. Describe and classify the various types of parallel algorithms. And also explain the advantages of parallelism.

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Code No: R32052 **R10** **Set No: 2**

III B.Tech. II Semester Supplementary Examinations, January -2014

COMPUTER ARCHITECTURE

(Computer Science and Engineering)

Time: 3 Hours **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. (a) Write differences between Multiprocessors and Multicomputers.
   (b) Explain in detail Taxonomy of MIMD computers.

2. Explain about
   (a) Virtual Memory
   (b) Virtual Machines

3. Write about instruction -set architectures.

4. Explain the principles of linear pipelining. Explain differences between Linear and Nonlinear pipeline processors.

5. Give the comparison of three multiprocessor hardware organizations:
   (a) Multiprocessor with time shared bus.
   (b) Multiprocessor with cross-bar switch
   (c) Multiprocessor with multiport memory.

6. What is cache coherence and why is it important in shared-memory multiprocessor systems? How can the problem be resolved with a snoopy cache controller?

7. Explain in detail about VSIMD and MIMD Computer Organizations.

8. What do you mean by parallel processing and what are the different levels at which parallel processing can be implanted?

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Code No: R32052 **R10** **Set No: 3**

III B.Tech. II Semester Supplementary Examinations, January -2014

COMPUTER ARCHITECTURE

(Computer Science and Engineering)

Time: 3 Hours **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. Write about in detail
   (a) Vector Supercomputers
   (b) SIMD Supercomputers

2. Explain the concept of protection via Virtual memory and Virtual Machines.

3. Explain in detail typical CISC and RISC Architecture.

4. Explain the following:
   (a) Nonlinear pipelining and reservation tables.
   (b) Interleaved memory organization

5. Distinguish among the following operating system configurations for multiprocessor computers. In each system configuration, name two example multiprocessor computers that have implemented an operating system similar to the configuration being discussed. Comment on the advantages and disadvantages, design problems, and shortcomings in each operating system configuration:
   (a) Master-slave Operating System
   (b) Separate supervisor system per processor
   (c) Floating-point supervisor system.

6. Write about
   (a) Snoopy bus protocols.
   (b) Directory based protocols.

7. Explain in detail CM-2 Architecture.

8. What is instruction level parallelism? Explain data dependencies and hazards.

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Code No: R32052 **R10** **Set No: 4**

III B.Tech. II Semester Supplementary Examinations, January -2014

COMPUTER ARCHITECTURE

(Computer Science and Engineering)

Time: 3 Hours **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. Write differences between Shared Memory Multiprocessors and Distributed Memory Multicomputers

2. (a) Introduce memory hierarchy design.
   (b) Explain about Optimization of cache performance.

3. Write about Hierarchical Memory Technology.

4. Write about Asynchronous and Synchronous models.

5. Explain the following:
   a. A single-bus multiprocessor organization
   b. multiprocessor with unidirectional buses
   c. multi-bus multiprocessor organization
   d. different algorithms for bus arbitration.

6. Introduce Routing Algorithms. Explain about Multicast Routing Algorithms.

7. Write in detail interprocessor Communications.

8. Describe the criteria that are used to evaluate parallel algorithms.

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