Code No: R32045 **R10** **Set No: 1**

III B.Tech. II Semester Supplementary Examinations, January -2014

**VLSI DESIGN**

(Common to Electronics and Communication Engineering & Electronics and Computer Engineering & Electronics and Instrumentation Engineering)

**Time: 3 Hours** **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. (a) Explain how the transistors are integrated on a single chip according to Moore's Law?
   ( b ) Explain the fabrication steps for NMOS Technology with neat diagrams. [5+10]

2. Define the following terms:
   ( i ) Threshold voltage (ii) Body effect (iii) Figure of merit [5+5+5]

3. ( a ) Explain the Transistor design rules for nMOS, pMOS and CMOS technologies.
   ( b ) Design and Draw the Layout of CMOS Inverter gate and explain its working. [8+7]

4. ( a ) Consider the metal wire segment of length 20λ and width of 3λ. Calculate the capacitance to substrate if the relative capacitance value is $0.075 \square C_g$.
   ( b ) Draw the model for derivation of delay unit and explain.
   ( c ) Derive the equation for fall time of CMOS inverter. [5+5+5]

5. ( a ) How to scale the following parameters:
   (i) power-speed product (ii) power dissipation per gate (iii) Switching energy per gate (iv) Carrier density in channel
   ( b ) What are the various limits due to sub threshold currents? [8+7]

6. ( a ) Compare PLAs and PALs with suitable examples.
   ( b ) What is FPGA and how these are used in VLSI Design. [7+8]

7. (a) What are the different styles or models of VHDL explain them with suitable syntax.
   ( b ) How packages are different from libraries in VHDL? [10+5]

8. ( a ) How VHDL is used to get a logic level simulation?
   ( b) Write a VHDL program for a ripple counter and also write its test bench program. [7+8]

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Code No: R32045 **R10** **Set No: 2**

III B.Tech. II Semester Supplementary Examinations, January -2014

**VLSI DESIGN**

(Common to Electronics and Communication Engineering & Electronics and Computer Engineering & Electronics and Instrumentation Engineering)

**Time: 3 Hours** **Max Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks
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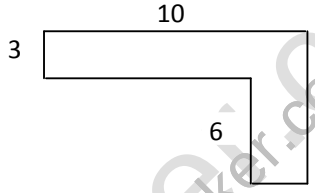
1. ( a ) Explain the various fabrication steps for CMOS technology with neat diagrams.
   ( b ) Compare speed and power performance of available technologies. [10+5]

2. ( a ) What is Threshold voltage and derive its expression.
   ( b) Derive the relation between pull-up and pull-down ratio for an nMOS inverter driven by another nMOS inverter. [7+8]

3. (a) Explain the design rules for p-well CMOS process.
   ( b ) Design and Draw the Layout of a 1-bit CMOS Shift Register and explain its shifting operation. [7+8]

4. ( a ) Find the sheet resistance of the following wire segment. All the measurements are in λ. [5+5+5]




   ( b ) Find the inverter pair delay for 4:1 ration nMOS inverter.
   ( c ) Draw the rise time model and find the equation for rise time of CMOS inverter.

5. ( a ) How to scale the following parameters: [8+7]
   (i) Maximum operating frequency (ii) Saturated current (iii) Channel resistance (iv) Power dissipation
   ( b ) What are the different effect of scaling on interconnect and contact resistances?

6. ( a ) Implement the following function with PALs.
   F= AC+AB'+B'C
   (b) Draw the basic architecture of FPGA and explain why these are called Field Programmable. [8+7]

7. ( a ) Compare the VHDL and Verilog HDL.
   ( b ) What are the different basic elements in VHDL and explain them. [7+8]

8. ( a ) How the VHDL logic synthesizer is used to verify logical operation of any given circuit?
   ( b ) Write a VHDL program to find number of ones in a given input and write its synthesis report . [7+8]

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Code No: R32045 **R10** **Set No: 3**

III B.Tech. II Semester Supplementary Examinations, January -2014

**VLSI DESIGN**

(Common to Electronics and Communication Engineering & Electronics and Computer Engineering & Electronics and Instrumentation Engineering)

**Time: 3 Hours** **Max Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks
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1. ( a ) Explain the various fabrication steps for pMOS technology with neat diagrams.
   ( b ) Discuss the Microelectronics evolutionary process with examples. [10+5]

2. ( a ) Draw the $I_{ds}$-$V_{ds}$ characteristics and derive the relation between $I_{ds}$ and W/L ratio.
   ( b ) Derive the relation between pull-up and pull-down ratio for an nMOS inverter driven through one or more pass transistors. [7+8]

3. ( a) Explain the design rules for wires and contacts. [8+7]
   ( b ) Design and Draw the Layout of CMOS NOR gate and explain its working.

4. Explain the following with suitable examples: [5+5+5]
   ( a ) Sheet resistance ( b ) Inverter delays ( c ) Propagation delays

5. ( a ) What are the different scaling factors for device parameters and explain how scale them?
   ( b ) What are the limitations on miniaturizing the size of transistor? [10+5]

6. ( a ) Implement the following function using PLAs
   F= abc' +ab'c +ac'
   ( b) Compare CPLDs and FPGAs in terms of architecture and applications. [8+7]

7. (a) How the variables and constants are assigned in VHDL?
   ( b ) What is mean by configuration bonding? How it is done in VHDL? [7+8]

8. (a) What are the different constraints can be provide using VHDL in synthesis analysis?
   ( b ) Write a VHDL program for a full adder and also write its test bench? [7+8]

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Code No: R32045 **R10** **Set No: 4**

III B.Tech. II Semester Supplementary Examinations, January -2014

**VLSI DESIGN**

(Common to Electronics and Communication Engineering & Electronics and Computer Engineering & Electronics and Instrumentation Engineering)

**Time: 3 Hours** **Max Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks
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1. ( a ) Explain the fabrication steps of twin-tub process for CMOS technology.
   ( b ) Compare BiCMOS and CMOS technologies. [10+5]

2. (a) Draw the structure of nMOS transistor and explain how $I_{ds}$ is depends on W/L ratio.
   ( b) What is Latchup in CMOS circuits? How to overcome it? [8+7]

3. ( a ) What are the Lambda-based design rules? Give some examples. [8+7]
   ( b ) Design and Draw the Layout of CMOS NAND gate and explain its working.

4. ( a ) How do you estimate the rise-time and fall-time of CMOS inverter?
   ( b ) Explain how to drive a large capacitive loads? [8+7]

5. ( a ) How to scale the following parameters:
   (i) Gate capacitance (ii) parasitic capacitance (iii) Channel resistance (iv) gate delay
   ( b ) Explain the effects of Substrate doping on Scaling. [8+7]

6. ( a ) Compare full custom and semicustom Design approaches with examples.
   ( b ) What is CPLDs? How these are used in VLSI designing? [8+7]

7. ( a ) What are the different design units in VHDL and explain them with suitable syntax.
   ( b ) How sequential statement are write in VHDL? Give some example. [8+7]

8. ( a ) How simulation and synthesis are obtained by VHDL?
   ( b ) Write a VHDL programme for a Decade counter. [7+8]

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