Code No: R32052 **R10** **Set No: 1**

III B.Tech. II Semester Regular/Supplementary Examinations, May/June -2014

COMPUTER ARCHITECTURE

(Computer Science and Engineering)

Time: 3 Hours **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. a) What are the different elements of Modern Computers? Explain briefly.
   b) What are the factors that influence the performance of a Processor?

2. a) What are the different Cache performance techniques that can be used to improve hit time, bandwidth, and miss penalty and miss rate.
   b) Give brief note on Pipelined Cache Access to Increase Cache Bandwidth.

3. a) Explain Vector Access Memory Schemes.
   b) Describe Multistage Crossbar Network in the Cray Y-MP 816.

4. a) Differentiate between centralized shared memory multiprocessors and distributed memory multiprocessors.
   b) Describe how architecture supports for protecting processes from each other via virtual memory.

5. a) Discuss about Message Routing Schemes.
   b) What is Snoopy bus protocol? Explain about the same.

6. a) What is Instruction Set? Explain Instruction Set Architectures.
   b) Explain Instruction Execution Phases.

7. a) Discuss various forms of parallelism.
   b) Discuss protection via Virtual Machines.

8. Write short notes on any two of the following.
   a) Inclusion.
   b) Advanced cache optimizations.
   c) Cray Y-MP 816 System Organization.

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Code No: R32052 **R10** **Set No: 2**

III B.Tech. II Semester Regular/Supplementary Examinations, May/June -2014

COMPUTER ARCHITECTURE

(Computer Science and Engineering)

Time: 3 Hours **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. a) What is the purpose of Distributed Memory Multiprocessor? Explain about the same.
   b) Give brief note on MIMD Computers.

2. a) What is multiprocessor cache coherence?
   b) Differentiate between instruction set architecture Vs computer Architecture.

3. Briefly explain the following.
   (a) Protection via virtual machines.
   (b) Vector Instruction Types.

4. a) What are the basic schemes for enforcing Coherence.
   b) Explain about Collision Free Scheduling problems.

5. a) What is Hot Spot problem? Discuss about it.
   b) Explain about Interprocessor Communication.

6. a) What is Deadlock Virtual Channel and how it works?
   b) Explain about Control Processors and Processing Nodes.

7. a) Describe forms of Parallelism.
   b) Explain CM-2 Architecture with the help of diagram.

8. Write short notes on any two of the following.
   (a) Parallel Algorithms.
   (b) Inclusion.
   (c) Characteristics of RISC architecture.

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Code No: R32052 **R10** **Set No: 3**

III B.Tech. II Semester Regular/Supplementary Examinations, May/June -2014

COMPUTER ARCHITECTURE

(Computer Science and Engineering)

Time: 3 Hours **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. a) Discuss evolution of Computer Architecture.
   b) Discuss the major factors that influence the cost of a computer and show how these factors are Changing over time.

2. a) Explain Protection via Virtual Machines.
   b) What is Memory Hierarchy and discuss Memory Hierarchy with the help of diagram?

3. a) Discuss characteristics of typical CISC and RISC Architecture.
   b) Discuss Asynchronous and Synchronous models for Linear and Nonlinear Pipeline Processors.

4. a) What are Collision Free scheduling problems and discuss in detail?
   b) Briefly explain Instruction Execution Phases.

5. a) What is Hot Spot Problem and discuss in detail?
   b) Explain Multistage Crossbar Network in the Cray Y-MP 816.

6. a) What is multiprocessor cache coherence?
   b) Describe the basic schemes for enforcing coherence.

7. a) Explain Parallel Algorithms.
   b) Describe directory based cache coherence protocol for Distributed memory multiprocessors.

8. a) Explain Interprocessor Communication.
   b) Explain Use of non blocking Cache to increase the Cache bandwidth.

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Code No: R32052 **R10** **Set No: 4**

III B.Tech. II Semester Regular/Supplementary Examinations, May/June -2014

COMPUTER ARCHITECTURE

(Computer Science and Engineering)

Time: 3 Hours **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. a) Discuss about SIMD Supercomputers.
   b) How the performance of a processor is represented and what factors that influence the performance?

2. a) Discuss characteristics of typical CISC and RISC Architecture.
   b) Explain Interprocessor Communications

3. a) Explain Flow Control Strategies.
   b) What is Hot Spot Problem and discuss in detail?

4. Discuss following under Linear and Nonlinear Pipeline Processors.
   (a) Clocking and Timing control.
   (b) Speedup.
   (c) Efficiency and Throughput.

5. a) Discuss Multicast Routing algorithms.
   b) Explain CM-2 Architecture.

6. Explain following protocols under Cache Coherence and Message Passing Mechanisms.
   (a) Snoopy Bus Protocols.
   (b) Directory based Protocols.

7. Write short notes on any two of the following.
   (a) Advanced Cache optimizations.
   (b) Practical issues in inter connection networks
   (c) Describe the ways of improving the performance of cache.

8. a) Discuss Structural Parallelism versus Instruction Level Parallelism.
   b) Explain Stream Processing.

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