Code No: R32045 **R10** **Set No: 1**

III B.Tech. II Semester Regular/Supplementary Examinations, May/June -2014

VLSI DESIGN

(Comm to Electronics and Communication Engineering & Electronics and Computer Engineering & Electronics and Instrumentation Engineering)

Time: 3 Hours **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. With neat diagrams, explain the different steps in n-well fabrication of CMOS transistors. [15]

2. a) Derive the expression for the threshold voltage of MOSFET.
   b) Explain the latch-up phenomenon in CMOS circuits and the methods by which that can be eliminated. [7+8]

3. a) Explain the color code used for drawing stick diagram for NMOS and PMOS designs.
   b) What are the different types of contact cuts made during the fabrication of an IC? Which one is commonly used and why?
   c) Draw the stick diagram for CMOS inverter. [15]

4. Describe three sources of writing capacitances. Explain the effect of writing capacitance on the performance of a VLSI circuit [15]

5. a) Explain about scaling models and scaling factors. [7+8]
   b) Explain different series and parallel combinations of push-up and pull-down networks

6. a) Compare CPLD and FPGA.
   b) Explain the methods of programming of PAL CMOS device. [8+7]

7. a) What are the different data types available in VHDL and how they are indicated?
   b) Write VHDL program for a 4-bit counter with asynchronous reset. [7+8]

8. a) How simulation is a very powerful technique in verifying a chip's timing characteristics?
   b) How random test generation is used for verification? [7+8]

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Code No: R32045 **R10** **Set No: 2**

III B.Tech. II Semester Regular/Supplementary Examinations, May/June -2014

VLSI DESIGN

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Time: 3 Hours **Max Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks
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1. a) Explain the process of thermal diffusion. [4+4+7]
   b) Compare wet and dry oxidation processes.
   c) What are the basic steps in n-MOS fabrication process? Explain them with diagrams.

2. a) Derive the expression for transit time for electron or hole.
   b) Explain channel length modulation and its importance. [7+8]

3. a) Design stick diagram for the function F = (A+B)(C+D).
   b) Design CMOS layout for the function $Y = (A.B+C+D)^{1}$. [8+7]

4. a) Derive the propagation delay τ_{PHL} for inverter.
   b) Draw the circuit diagram of complementary pass logic implementation of NAND/AND gate and explain its working. [7+8]

5. a) Explain how the transistor might be sized to optimize the delay through the carry stage in parallel adder.
   b) Design a two input XOR gate using a ROM. [8+7]

6. a) Differentiate between PROM, PAL and PLA.
   b) Implement a 3 bit synchronous counter using PAL. [7+8]

7. a) Explain how a FSM model is described in VHDL with suitable program.
   b) What is the difference between design capture tools and design verification tools? Give some examples of each. [7+8]

8. a) How simulation is a very powerful technique in verifying a chip's timing characteristics?
   b) How random test generation is used for verification? [8+7]

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Code No: R32045 **R10** **Set No: 3**

III B.Tech. II Semester Regular/Supplementary Examinations, May/June -2014

VLSI DESIGN

(Comm to Electronics and Communication Engineering & Electronics and Computer Engineering & Electronics and Instrumentation Engineering)

Time: 3 Hours **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. a) Discuss fabrication differences between NMOS and CMOS technologies. Which fabrication is preferred and why?
   b) Design the NMOS inverter circuit and explain its operation. [7+8]

2. a) With neat sketches explain the formation of the inversion layer in P-channel Enhancement MOSFET.
   b) Derive the expression for drain current of a CMOS transistor. [8+7]

3. a) What are the effects of constant voltage scaling on the current and power?
   b) What are the different design rules for wires and contacts? [7+8]

4. a) Explain how MOSFETs can be used as switches.
   b) What is inverter delay? How delay is calculated for multiple stages? [7+8]

5. a) Explain the Barrel Shifter operation with its circuit diagram.
   b) Explain the operation of zero/one detector. [8+7]

6. a) Draw the circuit diagram of six transistor SRAM cell and explain its working.
   b) Draw and explain the structure of an n-MOS ROM. [8+7]

7. a) Design logic diagram using PLA for the function
   $f = \Sigma m (0,1,3,5,7,11,14) + \Sigma \phi (2,6)$ diagram.
   b) Explain look up table (LUT) of FPGA with circuit diagram. [8+7]

8. Write short notes on following:
   (a) Technology Libraries.
   (b) post layout timing simulation.
   (c) Static timing. [5+5+5]

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Code No: R32045 **R10** **Set No: 4**

III B.Tech. II Semester Regular/Supplementary Examinations, May/June -2014

VLSI DESIGN

(Comm to Electronics and Communication Engineering & Electronics and Computer Engineering & Electronics and Instrumentation Engineering)

Time: 3 Hours **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. a) Distinguish between bipolar, n-MOS and CMOS transistor technologies.
   b) Explain the various steps in PMOS fabrication. [8+7]

2. a) Derive the expression for drain current of a CMOS transistor.
   b) Explain the working of a BiCMOS transistor. [8+7]

3. Design a stick diagram for two input CMOS NAND and NOR gates. [15]

4. a) Explain different types of capacitor loads for MOS transistors.
   b) Explain timing optimization with examples in VLSI design flow. [7+8]

5. With neat circuit diagram, explain the operation of
   (a) Carry look ahead adder
   (b) Barrel shifter. [7+8]

6. a) Explain about CPLD architecture and its applications.
   b) Implement a full subtractor by using PLA. [8+7]

7. With respect to synthesis process explain the following: [15]
   (a) Flattering
   (b) Factoring
   (c) Mapping.

8. a) Discuss different constraints of synthesis tools.
   b) Explain floor planning, place and route in detail. [5+10]

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